REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-08-02	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, GaAs, pHEMT, MMIC, 0.1 GHz to 6 GHz 1 W POWER AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/19618**
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AMSC N/A

5962-V119-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 0.1 GHz to 6 GHz, 1 W power amplifier microcircuit with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	HMC637ASCPZ-EP	GaAs, pHEMT, MMIC, 0.1 GHz to 6 GHz, 1 W power amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	32	MO-220-WHHD-4	Lead frame chip scale package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Drain bias voltage (V_{DD}) ..... 14 V_{DC}
Gate bias voltage control 1 (V_{GG1}) ..... -3 V_{DC} to 0 V_{DC}
Gate bias voltage control 2 (V_{GG2}) ..... 4 V_{DC} to 7 V_{DC}
Radio frequency input (RF_{IN}) power, V_{DD} = 12 V_{DC} ..... 25 dBm
Channel temperature ..... 175°C/W
Continuous power dissipation (P_D) : 2/
  T_C = +85°C ..... 8.6 W
  T_C = +125°C ..... 6.7 W
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum peak reflow temperature moisture sensitivity level 3 (MSL3) ..... 260°C
Thermal resistance, junction to case (θ_{JC}) ..... 10.5°C/W 3/
Electrostatic discharge (ESD) rating:
  Human body model (HDM) ..... 500 V, Class 1B

1.4 Recommended operating conditions. 4/

Drain bias voltage (V_{DD}) ..... 12 V
Gate bias voltage control 2 (V_{GG2}) ..... 5 V
Operating temperature range (T_A) ..... -55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ For maximum power dissipation versus case temperature, see figure 3.
3/ Thermal impedance simulated values are based on a JEDEC 1S0P thermal board test. See JEDEC JESD-51.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD 51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Maximum power dissipation versus case temperature graph. The Maximum power dissipation versus case temperature graph shall be as shown in figure 3.

3.5.4 Interface schematics. The interface schematics shall be as shown in figures 4, 5, 6, 7, 8, and 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency range			+25°C	01	0.1	6	GHz
Gain			+25°C	01	13 typical		dB
					12		
Gain flatness			+25°C	01	±0.75 typical		dB
Gain variation over temperature			-55°C to 125°C	01	0.015 typical		dB / °C
Return loss input			+25°C	01	12 typical		dB
Return loss output			+25°C	01	15 typical		dB
Output power for 1 dB compression	P1dB		+25°C	01	29 typical		dBm
					27		
Saturated output power	pSAT		+25°C	01	31 typical		dBm
Output third order intercept	OIP3	Output power (P_{OUT}) per tone = 10 dBm, 1 MHz spacing	+25°C	01	44 typical		dBm
Noise figure			+25°C	01	12 typical		dB
		2.0 GHz to 6.0 GHz			5 typical		
Supply current	I_{DD}		+25°C	01	400 typical		mA
					320	480	
Drain bias voltage 3/	V_{DD}	I_{DD} = 400 mA	+25°C	01	11.5 typical		V
					12.0 typical		
					12.5 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 12 V, V_{GG2} = 5 V, supply current (I_{DD}) = 400 mA (adjust V_{GG1} between -2 V to 0 V to achieve I_{DD} = 400 mA typical), 50 Ω system.

3/ V_{GG1} is initially set for nominal bias conditions of V_{DD} = 12 V and V_{GG2} = 5 V to achieve a I_{DD} = 400 mA typical, and then, adjust V_{DD} ± 0.5 V from 12 V to measure the I_{DD} variation.

Case X

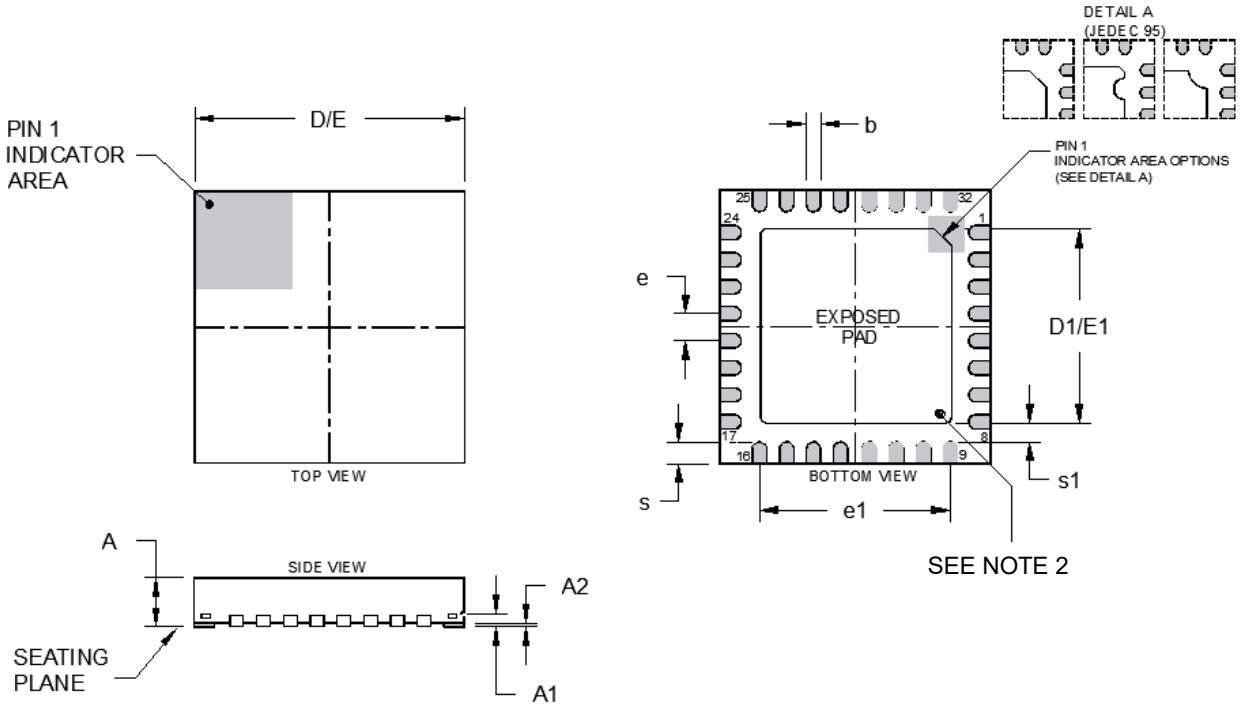


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/19618
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Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	.008 REF			0.203 REF		
A2	.003 COPLANARITY	.001	.002	0.08 COPLANARITY	0.02	0.05
b	.008	.010	.012	0.20	0.25	0.30
D/E	.193	.197	.201	4.90	5.00	5.10
D1/E1	.142	.145	.149	3.60	3.70	3.80
e	.20 BSC			0.50 BSC		
e1	.138 REF			3.50 REF		
s	.014	.016	.018	0.35	0.40	0.45
s1	.008	---	---	0.20	---	---

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WHHD-4.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NIC	17	NIC
2	V_{GG2}	18	NIC
3	NIC	19	NIC
4	GND	20	NIC
5	RFIN	21	RFOUT/V_{DD}
6	NIC	22	GND
7	NIC	23	NIC
8	NIC	24	NIC
9	NIC	25	NIC
10	NIC	26	NIC
11	NIC	27	NIC
12	GND	28	NIC
13	V_{GG1}	29	ACG2
14	NIC	30	ACG1
15	ACG4	31	NIC
16	ACG3	32	NIC

FIGURE 2. Terminal connections.

Device type	01
Case outlines	X
Terminal symbol	Description
NIC	No internal connection. These pins may be connected to RF ground. Performance is not affected.
V_{GG2}	Gate bias voltage control 2 for amplifier. Apply 5 V to V_{GG2} for nominal operation. Attach a bypass capacitor per the application circuit shown the Application Information section of the manufacturer's data sheet. See figure 4.
GND	Ground. Connect pin 4, pin 12, and pin 22 to RF and dc ground. See figure 9.
RF_{IN}	RF input. This pad is dc-coupled and matched to 50 Ω. See figures 6 and 7.
V_{GG1}	Gate bias voltage control 1 for amplifier. Attach a bypass capacitor per the application circuit shown in the Application Information section of the manufacturer's data sheet. Follow the power-up and power-down sequences outlined in the Application Information section of the manufacturer's data sheet. See figure 8.
ACG4	Low frequency termination 4. Attach a bypass capacitor per the application circuit shown in the Application Information section of the manufacturer's data sheet. See figure 7.
ACG3	Low frequency termination 3. Attach a bypass capacitor per the application circuit shown in the Application Information section of the manufacturer's data sheet. See figure 7.
RF_{OUT}/V_{DD}	RF output/drain bias voltage for amplifier. Connect the dc bias (V_{DD}) network to provide I_{DD}. See the application circuit shown in the Application Information section of the manufacturer's data sheet. See figure 5.
ACG2	Low frequency termination 2. Attach a bypass capacitor per the application circuit shown in the Application Information section of the manufacturer's data sheet. See figure 5.
ACG1	Low frequency termination 1. Attach a bypass capacitor per the application circuit shown in the Application Information section of the manufacturer's data sheet. See figure 5.
EPAD	Exposed pad. The exposed pad must be connected to RF and dc ground.

FIGURE 2. Terminal connections - continued.

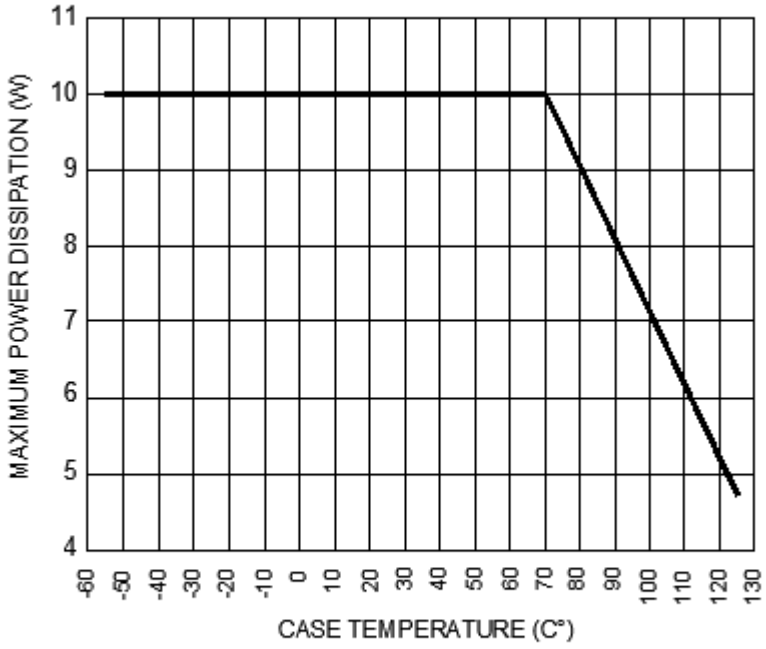
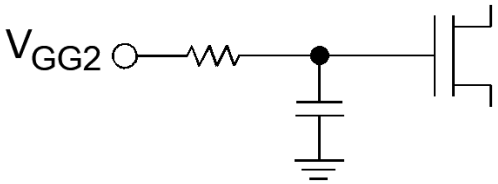
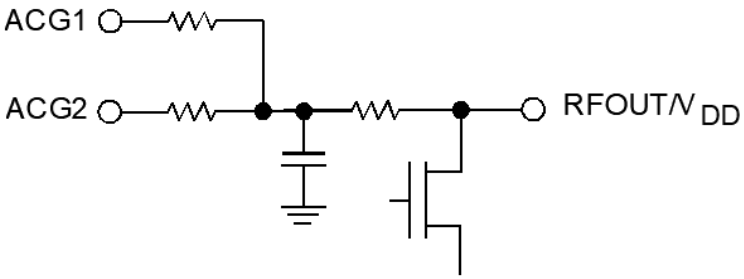
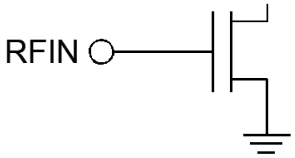


FIGURE 3. Maximum power dissipation versus case temperature.


V_{GG2}


ACG1
ACG2
RFOUT/V_{DD}


RFIN

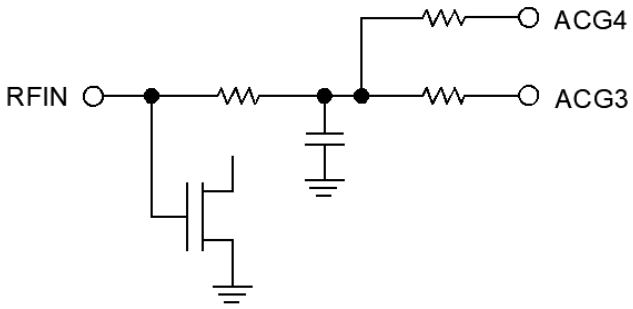


FIGURE 7. RFIN, ACG4, and ACG3 interface schematic.

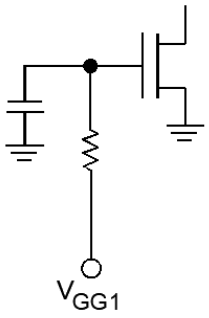


FIGURE 8. VGG1 interface schematic.



FIGURE 9. GND interface schematic.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/19618-01XE	24355	Cut reel, 50 units	H637AG	HMC637ASCPZ-EP-PT
		Reel, 500 units	H637AG	HMC637ASCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
Route 1 Industrial Park
P.O. Box 9106
Norwood, MA 02062
Point of contact: 20 Alpha Road
Chelmsford, MA 01824-4123