REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

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YY-MM-DD

19-10-03

CHECKED BY
RAJESH PITHADIA

APPROVED BY
JAMES R. ESCHMEYER

TITLE

MICROCIRCUIT, LINEAR, 3.0 V TO 5.5 V, ±12 kV IEC ESD PROTECTED, 50 MBPS RS-485 TRANSCEIVER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/19613

REV

PAGE 1 **OF** 28

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AMSC N/A

5962-V103-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.0 V to 5.5 V, ±12 kV International Electrotechnical Commission (IEC) electrostatic discharge (ESD) protected, 50 million bits per second (Mbps) RS-485 transceiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19613	-	01	T	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM3065E-EP	3.0 V to 5.5 V, ±12 kV IEC ESD protected, 50 Mbps RS-485 transceiver
02	ADM3066E-EP	3.0 V to 5.5 V, ±12 kV IEC ESD protected, 50 Mbps RS-485 transceiver
03	ADM3067E-EP	3.0 V to 5.5 V, ±12 kV IEC ESD protected, 50 Mbps RS-485 transceiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
U	8	MS-012-AA	Small outline package
T	8	MO-187-AA	Small outline package
X	10	MO-187-BA	Small outline package
Y	14	MS-012-AB	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}) to ground (GND) ..... 6 V
Input offset voltage (V_{IO}) to GND ..... -0.3 V to +6 V
Digital input and output voltage (DE, $\overline{RE}$, DI, and RO) ..... -0.3 V to V_{CC} + 0.3 V
Driver output and receiver input voltage ..... -9 V to +14 V
Continuous total power dissipation (P_D) :
  Case U ..... 0.225 W
  Case T ..... 0.151 W
  Case X ..... 0.151 W
  Case Y ..... 0.239 W
Maximum junction temperature (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Thermal resistance, junction to case (θ_{JC}): 2/
  Case U ..... 58.63°C/W
  Case T ..... 49.61°C/W
  Case X ..... 49.61°C/W
  Case Y ..... 42.90°C/W
Thermal resistance, junction to ambient (θ_{JA}): 2/
  Case U ..... 110.88°C/W
  Case T ..... 165.69°C/W
  Case X ..... 165.69°C/W
  Case Y ..... 104.5°C/W
Lead temperature:
  Soldering (10 seconds) ..... +300°C
  Vapor phase (60 seconds) ..... +215°C
  Infrared (15 seconds) ..... +220°C
Electrostatic discharge (ESD) on the bus pins (A, B, Y, Z):
  IEC 61000-4-2 contact discharge ..... ±12 kV
  IEC 61000-4-2 air discharge ..... ±15 kV
  DO-160 section 25 air discharge ..... ±15 kV
Electrostatic discharge (ESD) human body model (HDM) :
  On the bus pins (A, B,Y, Z) ..... ≥±30 kV
  All other pins ..... ±8 kV

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{CC}) ..... 3.0 V to 5.5 V
Input offset voltage (V_{IO}) :
  Device types 01 and 03 ..... $V_{IO} = V_{CC}$
  Device type 02 ..... 1.62 V to V_{CC}
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

International Electrotechnical Commission

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) - Part 4-2:
Testing and measurement techniques - Electrostatic discharge immunity test

(Copies of these documents are available online at https://www.iec.ch.)

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

Radio Technical Commission for Aeronautics (RTCA)

DO-160 – Environmental Conditions and Test Procedures for Airborne Equipment

(Copies of these documents are available from https://www.rtca.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms and test circuits. The timing waveforms and test circuit shall be as shown in figures 3 through 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
No load supply current	I_{CC}	DE = V_{IO}, $\overline{RE}$ = 0 V	25°C	01, 02, 03	2 typical		mA
			-55°C to +125°C			7.5	
		DE = V_{IO}, $\overline{RE}$ = V_{IO}	-55°C to +125°C			7.5	
		DE = 0 V, $\overline{RE}$ = 0 V	-55°C to +125°C			4.5	
Supply current, data rate = 50 Mbps		V_{CC} > 4.5 V, DE = V_{IO}, $\overline{RE}$ = 0 V, load resistance (R_L) = 54 Ω	25°C	01, 02, 03	107 typical		mA
			-55°C to +125°C			172	
		V_{CC} = 3.0 V, R_L = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V	25°C		67 typical		
			-55°C to +125°C			75	
Supply current in Shutdown mode	I_{SHDN}	DE = 0 V, $\overline{RE}$ = V_{IO}	25°C	01, 02, 03	210 typical		µA
			-55°C to +125°C			450	
V_{IO} shutdown current	I_{IOSHDN}	DE = 0 V, $\overline{RE}$ = V_{IO}	25°C	02,	1 typical		µA
			-55°C to +125°C			50	
Driver section							
Differential outputs							
Output voltage, loaded	$\lvert V_{OD2}\rvert$	V_{CC} ≥ 3.0 V, R_L = 50 Ω, see figure 3	-55°C to +125°C	01, 02, 03	2.0	V_{CC}	V
		V_{CC} ≥ 3.0 V, R_L = 27 Ω (RS-485), see figure 3			1.5	V_{CC}	
		V_{CC} ≥ 4.5V, R_L = 50 Ω, see figure 3			2.1	V_{CC}	
		V_{CC} ≥ 4.5 V, R_L = 27 Ω (RS-485), see figure 3			2.1	V_{CC}	
	$\lvert V_{OD3}\rvert$	V_{CC} ≥ 3.0 V, -7 V ≤ common mode voltage (VCM) ≤+12 V, see figure 4			1.5	V_{CC}	
		V_{CC} ≥ 4.5 V, -7 V ≤ V_{CM} ≤+12 V, see figure 4			2.1	V_{CC}	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver section –continued.							
Differential outputs – continued.							
Change in differential Input voltage for complementary output states	$\Delta\lvert V_{OD}\rvert$	R_L = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01, 02, 03		0.2	V
Common mode Output voltage	V_{OC}	R_L = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01, 02, 03		3.0	V
Change in common mode voltage for complementary output states	$\Delta\lvert V_{OC}\rvert$	R_L = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01, 02, 03		0.2	V
Output short circuit current	I_{OS}	-7 V < output voltage (V_{OUT}) < +12 V	-55°C to +125°C	01, 02, 03	-250	+250	mA
Output leakage (Y, Z) current	I_O	DE = 0 V, $\overline{RE}$ = 0 V, input voltage (V_{IN}) = 12 V, V_{CC} = 0 V or 3.6 V	-55°C to +125°C	03		+100	µA
		DE = 0 V, $\overline{RE}$ = 0 V, V_{IN} = -7 V, V_{CC} = 0 V or 3.6 V			-100		
Logic inputs (DE, $\overline{RE}$, DI)							
Input voltage, low	V_{IL}	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V	-55°C to +125°C	01, 02, 03		0.33 x V_{IO}	V
Input voltage, high	V_{IH}	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V	-55°C to +125°C	01, 02, 03	0.67 x V_{IO}		V
Input current	I_I	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}	-55°C to +125°C	01, 02, 03	-2	+2	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver section							
Differential inputs							
Differential input threshold voltage	V_{TH}	-7 V < V_{CM} < +12 V	+25°C	01, 02, 03	-125 typical		mV
			-55°C to +125°C		-200	-30	
Input voltage hysteresis	V_{HYS}	-7 V < V_{CM} < +12 V	+25°C	01, 02, 03	30 typical		mV
Input current (A,B)	I_I	DE = 0 V, V_{IN} = 12 V, V_{CC} = powered/unpowered	-55°C to +125°C	01, 02, 03		0.25	mA
		DE = 0 V, V_{IN} = -7 V, V_{CC} = powered/unpowered			-0.20		
Line input resistance	R_{IN}	-7 V < V_{CM} < +12 V	-55°C to +125°C	01, 02, 03	48		kΩ
Logic inputs							
Output voltage, low	V_{OL}	V_{IO} = 3.6 V, V_{ID} ≤ -0.2 V, 3/ output current (I_{OUT}) = 2 mA	-55°C to +125°C	01, 02, 03		0.4	V
		V_{IO} = 2.7 V, V_{ID} ≤ -0.2 V, 3/ I_{OUT} = 2 mA		02		0.4	
		V_{IO} = 1.95 V, V_{ID} ≤ -0.2 V, 3/ I_{OUT} = 500 μA		02		0.2	
Output voltage, high	V_{OH}	V_{IO} = 3.0 V, V_{ID} ≤ -0.03 V, 3/ I_{OUT} = -2 mA	-55°C to +125°C	01, 02, 03	2.4		V
		V_{IO} = 2.3 V, V_{ID} ≤ -0.03 V, 3/ I_{OUT} = -1 mA		02	2.4		
		V_{IO} = 1.65 V, V_{ID} ≤ -0.03 V, 3/ I_{OUT} = -500 μA		02	V_{IO} – 0.2		
Short circuit current		V_{OUT} = GND or V_{IO}	-55°C to +125°C	01, 02, 03		85	mA
Three state output leakage		RO = 0 V or V_{IO}	-55°C to +125°C	01, 02, 03		±2	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification section							
Driver							
Maximum date rate 5/			-55°C to +125°C	02	50		Mbps
Propagation delay	t_{DPLH}, t_{DPHL}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figures 5 and 6	+25°C	02	9 typical		ns
			-55°C to +125°C			15	
Skew	t_{DSKEW}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figures 5 and 6	+25°C	02	1 typical		ns
			-55°C to +125°C			2	
Rise/fall times	t_{DR}, t_{DF}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figures 5 and 6	+25°C	02	4 typical		ns
			-55°C to +125°C			6.7	
Enable to output high	t_{DZH}	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	+25°C	02	10 typical		ns
			-55°C to +125°C			30	
Enable to output low	t_{DZL}	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	+25°C	02	10 typical		ns
			-55°C to +125°C			30	
Disable to output low	t_{DLZ}	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	+25°C	02	10 typical		ns
			-55°C to +125°C			30	
Disable to output high	t_{DHZ}	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	+25°C	02	10 typical		ns
			-55°C to +125°C			30	
Enable time from Shutdown to high	$t_{DZH(SHDN)}$	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	-55°C to +125°C	02		2000	ns
Enable time from Shutdown to low	$t_{DZL(SHDN)}$	R_L = 110 Ω, C_L = 50 pF, see figures 7 and 8	-55°C to +125°C	02		2000	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification section – continued.							
Receiver							
Maximum data rate			-55°C to +125°C	02	50		Mbps
Propagation delay	t_{RPLH}, t_{RPHL}	C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, V_{CM} = 1.5 V, see figures 9 and 10	-55°C to +125°C	02		35	ns
Skew/pulse width distortion	t_{RSKEW}	C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, V_{CM} = 1.5 V, see figures 9 and 10	-55°C to +125°C	02		3.5	ns
Enable to output high	t_{RZH}	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, DE high, see figures 11 and 12	+25°C	02	10 typical		ns
			-55°C to +125°C			35	
Enable to output low	t_{RZL}	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, DE high, see figures 11 and 12	+25°C	02	10 typical		ns
			-55°C to +125°C			35	
Disable time from low	t_{RLZ}	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, DE high, see figures 11 and 12	+25°C	02	10 typical		ns
			-55°C to +125°C			35	
Enable time from high	t_{RHZ}	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq 1.5$ V, DE high, see figures 11 and 12	+25°C	02	10 typical		ns
			-55°C to +125°C			35	
Enable from 7/ Shutdown to high	$t_{RZH(SHDN)}$	R_L = 110 Ω, C_L = 50 pF, see figures 11 and 13	-55°C to +125°C	02		2000	ns
Enable from 7/ Shutdown to low	$t_{RZL(SHDN)}$	R_L = 110 Ω, C_L = 50 pF, see figures 11 and 13	-55°C to +125°C	02		2000	ns
Time to Shutdown 8/	t_{SHDN}		-55°C to +125°C	02	40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IO} = V_{CC} for device types 01 and 03; V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} for device type 02, T_A = -55°C to +125°C. All typical specifications are at T_A = +25°C, V_{IO} = V_{CC} = 3.3 V.

3/ V_{ID} is the receiver input differential voltage.

4/ Unless otherwise specified, V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} for device type 02, T_A = -55°C to +125°C. All typical specifications are at T_A = +25°C, V_{IO} = V_{CC} = 3.3 V.

5/ Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1.

6/ $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when DE changes from 0 V to V_{CC}. $\overline{RE}$ = V_{CC} for this condition.

7/ $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when $\overline{RE}$ changes from V_{CC} to 0 V. DE = 0 V for this condition.

8/ Minimum time required to put the device into shutdown: DE and $\overline{RE}$ must be disabled for more than 40 ns for the device to go into shutdown

Case T

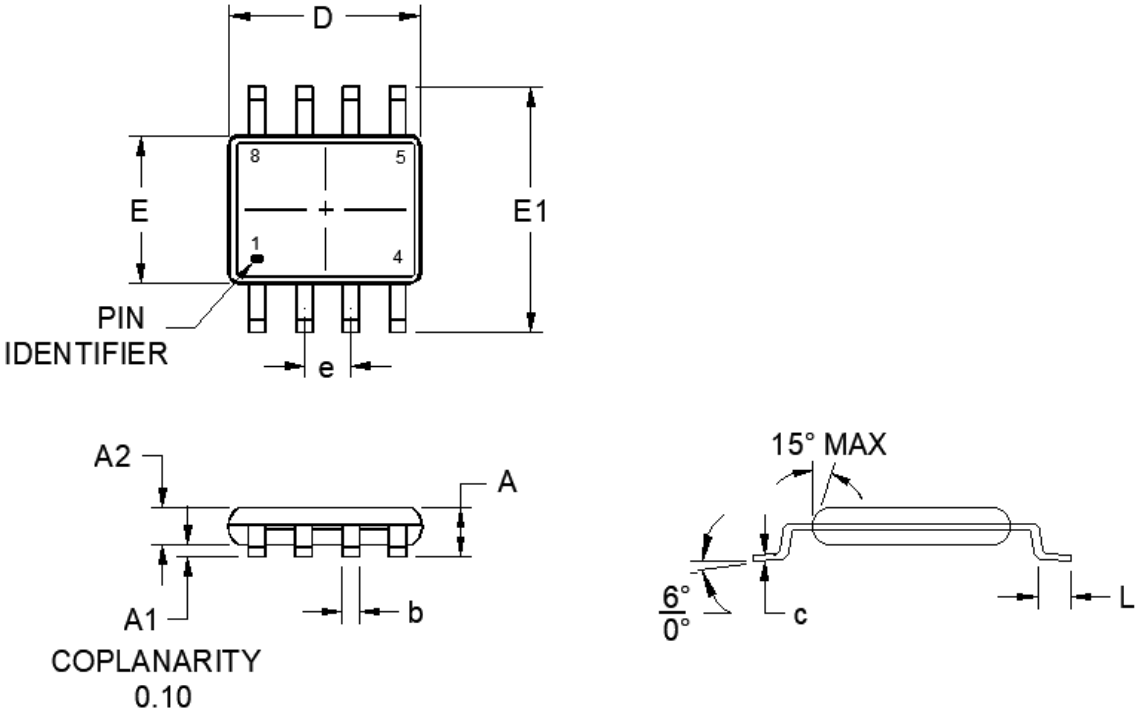


FIGURE 1. Case outlines.

Case T - continued

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A		---	.0433	---	---	1.10
A1	.0019	---	.0059	0.05	---	0.15
A2	.0295	.0334	.0374	0.75	0.85	0.95
b	.0098	---	.0157	0.25	---	0.40
c	.0035	---	.0090	0.09	---	0.23
D	.1102	.1181	.1259	2.80	3.00	3.20
E	.1102	.1181	.1259	2.80	3.00	3.20
E1	.1830	.1929	.2027	4.65	4.90	5.15
e	.0255 BSC			0.65 BSC		
L	.0157	.0216	.0314	0.40	0.55	0.80

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO187-AA.

FIGURE 1. Case outlines - Continued.

Case U

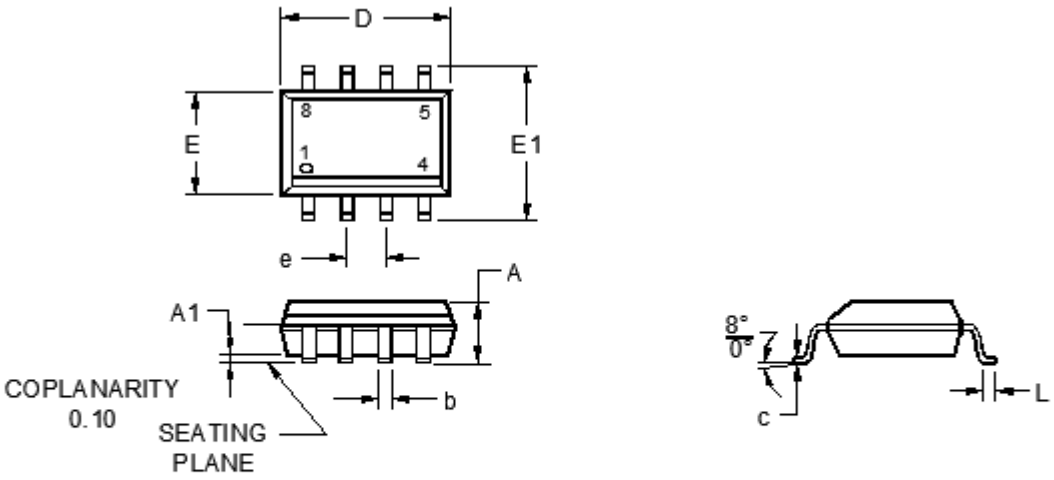


FIGURE 1. Case outlines - Continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.0122	.0201	0.31	0.51
c	.0067	.0098	0.17	0.25
D	.1890	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
E1	.2284	.2441	5.80	6.20
e	.0500 BSC		1.27 BSC	
L	.0157	.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AA

FIGURE 1. Case outlines - Continued.

Case X

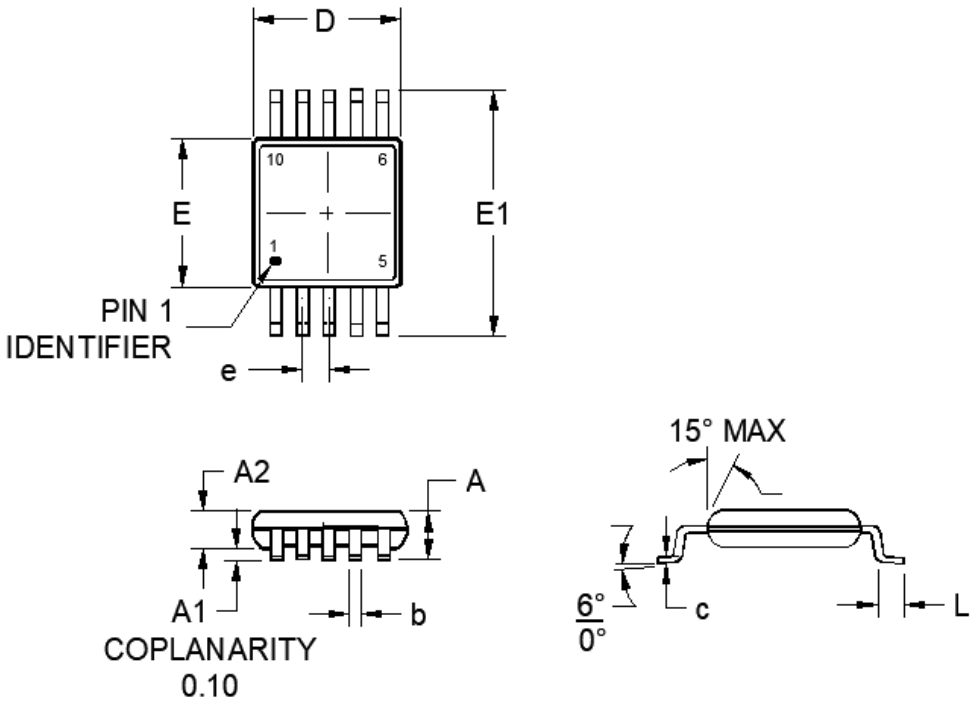


FIGURE 1. Case outlines - Continued.

Case X - continued

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.0433	---	---	1.10
A1	.0019	---	.0059	0.05	---	0.15
A2	.0295	.0334	.0374	0.75	0.85	0.95
b	.0059	---	.0118	0.15	---	0.30
c	.0051	---	.0090	0.13	---	0.23
D	.1141	.1181	.1220	2.90	3.00	3.10
E	.1141	.1181	.1220	2.90	3.00	3.10
E1	.1830	.1929	.2027	4.65	4.90	5.15
e	.0196 BSC			0.50 BSC		
L	.0157	.0216	.0275	0.40	0.55	0.70

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-BA.

FIGURE 1. Case outlines - Continued.

Case Y

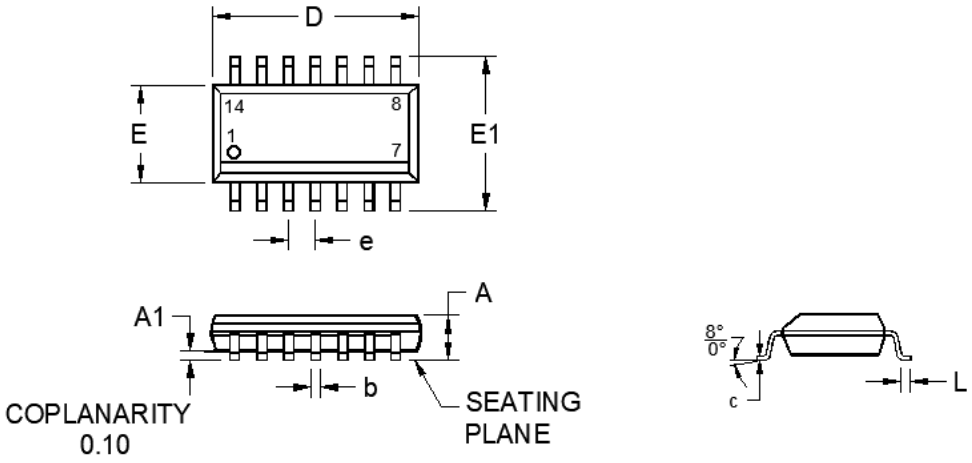


FIGURE 1. Case outlines - Continued.

Case Y - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0531	.0689	1.35	1.75
A1	.0039	.0098	0.10	0.25
b	.0122	.0201	0.31	0.51
c	.0067	.0098	0.17	0.25
D	.3366	.3445	8.55	8.75
E	.1496	.1575	3.80	4.00
E1	.2283	.2441	5.80	6.20
e	.0500 BSC		1.27 BSC	
L	.0157	.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AB.

FIGURE 1. Case outlines - Continued.

Device type	01	
Case outlines	U and T	
Terminal number	Terminal symbol	Description
1	RO	Receiver output data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
2	$\overline{RE}$	Receiver enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
3	DE	Driver enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	DI	Transmit data input. Data to be transmitted by the driver is applied to this input.
5	GND	Ground.
6	A	Noninverting driver output and receiver Input. When the driver is disabled, or when V_{CC} is powered down, pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting driver output and receiver input. When the driver is disabled, or when V_{CC} is powered down, pin B is put into a high impedance state to avoid overloading the bus.
8	V_{CC}	3.0 V to 5.5 V power supply. Adding a 0.1 μF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

FIGURE 2. Terminal connections.

Device type	02	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{IO}	1.62 V to 5.5 V logic supply. Adding a 0.1 µF decoupling capacitor between the V_{IO} pin and the GND pin is recommended.
2	RO	Receiver output data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	DE	Driver enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	$\overline{RE}$	Receiver enable input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DI	Transmit data input. Data to be transmitted by the driver is applied to this input.
6	GND	Ground.
7	NIC	No internal connection. This pin is not internally connected.
8	A	Noninverting driver output and receiver input. When the driver is disabled, or when V_{CC} is powered down, pin A is put into a high impedance state to avoid overloading the bus.
9	B	Inverting driver output and receiver input. When the driver is disabled, or when V_{CC} is powered down, pin B is put into a high impedance state to avoid overloading the bus.
10	V_{CC}	3.0 V to 5.5 V power supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

FIGURE 2. Terminal connections - Continued.

Device type	03	
Case outline	Y	
Terminal number	Terminal symbol	Description
1	NIC	No internal connection. This pin is not internally connected.
2	RO	Receiver output data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	$\overline{RE}$	Receiver enable input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
4	DE	Driver enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level places the driver output into a high impedance state.
5	DI	Transmit data input. Data to be transmitted by the driver is applied to this input.
6	GND	Ground.
7	GND	Ground.
8	NIC	No internal connection. This pin is not internally connected.
9	Y	Driver noninverting output. When the driver is disabled, or when V_{CC} is powered down, pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Driver inverting output. When the driver is disabled, or when V_{CC} is powered down, pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting receiver input.
12	A	Noninverting receiver input.
13	V_{CC}	3.0 V to 5.5 V power supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.
14	V_{CC}	3.0 V to 5.5 V power supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

FIGURE 2. Terminal connections - Continued.

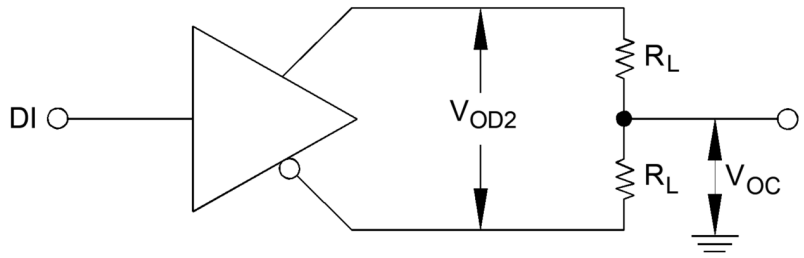


FIGURE 3. Driver voltage measurements.

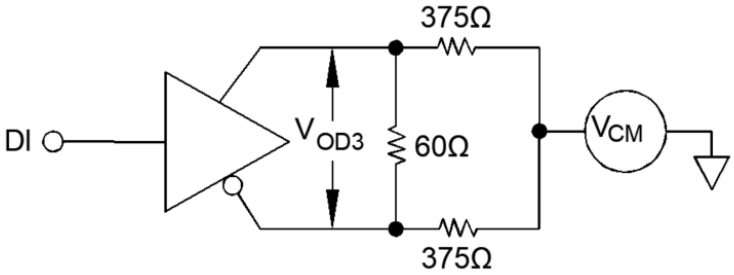
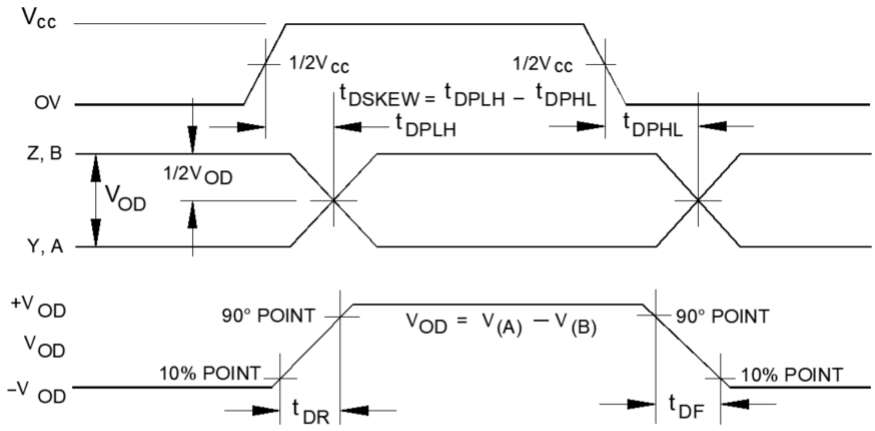


FIGURE 4. Driver voltage measurements over common mode range.



NOTES:

1. V_{OD} is the difference between A and B, with $+V_{OD}$ being the maximum point of V_{OD}, and $–V_{OD}$ being the minimum point of V_{OD}.
2. $V_{CC} = V_{IO}$ for device type 02.

FIGURE 5. Driver propagation delay rise and fall timing diagram.

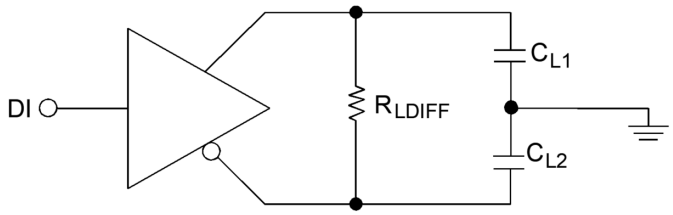
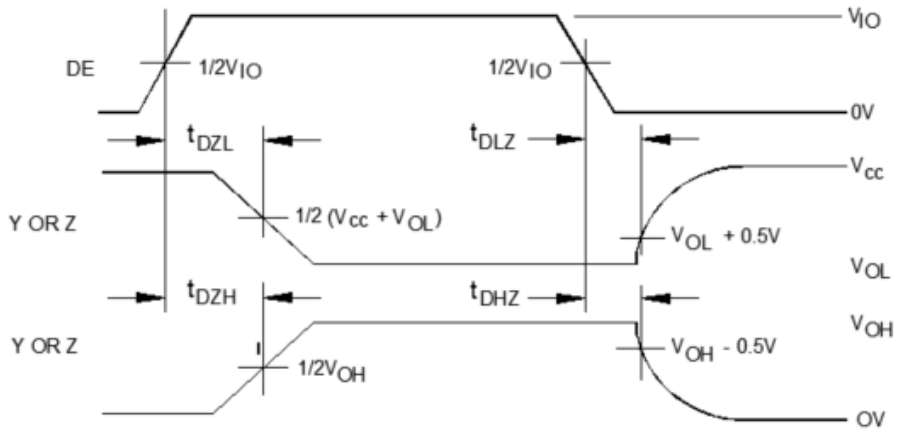


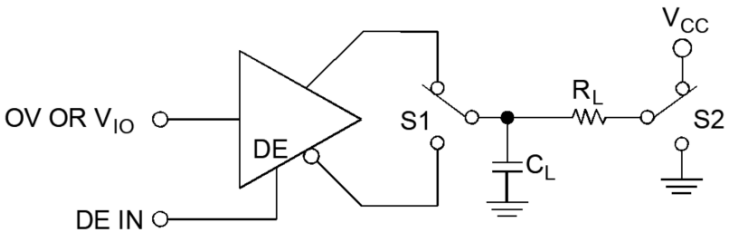
FIGURE 6. Driver propagation delay.



NOTES:

1. V_{IO} = V_{CC} for device types 01 and 03.
2. Y = A, Z = B for device types 01 and 02.

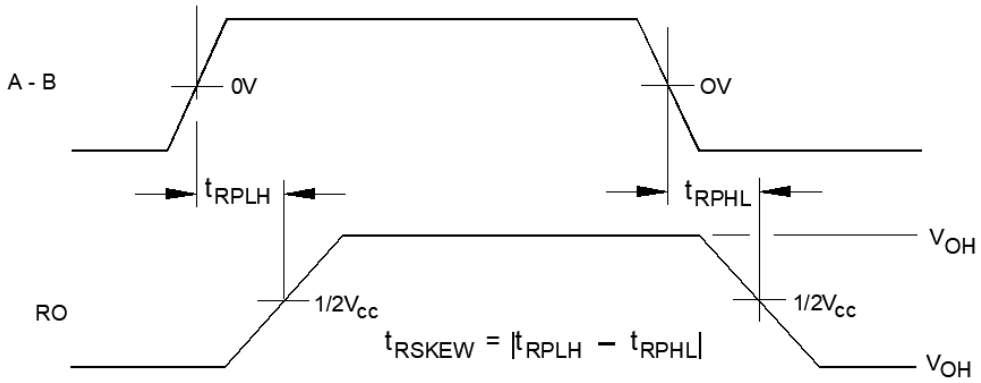
FIGURE 7. Driver enable and disable timing diagram.



NOTES:

1. V_{IO} = V_{CC} for device types 01 and 03.

FIGURE 8. Driver enable/disable.



NOTES:

1. V_{IO} = V_{CC} for device type 02.

FIGURE 9. Receiver propagation delay timing diagram.

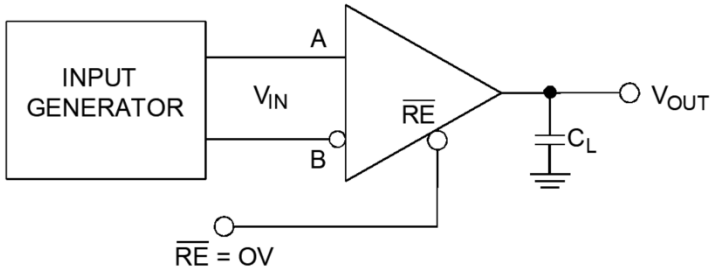
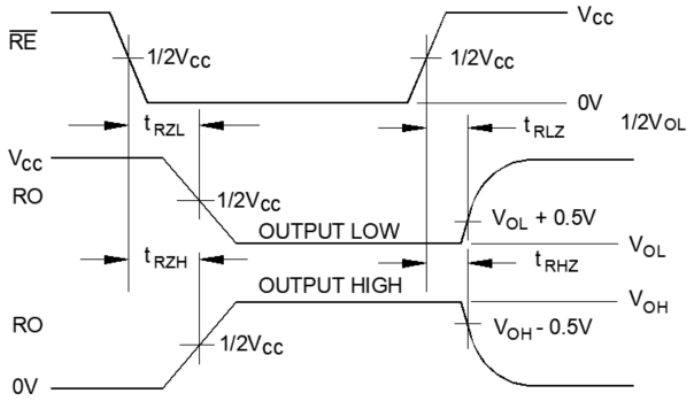
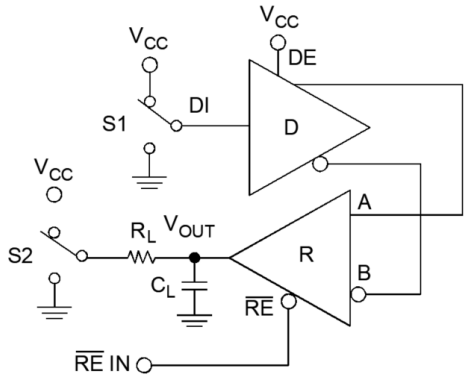


FIGURE 10. Receiver propagation delay/skew.



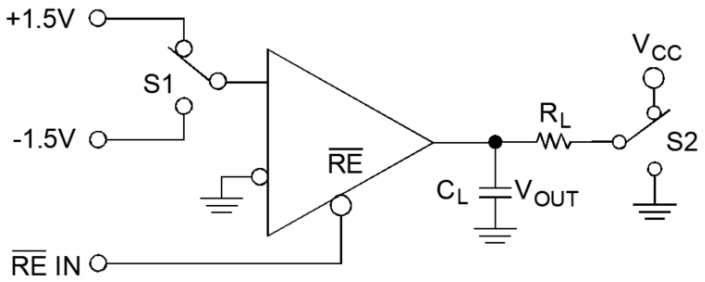
NOTES:
1. V_{IO} = V_{CC} for device type 02.

FIGURE 11. Receiver enable and disable timing diagram.



NOTES:
1. V_{IO} = V_{CC} for device type 02.

FIGURE 12. Receiver enable/disable.



NOTES:
1. V_{IO} = V_{CC} for device type 02.

FIGURE 13. Receiver enable/disable from Shutdown.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/19613-01TE	24355	Tube, 50 units	ADM3065ETRMZ-EP
		Reel, 250 units	ADM3065ETRMZ-EP-R7
V62/19613-01UE	24355	Tube, 98 units	ADM3065ETRZ-EP
		Reel, 1000 units	ADM3065ETRZ-EP-R7
V62/19613-02XE	24355	Tube, 50 units	ADM3066ETRMZ-EP
		Reel, 1000 units	ADM3066ETRMZ-EP-R7
V62/19613-03YE	24355	Tube, 56 units	ADM3067ETRZ-EP
		Reel, 1000 units	ADM3067ETRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123