REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make corrections to figures 5, 7, 9, and 11 by replacing the subscript "1O" with "IO". - ro	18-05-02	C. SAFFLE
B	Make corrections to Figure 7 by deleting $12V_{IO}$ and replacing with $1/2V_{IO}$ and deleting $12V_{CC}$ and replacing with $1/2V_{CC}$. Make correction to figure 11 by deleting RE and replacing with $\overline{RE}$. Update document paragraphs to current requirements. - ro	23-08-17	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																							
SHEET																							
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

Original date of drawing

YY-MM-DD
17-12-07

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TITLE
MICROCIRCUIT, LINEAR, LEVEL 4 DO-160G EMC PROTECTED RS-485 TRANSCEIVER WITH FULL ±42 V FAULT PROTECTION, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/17618
REV B		PAGE 1 OF 18

AMSC N/A

5962-V107-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Level 4 DO-160G electromagnetic capability (EMC) protected RS-485 transceiver with full ±42 V fault protection microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM3095E-EP	Level 4 DO-160G electromagnetic capability (EMC) protected RS-485 transceiver with full ±42 V fault protection

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012-AC	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC}) to ground (GND)	-0.5 V to +7 V
Input offset voltage (V_{IO}) to ground (GND)	-0.5 V to +7 V
Digital input/output voltage (DE, $\overline{RE}$, TxD, RxD)	-0.3 V to V_{IO} + 0.3 V
Driver output/receiver input voltage	±48 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature range (T_J)	150°C
Continuous total power dissipation (P_D)	400 mW
Lead temperature:	
Soldering (10 seconds)	300°C
Vapor phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Electrostatic discharge (ESD) (A and B pins only):	
IEC 61000-4-2 contact discharge	±8 kV
IEC 61000-4-2 air discharge	±15 kV
Electrical fast transients (EFT) (A and B pins only):	
IEC 61000-4-4 level 4 EFT	±2 kV
Surge (A and B pins only):	
IEC 61000-4-5 level 4 surge	±4 kV
Human body model (HBM) ESD protection:	
All pins	±4 kV
A and B pins only	>±30 kV
Field induced charged device model (FICDM) ESD	±1.25 kV
Thermal resistance, junction to ambient (θ_{JC})	18.9°C/W 2/
Thermal resistance, junction to ambient (θ_{JA})	50.9°C/W 2/

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{CC})	3.0 V to 5.5 V
Operating temperature range (T_A)	-55°C to +125°C

_____

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias. See JEDEC JESD51.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

International Electrotechnical Commission

IEC 61000-4-2	–	Electromagnetic Compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
IEC 61000-4-4	–	Electromagnetic Compatibility (EMC) - Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test
IEC 61000-4-5	–	Electromagnetic Compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test

(Copies of these documents are available from https://www.iec.org.)

JEDEC Solid State Technology Association

JEDEC JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Test circuit. The test circuit shall be as shown in figure 3, 4, 6, 8, 10, and 12.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 5, 7, 9, and 11.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{CC} = 3.0 V to 5.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver							
Differential output voltage	V_{OD}	$V_{CC} \geq$ 3.0 V, R = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01	1.5	5.0	V
		$V_{CC} \geq$ 4.5 V, R = 27 Ω or 50 Ω, see figure 3			2.1	5.0	
Differential output voltage or common mode range	$\|V_{OD3}\|$	$V_{CC} \geq$ 3.0 V, V_{CM} = -25 V to +25 V, see figure 4	-55°C to +125°C	01	1.5	5.0	V
		$V_{CC} \geq$ 4.5 V, V_{CM} = -25 V to +25 V, see figure 4			2.1	5.0	
Δ|VOD| for complementary output states		R = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01		0.2	V
Common mode output voltage	V_{OC}	R = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01		3	V
Δ|VOC| for complementary output states		R = 27 Ω or 50 Ω, see figure 3	-55°C to +125°C	01		0.2	V
High output short circuit current	V_{OUT}	-42 V ≤ V_{SC} 2/ ≤ +42 V	-55°C to +125°C	01	-250	+250	mA
Low output short circuit current	V_{OUT}	-42 V ≤ V_{SC} 2/ ≤ +42 V	-55°C to +125°C	01	-250	+250	mA
Driver input logic							
Input logic threshold low		1.62 V ≤ V_{IO} ≤ 5.5 V	-55°C to +125°C	01		0.33 x V_{IO}	V
Input logic threshold high		1.62 V ≤ V_{IO} ≤ 5.5 V	-55°C to +125°C	01	0.7 x V_{IO}		V
Logic input current		0 ≤ V_{IN} ≤ V_{IO}	-55°C to +125°C	01		±1	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{CC} = 3.0 V to 5.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver							
Differential input threshold	V_{TH}	-25 V ≤ V_{CM} ≤ +25 V	-55°C to +125°C	01	-125 typical		mV
					-200	-30	
Input hysteresis	ΔV_{TH}	-25 V ≤ V_{CM} ≤ +25 V	-55°C to +125°C	01	30 typical		mV
Input resistance (A, B)		-25 V ≤ V_{CM} ≤ +25 V	-55°C to +125°C	01	96		kΩ
Input capacitance (A, B)			+25°C	01	150 typical		pF
Input current (A, B)		DE = 0 V, V_{CC} = 0 V or +5 V, V_{IN} = ±25 V	-55°C to +125°C	01	-1.0	+1.0	mA
		DE = 0 V, V_{CC} = 0 V or +5 V, V_{IN} = ±42 V			-1.0	+1.0	
CMOS logic input current ($\overline{RE}$)			-55°C to +125°C	01		±1	μA
Low output voltage	V_{OL}	I_{OUT} = 300 μA	-55°C to +125°C	01		0.2	V
High output voltage	V_{OH}	V_{IO} ≥ +1.62 V, I_{OUT} = -300 μA	-55°C to +125°C	01	V_{IO} – 0.2		V
Output short circuit current		V_{OUT} = GND or V_{IO}, $\overline{RE}$ = 0 V, V_{IO} ≥ 3.0 V	-55°C to +125°C	01	4	85	mA
		V_{OUT} = GND/V_{IO}, $\overline{RE}$ = 0 V, V_{IO} < 3.0 V				85	
Three state output leakage current		$\overline{RE}$ = V_{IO}, RxD = 0 V or V_{IO}	-55°C to +125°C	01		±2	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{CC} = 3.0 V to 5.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply							
Input offset voltage	V_{IO}		-55°C to +125°C	01	1.62	V_{CC}	V
Supply current	I_{CC}	No load, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V	-55°C to +125°C	01		8	mA
		TxD data rate = 2.5 Mbps, No load, DE = V_{CC} = V_{IO}, $\overline{RE}$ = V_{CC} = V_{IO}				50	
		RxD data rate = 2.5 Mbps, No load, DE = 0 V, $\overline{RE}$ = 0 V				6	
		TxD/RxD data rate = 2.5 Mbps, No load, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V				90	
		TxD/RxD data rate = 2.5 Mbps, R_L = 54 Ω, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V				130	
		TxD/RxD data rate = 2.5 Mbps, R_L = 54 Ω, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V, V_{CC} = 5.5 V			90 typical		
		TxD/RxD data rate = 2.5 Mbps, R_L = 54 Ω, DE = V_{CC} = V_{IO}, $\overline{RE}$ = 0 V, V_{CC} = 3.0 V			45 typical		
Supply current in shutdown mode		DE = 0 V, $\overline{RE}$ = V_{CC} = V_{IO}	-55°C to +125°C	01		5	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC}	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver							
Data rate			-55°C to +125°C	01		2.5	Mbps
Propagation delay	t_{PLH}, t_{PHL}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figure 5 and figure 6	-55°C to +125°C	01	35 typical		ns
						500	
Differential skew	t_{SKEW}	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figure 5 and figure 6	-55°C to +125°C	01	10 typical		ns
						50	
Rise/fall times	t_R, t_F	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see figure 5 and figure 6	-55°C to +125°C	01	40 typical		ns
						130	
Enable time	t_{ZH}, t_{ZL}	R_L = 110 Ω, C_L = 50 pF, see figure 7 and figure 8	-55°C to +125°C	01	500 typical		ns
						2500	
Disable time	t_{HZ}, t_{LZ}	R_L = 110 Ω, C_L = 50 pF, see figure 7 and figure 8	-55°C to +125°C	01	500 typical		ns
						2500	
Enable time from shutdown	t_{HZ}, t_{LZ}	R_L = 110 Ω, C_L = 50 pF, see figure 7 and figure 8	-55°C to +125°C	01	4000 typical		ns
						5500	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC}	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver							
Propagation delay	t_{PLH}, t_{PHL}	C_L = +15 pF, V_{ID} 3/ ≥ ±1.5 V, see figure 9 and figure 10	-55°C to +125°C	01	120 typical		ns
						200	
		C_L = +15 pF, V_{ID} 3/ ≥ ±600 mV, see figure 9 and figure 10			140 typical		
						220	
Skew	t_{SKEW}	C_L = +15 pF, V_{ID} 3/ ≥ ±1.5 V, see figure 9 and figure 10	-55°C to +125°C	01	4 typical		ns
						40	
Enable time	t_{ZH}, t_{ZL}	R_L = 1 kΩ, C_L = 15 pF, see figure 11 and figure 12	-55°C to +125°C	01	12 typical		ns
						55	
Disable time	t_{HZ}, t_{LZ}	R_L = 1 kΩ, C_L = 15 pF, see figure 11 and figure 12	-55°C to +125°C	01	12 typical		ns
						55	
Enable time from shutdown		R_L = 1 kΩ, C_L = 15 pF, see figure 11 and figure 12	-55°C to +125°C	01	3000 typical		ns
						4500	
Time to shutdown		R_L = 1 kΩ, C_L = 15 pF, see figure 11 and figure 12	-55°C to +125°C	01	330 typical		ns
					50	3000	
Rx, pulse width distortion		C_L = +15 pF, V_{ID} 3/ ≥ ±1.5 V, see figure 9 and figure 10	-55°C to +125°C	01		40	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{SC} is the short voltage at the RS-485 A or B bus pin.

3/ V_{ID} is the input differential voltage to the RS-485 receiver.

Case X

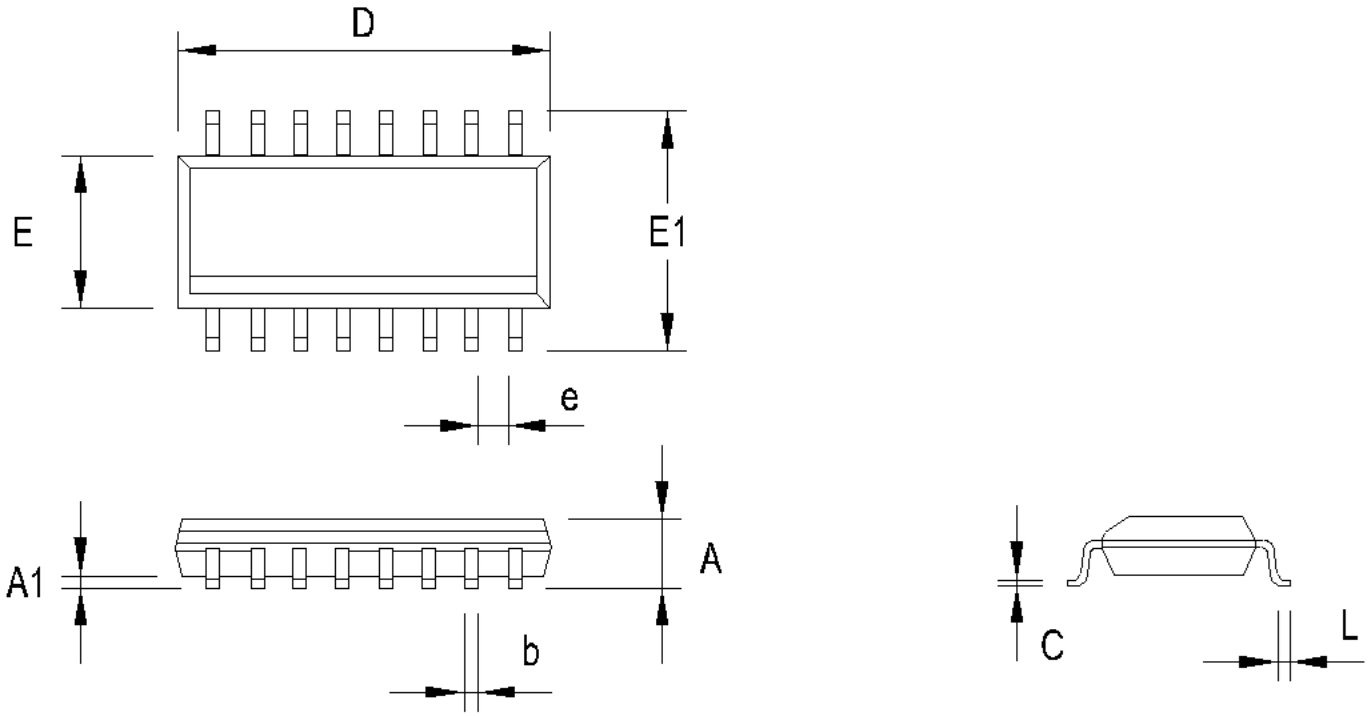


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0531	.0689	1.35	1.75
A1	.0039	.0098	0.10	0.25
b	.0122	.0201	0.31	0.51
c	.0067	.0098	0.17	0.25
D	.3858	.3937	9.80	10.00
E	.1496	.1575	3.80	4.00
E1	.2283	.2441	5.80	6.20
e	.0500 BSC		1.27 BSC	
L	.0157	.0500	0.40	1.27

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	GND	Ground.
2	V_{CC}	3.0 V to 5.5 V power supply. It is recommended that a 0.1 μF decoupling capacitor is added between pin V_{CC} and pin GND.
3	V_{IO}	1.62 V to 5.5 V V_{IO} logic supply. It is recommended that a 0.1 μF decoupling capacitor is added between pin V_{IO} and pin GND.
4	TxD	Transmit data input. Data transmitted by the driver is applied to this input.
5	DE	Driver output enable. A high level on this pin enables the A and B driver differential outputs. A low level places them into a high impedance state.
6	$\overline{RE}$	Receiver enable input. This is an active low input. Driving this input low enables the receiver and driving the input high disables the receiver.
7	RxD	Receiver output data. This output is high when $(A - B) > -30$ mV and low when $(A - B) < -200$ mV.
8	GND	Ground.
9	GND	Ground.
10	GND	Ground.
11	A	Noninverting driver output/receiver input. When the driver is disabled, or when V_{CC} is powered down, pin A is put into a high impedance state to avoid overloading the bus.
12	GND	Ground.
13	GND	Ground.
14	B	Inverting driver output/receiver input. When the driver is disabled, or when V_{CC} is powered down, pin B is put into a high impedance state to avoid overloading the bus.
15	GND	Ground.
16	GND	Ground.

FIGURE 2. Terminal connections.

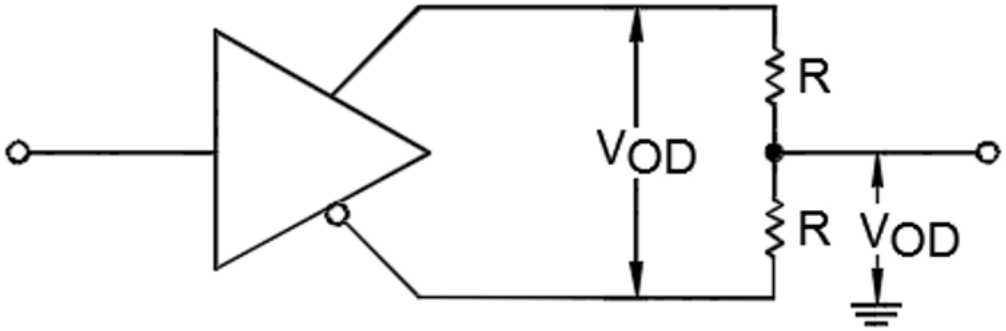


FIGURE 3. Driver voltage measurement.

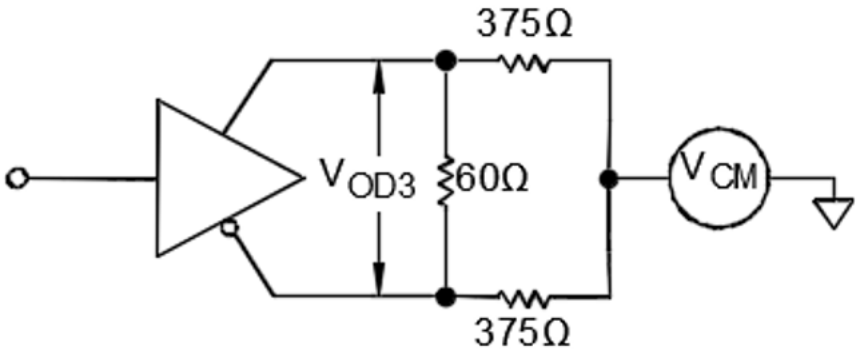
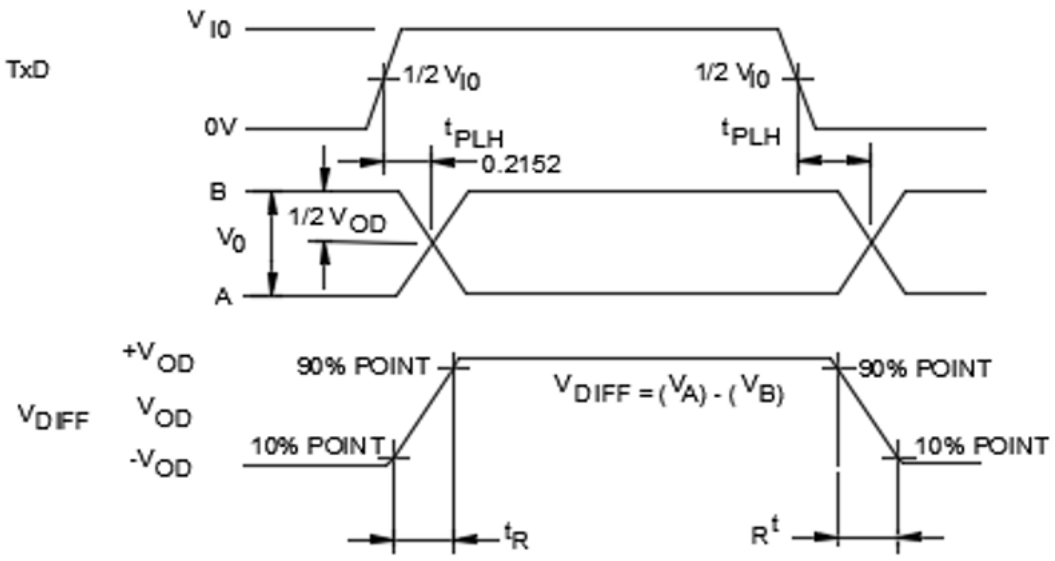


FIGURE 4. Driver voltage measurement over common mode voltage range.



NOTE:

1. V_{OD} is the difference between A and B, with $+V_{OD}$ being the maximum point of V_{OD}, and $–V_{OD}$ being the. minimum point of V_{OD}.

FIGURE 5. Driver propagation delay, rise/fall timing diagram.

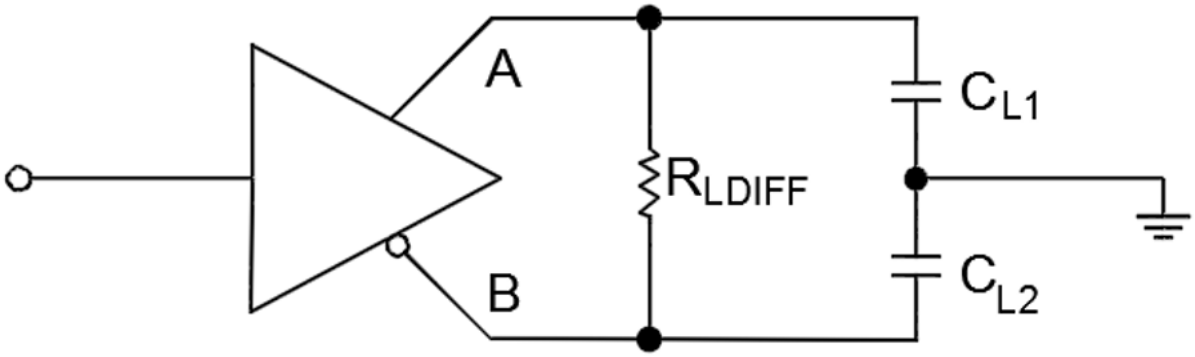


FIGURE 6. Driver propagation delay.

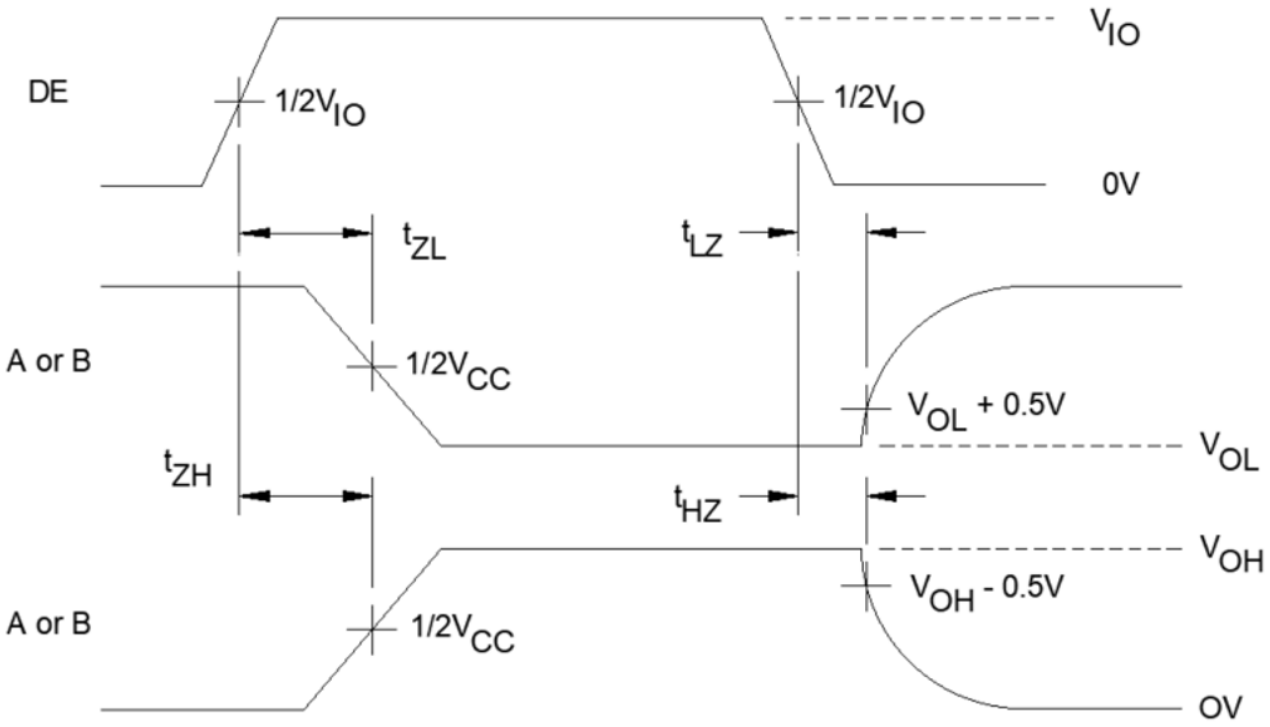


FIGURE 7. Driver enable/disable timing diagram.

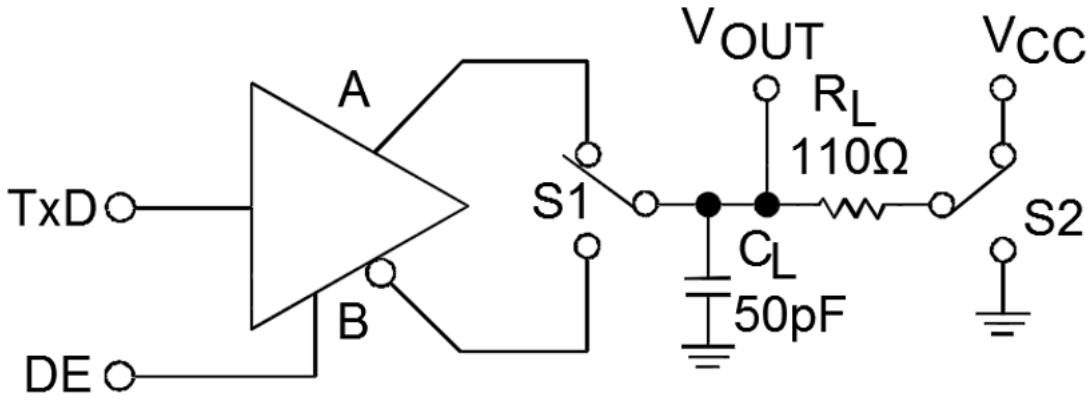


FIGURE 8. Driver enable/disable.

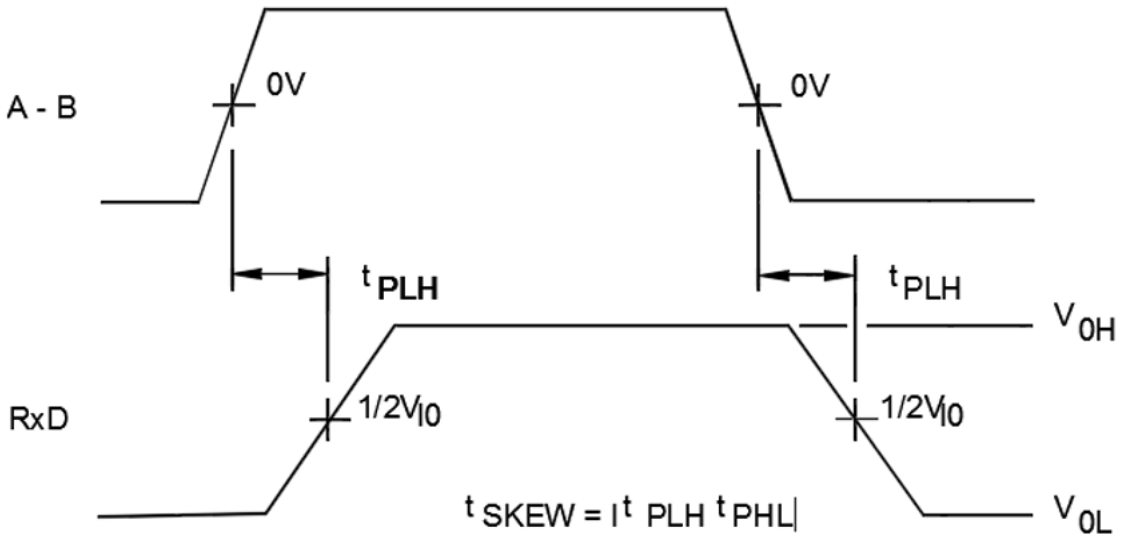


FIGURE 9. Receiver propagation delay timing diagram.

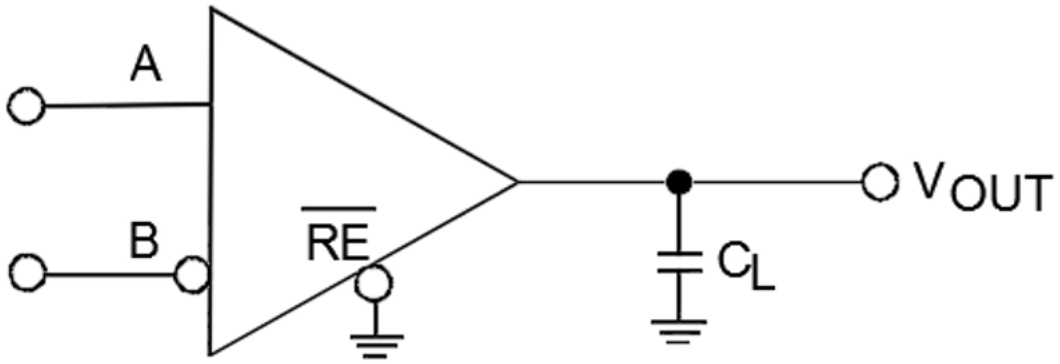


FIGURE 10. Receiver propagation delay.

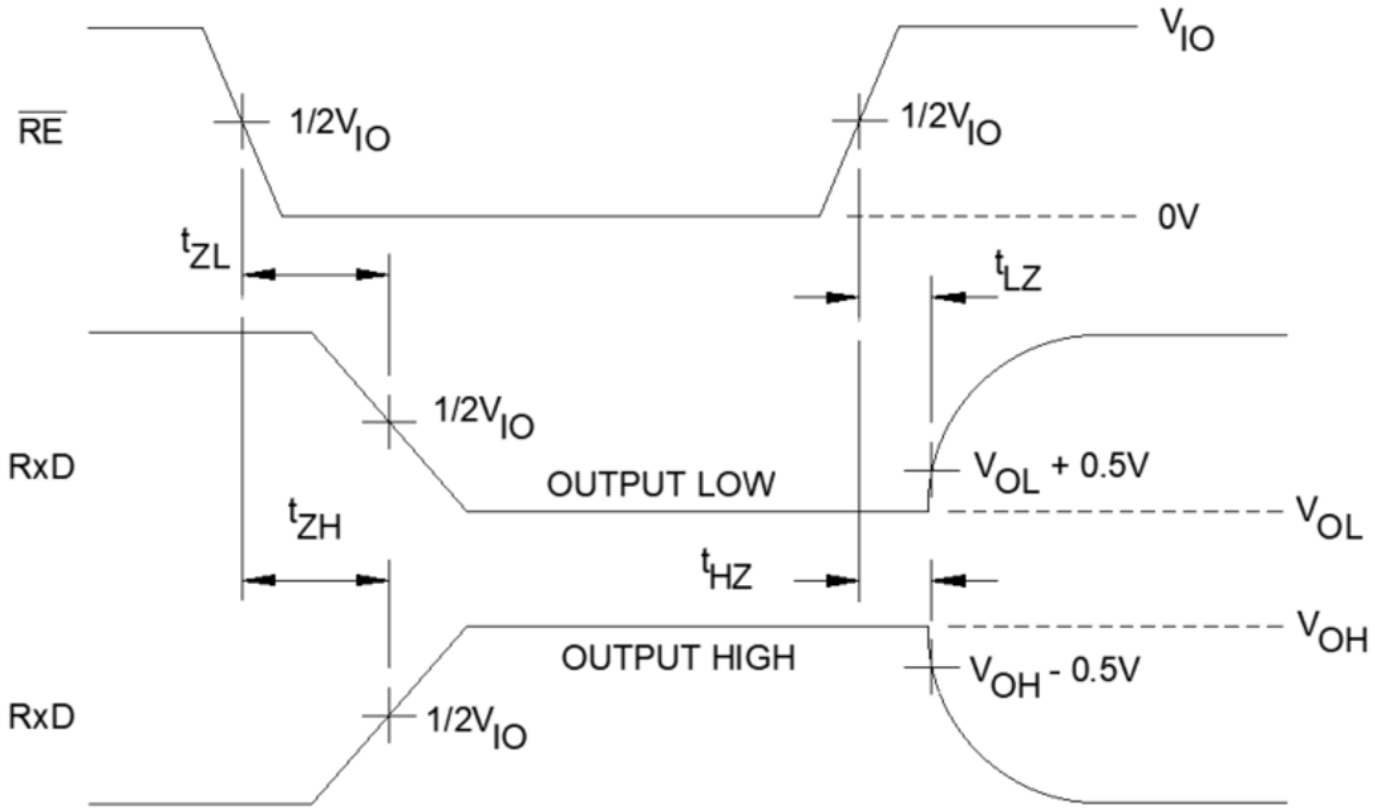


FIGURE 11. Receiver enable/disable timing diagram.

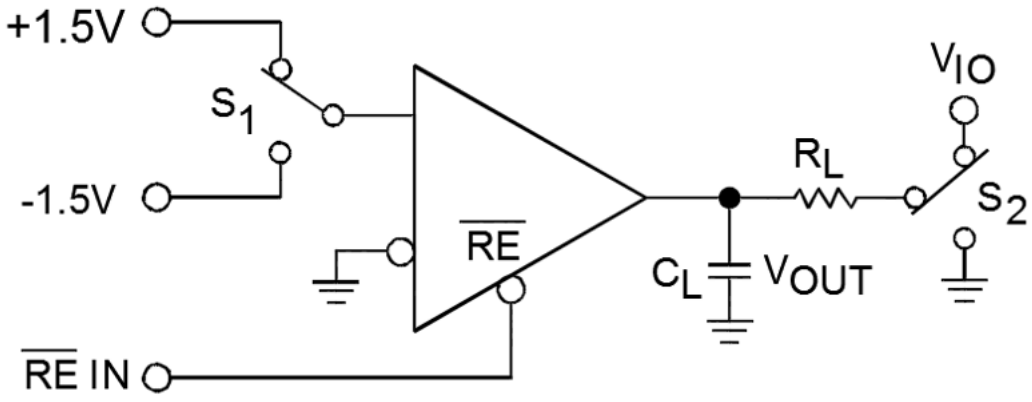


FIGURE 12. Receiver enable/disable.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/17618-01XE	24355	Tube, 48 units	ADM3095E	ADM3095ETRZ-EP
V62/17618-01XE	24355	Reel, 1,000 units	ADM3095E	ADM3095ETRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123