REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Under Table I, $+V_S$ = +5 V, $-V_S$ = 0 V section, make correction to the Gain Error test V_{OUT} limits specified under the condition column. Delete the Coplanarity limits under A1 dimension as specified in Figure 1. Update document paragraphs to current requirements. - ro	22-05-19	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

Original date of drawing
YY-MM-DD
17-05-31

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TITLE
MICROCIRCUIT, LINEAR, JFET INPUT INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL OUTPUT, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/17607
REV A		PAGE 1 OF 19

AMSC N/A

5962-V063-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance junction field effect transistor (JFET) input instrumentation amplifier with rail-to-rail output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD8220-EP	JFET input instrumentation amplifier with rail-to-rail output

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_S)	±18 V
Power dissipation (P_D)	See figure 3
Output short circuit current	Indefinite 2/
Input voltage (common mode)	±V_S
Differential input voltage	±V_S
Storage temperature range (T_{STG})	-65°C to +125°C
Reflow temperature	+260°C
Junction temperature range (T_J)	+140°C
Thermal resistance, junction to ambient (θ_{JA}) (4 layer JEDEC standard board)	189°C/W 3/
Electrical discharge (ESD):	
Human body model (HBM)	7 kV
Charge device model (CDM)	1.25 kV
Machine Model (MM)	0.4 kV

1.4 Recommended operating conditions. 4/

Supply voltage ranges (V_S)	+V_S = +15 V, -V_S = -15 V
	+V_S = +5 V, -V_S = 0 V
Operating temperature range (T_A)	-55°C to +125°C

———

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Assumes the load is referenced to midsupply.

3/ θ_{JA} value is an approximation.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +15 V, $-V_S$ = -15 V, V_{REF} = 0 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Common mode rejection ratio		(CMRR)					
CMRR to DC to 60 Hz with 1 kΩ source imbalance		V_{CM} = ±10 V, G = 1	-55°C to +125°C	01	77		dB
		V_{CM} = ±10 V, G = 10			92		
		V_{CM} = ±10 V, G = 100			92		
		V_{CM} = ±10 V, G = 1000			92		
CMRR at 5 kHz		V_{CM} = ±10 V, G = 1			72		
		V_{CM} = ±10 V, G = 10			80		
		V_{CM} = ±10 V, G = 100			80		
		V_{CM} = ±10 V, G = 1000			80		
Noise		Referred to input (RTI) noise = $\sqrt{(e_{ni}^2 + (e_{no} / G)^2)}$					
Input voltage noise, 1 kHz	e_{ni}	V_{IN+}, V_{IN-} = 0 V	+25°C	01	14 typical		nV / $\sqrt{Hz}$
Output voltage noise, 1 kHz	e_{no}	V_{IN+}, V_{IN-} = 0 V	+25°C	01	90 typical		nV / $\sqrt{Hz}$
Referred to input	RTI	0.1 Hz to 10 Hz, G = 1	+25°C	01	5 typical		µV p-p
		0.1 Hz to 10 Hz, G = 1000			0.8 typical		
Current noise		f = 1 kHz	+25°C	01	1 typical		fA/ $\sqrt{Hz}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +15 V, $-V_S$ = -15 V, V_{REF} = 0 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Voltage offset		$V_{OS} = V_{OSI} + V_{OSO} / G$					
Input offset	V_{OSI}		+25°C	01	-250	+250	µV
Input offset average temperature coefficient	V_{OSI}		-55°C to +125°C	01	-10	+10	µV/°C
Output offset	V_{OSO}		+25°C	01	-750	+750	µV
Output offset average temperature coefficient	V_{OSO}		-55°C to +125°C	01	-10	+10	µV/°C
Offset referred to input (RTI) versus supply (PSR)		V_S = ±5 V to ±15 V, G = 1	-55°C to +125°C	01	80		dB
		V_S = ±5 V to ±15 V, G = 10			92		
		V_S = ±5 V to ±15 V, G = 100			92		
		V_S = ±5 V to ±15 V, G = 1000			92		
Input current							
Input bias current	I_{IB}		+25°C	01		25	pA
			-55°C to +125°C			100	nA
Input offset current	I_{OS}		+25°C	01		2	pA
			-55°C to +125°C			10	nA
Dynamic response							
Small signal bandwidth, -3 dB	SSBW	G = 1	+25°C	01	1500 typical		kHz
		G = 10			800 typical		
		G = 100			120 typical		
		G = 1000			14 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +15 V, $-V_S$ = -15 V, V_{REF} = 0 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic response - con tinued.							
Settling time, 0.01%	t_S	10 V step, G = 1	+25°C	01	5 typical		µs
		10 V step, G = 10			4.3 typical		
		10 V step, G = 100			8.1 typical		
		10 V step, G = 1000			58 typical		
Settling time, 0.001%	t_S	10 V step, G = 1	+25°C	01	6 typical		µs
		10 V step, G = 10			4.6 typical		
		10 V step, G = 100			9.6 typical		
		10 V step, G = 1000			74 typical		
Slew rate	SR	G = 1 to 100	+25°C	01	2		V/µs
Gain		$G = 1 + (49.4\ k\Omega / R_G)$					
Gain range			-55°C to +125°C	01	1	1000	V/V
Gain error		V_{OUT} = ±10 V, G = 1	-55°C to +125°C	01	-0.1	+0.1	%
		V_{OUT} = ±10 V, G = 10			-0.8	+0.8	
		V_{OUT} = ±10 V, G = 100			-0.8	+0.8	
		V_{OUT} = ±10 V, G = 1000			-0.8	+0.8	
Gain nonlinearity		V_{OUT} = -10 V to +10 V, R_L = 10 kΩ, G = 1	+25°C	01		15	ppm
					10 typical		
		V_{OUT} = -10 V to +10 V, R_L = 10 kΩ, G = 10				10	
					5 typical		
		V_{OUT} = -10 V to +10 V, R_L = 10 kΩ, G = 100				60	
					30 typical		
		V_{OUT} = -10 V to +10 V, R_L = 10 kΩ, G = 1000				500	
					400 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +15 V, $-V_S$ = -15 V, V_{REF} = 0 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Gain – continued.							
Gain nonlinearity		V_{OUT} = -10 V to +10 V, R_L = 2 kΩ, G = 1	+25°C	01		15	ppm
					10 typical		
		V_{OUT} = -10 V to +10 V, R_L = 2 kΩ, G = 10				15	
					10 typical		
		V_{OUT} = -10 V to +10 V, R_L = 20 kΩ, G = 100				75	
					50 typical		
Gain versus temperature		G = 1	-55°C to +125°C	01		10	ppm/°C
					3 typical		
		G > 10				-50	
Input							
Impedance 4/ (pin to ground)			+25°C	01	10^4||5 typical		GΩ||pF
Input operating 5/ voltage range		V_S = ±2.25 V to ±18 V for dual supplies	+25°C	01	$-V_S$ – 0.1	$+V_S$ - 2	V
			-55°C to +125°C		$-V_S$ – 0.1	$+V_S$ - 2.2	
Output							
Output swing		R_L = 10 kΩ	+25°C	01	-14.7	+14.7	V
			-55°C to +125°C		-14.3	+14.3	
Short circuit current			+25°C	01	15 typical		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +15 V, $-V_S$ = -15 V, V_{REF} = 0 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference input							
Input resistance	R_{IN}		+25°C	01	40 typical		kΩ
Input current	I_{IN}	V_{IN+}, V_{IN-} = 0 V	+25°C	01		70	µA
Voltage range			+25°C	01		$+V_S$	V
Gain to output			+25°C	01		1 ± 0.0001	V/V
Power supply							
Operating range 6/	V_S	Dual supply	-55°C to +125°C	01	±2.25	±18	V
Quiescent current	I_Q		+25°C	01		750	µA
			-55°C to +125°C			1000	
Temperature range	T_A			01	-55	+125	°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Common mode rejection ratio		(CMRR)					
CMRR to DC to 60 Hz with 1 kΩ source imbalance		V_{CM} = 0 V to 2.5 V, G = 1	-55°C to +125°C	01	77		dB
		V_{CM} = 0 V to 2.5 V, G = 10			92		
		V_{CM} = 0 V to 2.5 V, G = 100			92		
		V_{CM} = 0 V to 2.5 V, G = 1000			92		
CMRR at 5 kHz		V_{CM} = 0 V to 2.5 V, G = 1			72		
		V_{CM} = 0 V to 2.5 V, G = 10			80		
		V_{CM} = 0 V to 2.5 V, G = 100			80		
		V_{CM} = 0 V to 2.5 V, G = 1000			80		
Noise		Referred to input (RTI) noise = $\sqrt{(e_{ni}^2 + (e_{no} / G)^2)}$					
Input voltage noise, 1 kHz	e_{ni}	V_{IN+}, V_{IN-} = 0 V, V_{REF} = 0 V	+25°C	01	14 typical		nV / $\sqrt{Hz}$
Output voltage noise, 1 kHz	e_{no}	V_{IN+}, V_{IN-} = 0 V, V_{REF} = 0 V	+25°C	01	90 typical		nV / $\sqrt{Hz}$
Referred to input	RTI	0.1 Hz to 10 Hz, G = 1	+25°C	01	5 typical		μV p-p
		0.1 Hz to 10 Hz, G = 1000			0.8 typical		
Current noise		f = 1 kHz	+25°C	01	1 typical		fA/ $\sqrt{Hz}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Voltage offset		$V_{OS} = V_{OSI} + V_{OSO} / G$					
Input offset	V_{OSI}		+25°C	01	-300	+300	µV
Input offset average temperature coefficient	V_{OSI}		-55°C to +125°C	01	-10	+10	µV/°C
Output offset	V_{OSO}		+25°C	01	-800	+800	µV
Output offset average temperature coefficient	V_{OSO}		-55°C to +125°C	01	-10	+10	µV/°C
Offset referred to input (RTI) versus supply (PSR)		G = 1	-55°C to +125°C	01	80		dB
		G = 10			92		
		G = 100			92		
		G = 1000			92		
Input current							
Input bias current	I_{IB}		+25°C	01		25	pA
			-55°C to +125°C			100	nA
Input offset current	I_{OS}		+25°C	01		2	pA
			-55°C to +125°C			10	nA
Dynamic response							
Small signal bandwidth, -3 dB	SSBW	G = 1	+25°C	01	1500 typical		kHz
		G = 10			800 typical		
		G = 100			120 typical		
		G = 1000			14 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic response - continued.							
Settling time, 0.01%	t_S	3 V step, G = 1	+25°C	01	2.5 typical		µs
		4 V step, G = 10			2.5 typical		
		4 V step, G = 100			7.5 typical		
		4 V step, G = 1000			30 typical		
Settling time, 0.001%	t_S	3 V step, G = 1	+25°C	01	3.5 typical		µs
		4 V step, G = 10			3.5 typical		
		4 V step, G = 100			8.5 typical		
		4 V step, G = 1000			37 typical		
Slew rate	SR	G = 1 to 100	+25°C	01	2		V/µs
Gain		$G = 1 + (49.4\ k\Omega / R_G)$					
Gain range			-55°C to +125°C	01	1	1000	V/V
Gain error		V_{OUT} = 0.3 V to 2.9 V, G = 1	-55°C to +125°C	01	-0.1	+0.1	%
		V_{OUT} = 0.3 V to 3.8 V, G = 10			-0.8	+0.8	
		V_{OUT} = 0.3 V to 3.8 V , G = 100			-0.8	+0.8	
		V_{OUT} = 0.3 V to 3.8 V , G = 1000			-0.8	+0.8	
Gain nonlinearity		V_{OUT} = 0.3 V to 2.9 V, R_L = 10 kΩ, G = 1	+25°C	01		50	ppm
		V_{OUT} = 0.3 V to 3.8 V, R_L = 10 kΩ, G = 10				50	
		V_{OUT} = 0.3 V to 3.8 V, R_L = 10 kΩ, G = 100				75	
		V_{OUT} = 0.3 V to 3.8 V, R_L = 10 kΩ, G = 1000				750	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Gain – continued.							
Gain nonlinearity		V_{OUT} = 0.3 V to 2.9 V, R_L = 2 kΩ, G = 1	+25°C	01		50	ppm
		V_{OUT} = 0.3 V to 3.8 V, R_L = 2 kΩ, G = 10				50	
		V_{OUT} = 0.3 V to 3.8 V, R_L = 20 kΩ, G = 100				75	
Gain versus temperature		G = 1	-55°C to +125°C	01	3 typical		ppm/°C
						10	
		G > 10				-50	
Input							
Impedance 4/ (pin to ground)			+25°C	01	10^4||6 typical		GΩ||pF
Input voltage range			-55°C to +125°C		– 0.1	$+V_S$ - 2.2	V
Output							
Output swing		R_L = 10 kΩ	+25°C	01	0.15	4.85	V
			-55°C to +125°C		0.3	4.70	
Short circuit current			+25°C	01	15 typical		mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ $+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference input							
Input resistance	R_{IN}		+25°C	01	40 typical		kΩ
Input current	I_{IN}	V_{IN+}, V_{IN-} = 0 V	+25°C	01		70	μA
Voltage range			+25°C	01	$-V_S$	$+V_S$	V
Gain to output			+25°C	01	1 ± 0.0001 typical		V/V
Power supply							
Operating range	V_S	Single supply	-55°C to +125°C	01	4.5	36	V
Quiescent current	I_Q		+25°C	01		750	μA
			-55°C to +125°C			1000	
Temperature range	T_A			01	-55	+125	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, G = 1 and R_L = 2 kΩ 3/.

3/ When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.

4/ Differential and common mode input impedance (Z_{DIFF} and Z_{CM}) can be calculated from the pin impedance (Z_{PIN}) : $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.

5/ The device can operate up to a diode drop below the negative supply but, the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current within the specification.

6/ At the minimum supply voltage of ±2.25 V, ensure that the common mode voltage is within the input voltage range specification.

Case X

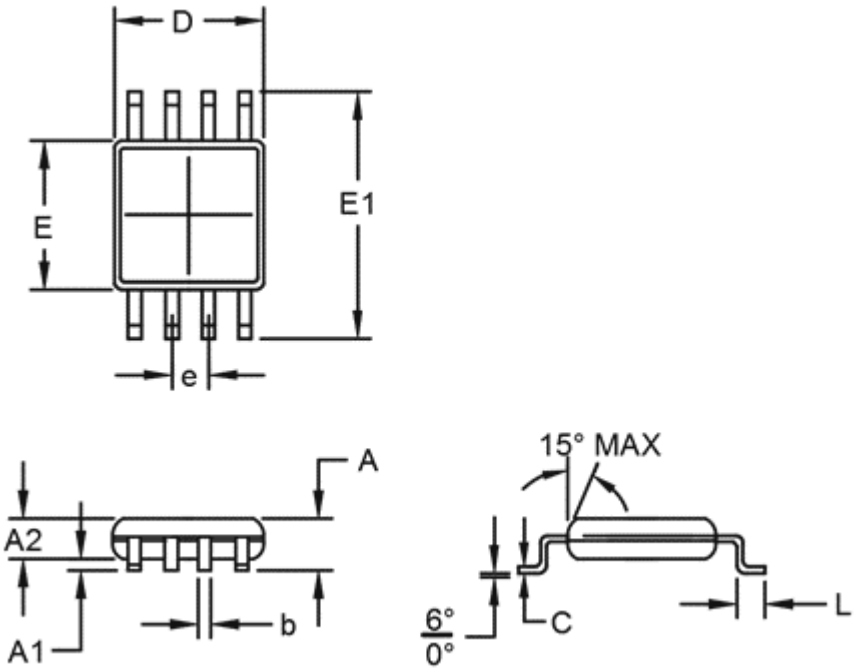


FIGURE 1. Case outline.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.0433	---	---	1.10
A1	.0019	---	.0059	0.05	---	0.15
A2	.0295	.0334	.0374	0.75	0.85	0.95
b	.0098	---	.0157	0.25	---	0.40
c	.0035	---	.0090	0.09	---	0.23
D	.1102	.1181	.1259	2.80	3.00	3.20
e	.0255 BSC			0.65 BSC		
E	.1102	.1181	.1259	2.80	3.00	3.20
E1	.1830	.1929	.2027	4.65	4.90	5.15
L	.0157	.0216	.0314	0.40	0.55	0.80

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	-IN	Negative input terminal (true differential input).
2	R_G	Gain setting terminals. Place a resistor across the RG pins.
3	R_G	Gain setting terminals. Place a resistor across the RG pins.
4	+IN	Positive input terminal (true differential input).
5	$-V_S$	Negative power supply terminal.
6	REF	Reference voltage terminal. Drive this terminal with low impedance voltage source to level shift the output.
7	V_{OUT}	Output terminal.
8	$+V_S$	Positive power supply terminal.

FIGURE 2. Terminal connections.

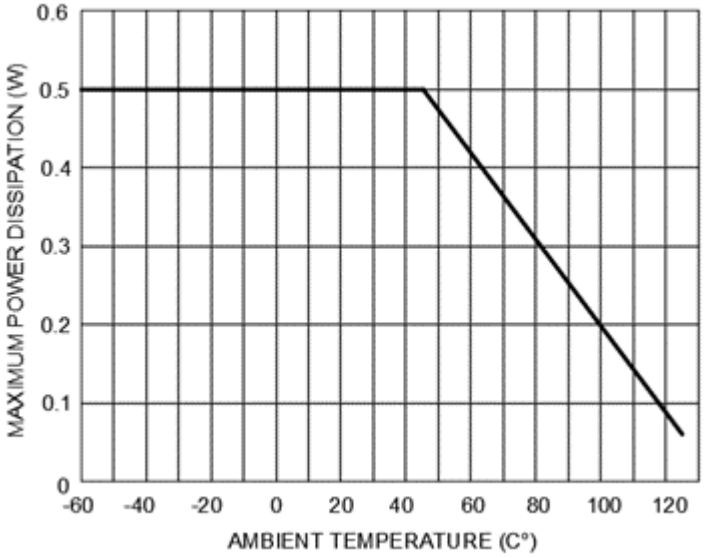


Figure 3. Maximum power dissipation versus ambient temperature.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/17607-01XE	24355	Tube, 50 units	Y6T	AD8220TRMZ-EP
V62/17607-01XE	24355	Reel, 1000 units	Y6T	AD8220TRMZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123