REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to footnotes 5/, 12/ and delete footnotes 18/ and 21/ due to repetition with footnote 4/ as specified under Table I. Delete the numerical limits from Figure 1 case outline and replace with assigned letter symbols. Add dimensions table under figure 1. Make corrections to V_{LOGIC}, $\overline{RESET}$, and RSTSEL pin descriptions as specified in figure 3. Update document paragraphs to current requirements. - ro	22-04-07	J. Eschmeyer

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

Original date of drawing
YY-MM-DD
17-01-09

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, LINEAR, QUAD, 16-BIT NANODAC+ WITH 4 ppm/°C REFERENCE, SPI INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/14635
REV A		PAGE 1 OF 19

AMSC N/A

5962-V044-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad, 16-Bit nano digital to analog converter (DAC+) with 4 ppm/°C reference, serial peripheral interface (SPI) interface microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14635	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5686R –EP	Quad, 16-Bit nano DAC+ with 4 ppm/°C reference, SPI interface

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-220-WEED-6	Lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +7 V
V_{LOGIC} to GND	-0.3 V to +7 V
V_{OUT} to GND	-0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	-0.3 V to V_{DD} + 0.3 V
Digital input voltage to GND	-0.3 V to V_{LOGIC} + 0.3 V
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Junction temperature	135°C
Case outline X, θ_{JA} thermal Impedance, 0 airflow (4-layer board)	70°C/W
Reflow soldering peak temperature, lead (Pb) free (J-STD-020)	260°C
Electrostatic discharge sensitivity (ESDS):	
Human body model (HBM)	4 kV
Field induced charged device model (FICDM)	1.25 kV

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC J STD-020	–	Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Serial write operation. The serial write operation shall be as shown in figure 5.

3.5.6 Load circuit for digital output (SDO) timing specification. The load circuit for digital output (SDO) timing specification shall be as shown in figure 6.

3.5.7 Daisy-chain timing diagram. The daisy-chain timing diagram shall be as shown in figure 7.

3.5.8 Readback timing diagram. The readback timing diagram shall be as shown in figure 8.

3.5.9 Headroom/footroom versus load current. The Headroom/footroom versus load current shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Static performance 3/					
Resolution		16			Bits
Relative accuracy	Gain = 2		±1	±4	LSB
	Gain = 1		±1	±5	LSB
Differential nonlinearity (DNL)	Guaranteed monotonic by design			±1	LSB
Zero-code error	All zeros loaded to DAC register		0.4	1.5	mV
Offset error			±0.1	±0.5	mV
Full-scale error	All ones loaded to DAC register		+0.01	+0.1	% of FSR
Gain error	Gain = 2		±0.02	±0.1	% of FSR
	Gain = 1		±0.02	±0.15	% of FSR
Total unadjusted error	External reference; gain = 2		±0.01	±0.1	% of FSR
	Internal reference; gain = 1			±0.2	% of FSR
Offset error drift 4/			±1		µV/°C
Gain temperature coefficient (TC) 4/	Of FSR/°C		±1		ppm
DC power supply rejection ratio 4/	DAC code = midscale, V_{DD} = 5 V ± 10%		0.15		mV/V
DC crosstalk	Due to single channel, full-scale output change		±2		µV
	Due to load current change		±3		µV/mA
	Due to powering down (per channel)		±2		µV
Output characteristics 4/					
Output voltage range	Gain = 1	0		V_{REF}	V
	Gain = 2, see Figure 9	0		2 × V_{REF}	V
Capacitive load stability	RL = ∞		2		nF
	RL = 1 kΩ		10		nF
Resistive load 5/		1			kΩ
Load regulation	5 V ± 10%, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ 30 mA		80		µV/mA
	3 V ± 10%, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ 20 mA		80		µV/mA
Short-circuit current 6/			40		mA
Load impedance at rails 7/	See Figure 9		25		Ω
Power-up time	Coming out of power-down mode; V_{DD} = 5 V		2.5		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Reference output.					
Output voltage 8/	At ambient	2.4975		2.5025	V
Reference TC 9/ 10/			4	13	ppm/°C
Output impedance 4/			0.04		Ω
Output voltage noise 4/	0.1 Hz to 10 Hz		12		µV p-p
Output voltage noise density	At ambient; f = 10 kHz, C_L = 10 nF		240		nV/√Hz
Load regulation sourcing 4/	At ambient		20		µV/mA
Load regulation sinking 4/	At ambient		40		µV/mA
Output current load capability	V_{DD} ≥ 3 V		±5		mA
Line regulation	At ambient		100		µV/V
Thermal hysteresis 4/	First cycle		125		ppm
	Additional cycles		25		ppm
Logic inputs 4/					
Input current	Per pin			±2	µA
Input voltage, low (V_{IN})				0.3 × V_{LOGIC}	V
Input voltage, high (V_{INH})		0.7 × V_{LOGIC}			V
Pin capacitance			2		pF
Logic outputs (SDO) 4/					
Output voltage, low (V_{OL})	I_{SINK} = 200 µA			0.4	V
Output voltage, high (V_{OH})	I_{SOURCE} = 200 µA	V_{LOGIC} − 0.4			V
Floating state output capacitance			4		pF
Power requirements					
V_{LOGIC}		1.62		5.5	V
I_{LOGIC}				3	µA
V_{DD}	Gain = 1	2.7		5.5	V
V_{DD}	Gain = 2	V_{REF} + 1.5		5.5	V
I_{DD}	V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V				
Normal mode 11/	Internal reference off		0.59	0.7	mA
	Internal reference on, at full scale		1.1	1.3	mA
All power-down modes 12/	−40°C to +85°C		1	4	µA
	−55°C to +125°C			6	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
AC characteristics 13/ 14/ 15/					
Output voltage settling time	¼ to ¾ scale settling to ±2 LSB		5	8	µs
Slew rate			0.8		V/µs
Digital-to-analog glitch impulse	1 LSB change around major carry		0.5		nV-sec
Digital feedthrough			0.13		nV-sec
Digital crosstalk			0.1		nV-sec
Analog crosstalk			0.2		nV-sec
DAC-to-DAC crosstalk			0.3		nV-sec
Total harmonic distortion (THD) 16/	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		-80		dB
Output noise spectral density (NSD)	DAC code = midscale, 10 kHz; gain = 2		300		$nV/\sqrt{Hz}$
Output noise	0.1 Hz to 10 Hz		6		µV p-p
Signal-to-noise ratio (SNR)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		90		dB
Spurious free dynamic range (SFDR)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		83		dB
Signal-to-noise-and-distortion ratio (SINAD)	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		80		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits				Unit
			1.62 V ≤ V_{LOGIC} ≤ 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
			Min	Max	Min	Max	
Timing characteristics 4/ 17/		(See Figure 5)					
SCLK cycle time	t_1		20		20		ns
SCLK high time	t_2		10		10		ns
SCLK low time	t_3		10		10		ns
$\overline{SYNC}$ to SCLK falling edge setup time	t_4		15		10		ns
Data setup time	t_5		5		5		ns
Data hold time	t_6		5		5		ns
SCLK falling edge to $\overline{SYNC}$ rising edge	t_7		10		10		ns
Minimum $\overline{SYNC}$ high time	t_8		20		20		ns
$\overline{SYNC}$ rising edge to $\overline{SYNC}$ rising edge (DAC register update/s)	t_9		870		830		ns
$\overline{SYNC}$ falling edge to SCLK fall ignore	t_{10}		16		10		ns
$\overline{LDAC}$ pulse width low	t_{11}		15		15		ns
$\overline{SYNC}$ rising edge to $\overline{LDAC}$ rising edge	t_{12}		20		20		ns
$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge	t_{13}		30		30		ns
$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge	t_{14}		840		800		ns
Minimum pulse width low	t_{15}		30		30		ns
Pulse activation time	t_{16}		30		30		ns
Power-up time 18/			4.5		4.5		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits				Unit
			1.62 V ≤ V_{LOGIC} ≤ 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
			Min	Max	Min	Max	
Daisy-chain and readback timing characteristics	4/ 19/		(See Figures 6-8)				
SCLK cycle time	t_1		66		40		ns
SCLK high time	t_2		33		20		ns
SCLK low time	t_3		33		20		ns
$\overline{SYNC}$ to SCLK falling edge	t_4		33		20		ns
Data setup time	t_5		5		5		ns
Data hold time	t_6		5		5		ns
SCLK falling edge to $\overline{SYNC}$ rising edge	t_7		15		10		ns
Minimum $\overline{SYNC}$ high time	t_8		60		30		ns
SDO data valid from SCLK rising edge	t_9			45		30	ns
$\overline{SYNC}$ rising edge to SCLK rising edge	t_{10}		15		10		ns
$\overline{SYNC}$ rising edge to SDO disable	t_{11}		60		60		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.7 V to 5.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. R_L = 2 kΩ; C_L = 200 pF.

3/ DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when V_{REF} = V_{DD} with gain = 1 or when $V_{REF}/2$ = V_{DD} with gain = 2. Linearity is calculated using a reduced code range of 256 to 65,280.

4/ Guaranteed by design, not subject to production test.

5/ Channel A and Channel B can have a combined output current of up to 15 mA. Similarly, Channel C and Channel D can have a combined output current of up to 15 mA, up to a junction temperature of 135°C.

6/ V_{DD} = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature may be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.

7/ When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 25 Ω typical channel resistance of the output device. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 9).

8/ Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See manufacturer data sheet for more information.

9/ Reference is trimmed and tested at two temperatures and is characterized from −55°C to +125°C.

10/ Reference temperature coefficient is calculated as per the box method. See manufacturer data sheet for more information.

11/ Interface inactive. Both DACs active. DAC outputs unloaded.

12/ All DACs powered down.

13/ V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization; not production tested.

14/ Temperature range is −55°C to +125°C, typical at 25°C.

15/ See manufacturer data sheet.

16/ Digitally generated sine wave at 1 kHz.

17/ All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 5. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

18/ Time to exit power-down to normal mode of device operation, $\overline{SYNC}$ clock edge to 90% of DAC midscale value, with output unloaded.

19/ All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 7 and Figure 8. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. V_{DD} = 2.7 V to 5.5 V.

Case X

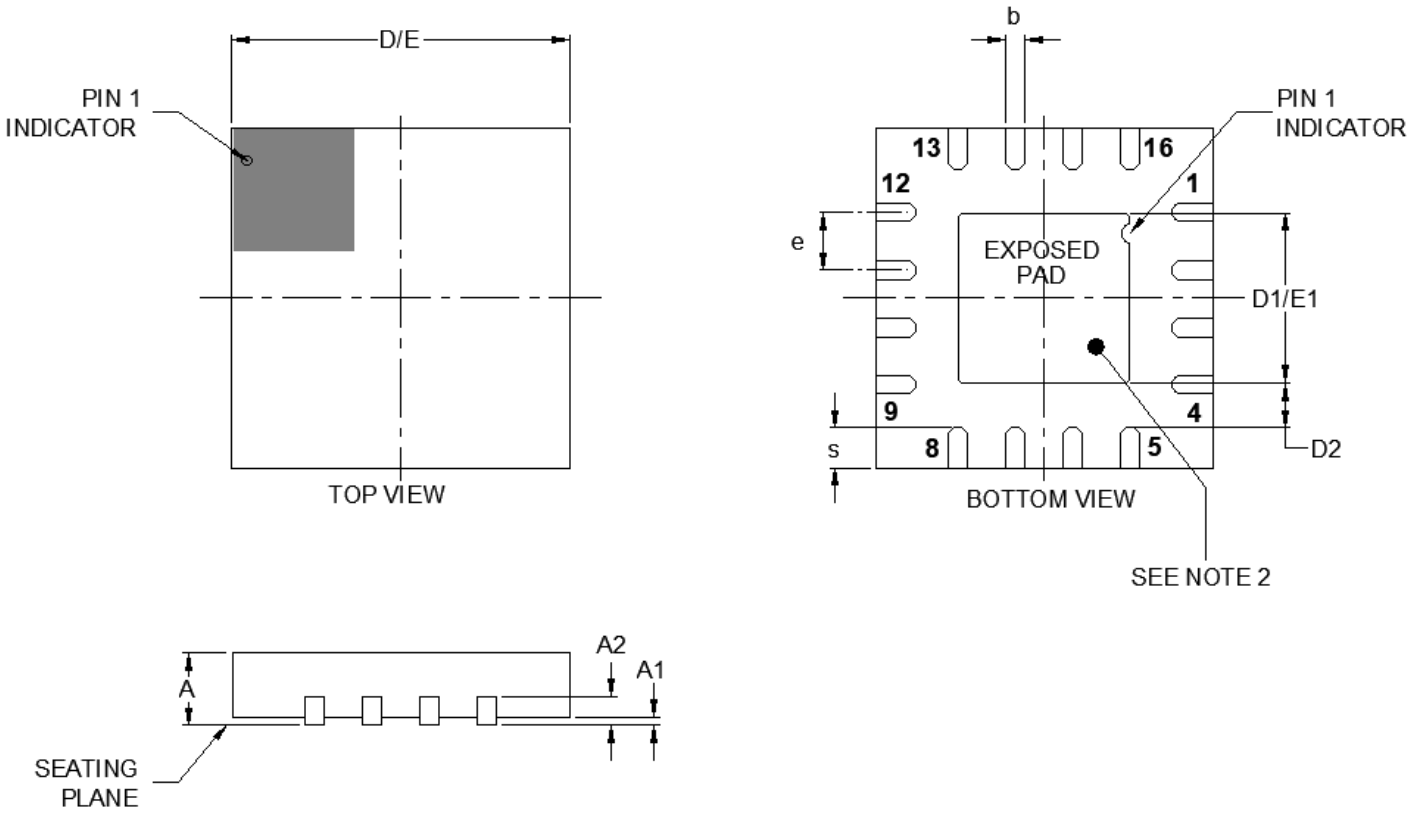


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/14635
		REV A	PAGE 11

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.029	.031	0.70	0.75	0.80
A1	---	.001	.002		0.02	0.05
A2	.008 REF			0.20 REF		
b	.007	.009	.012	0.18	0.23	0.30
D/E	.114	.118	.122	2.90	3.00	3.10
D1/E1	.057	.063	.069	1.45	1.60	1.75
D2	.010	---	---	0.25	---	---
e	.020 BSC			0.50 BSC		
s	.012	.016	.020	0.30	0.40	0.50

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's data sheet.
3. Falls within reference to JEDEC MO-220-WEED-6.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$V_{OUT}A$
2	GND
3	V_{DD}
4	$V_{OUT}C$
5	$V_{OUT}D$
6	SDO
7	$\overline{LDAC}$
8	GAIN
9	V_{LOGIC}
10	SCLK
11	$\overline{SYNC}$
12	SDIN
13	$\overline{RESET}$
14	RSTSEL
15	V_{REF}
16	$V_{OUT}B$

NOTES:
1. The exposed PAD must be tied to GND.
2. NC = No Connect. Do not Connect to this PIN.

FIGURE 2. Terminal connections.

Terminal Number	Terminal Symbol	Description
1	$V_{OUT}A$	Analog output voltage from DAC A. The output amplifier has rail-to-rail operation.
2	GND	Ground reference point for all circuitry on the device.
3	V_{DD}	Power supply input. The device can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{OUT}C$	Analog output voltage from DAC C. The output amplifier has rail-to-rail operation.
5	$V_{OUT}D$	Analog output voltage from DAC D. The output amplifier has rail-to-rail operation.
6	SDO	Serial data output. SDO can be used to daisy-chain a number of devices together, or it can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
7	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
8	GAIN	Span set pin. When this pin is tied to GND, all four DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all four DACs output a span of 0 V to 2 × V_{REF}.
9	V_{LOGIC}	Digital power supply. Voltage ranges from 1.62 V to 5.5 V.
10	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
11	$\overline{\text{SYNC}}$	Active low control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 24 clocks.
12	SDIN	Serial data input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	$\overline{\text{RESET}}$	Asynchronous reset input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. If this pin is forced low at power up, the power on reset (POR) circuit will not initialize the device correctly until this pin is released.
14	RSTSEL	Power-on reset select. Tying this pin to GND powers up all four DACs to zero scale. Tying this pin to V_{LOGIC} powers up all four DACs to midscale.
15	V_{REF}	Reference voltage. The device has a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	$V_{OUT}B$	Analog output voltage from DAC B. The output amplifier has rail-to-rail operation.
17	EPAD	Exposed pad. The exposed pad must be tied to GND.

FIGURE 3. Terminal function.

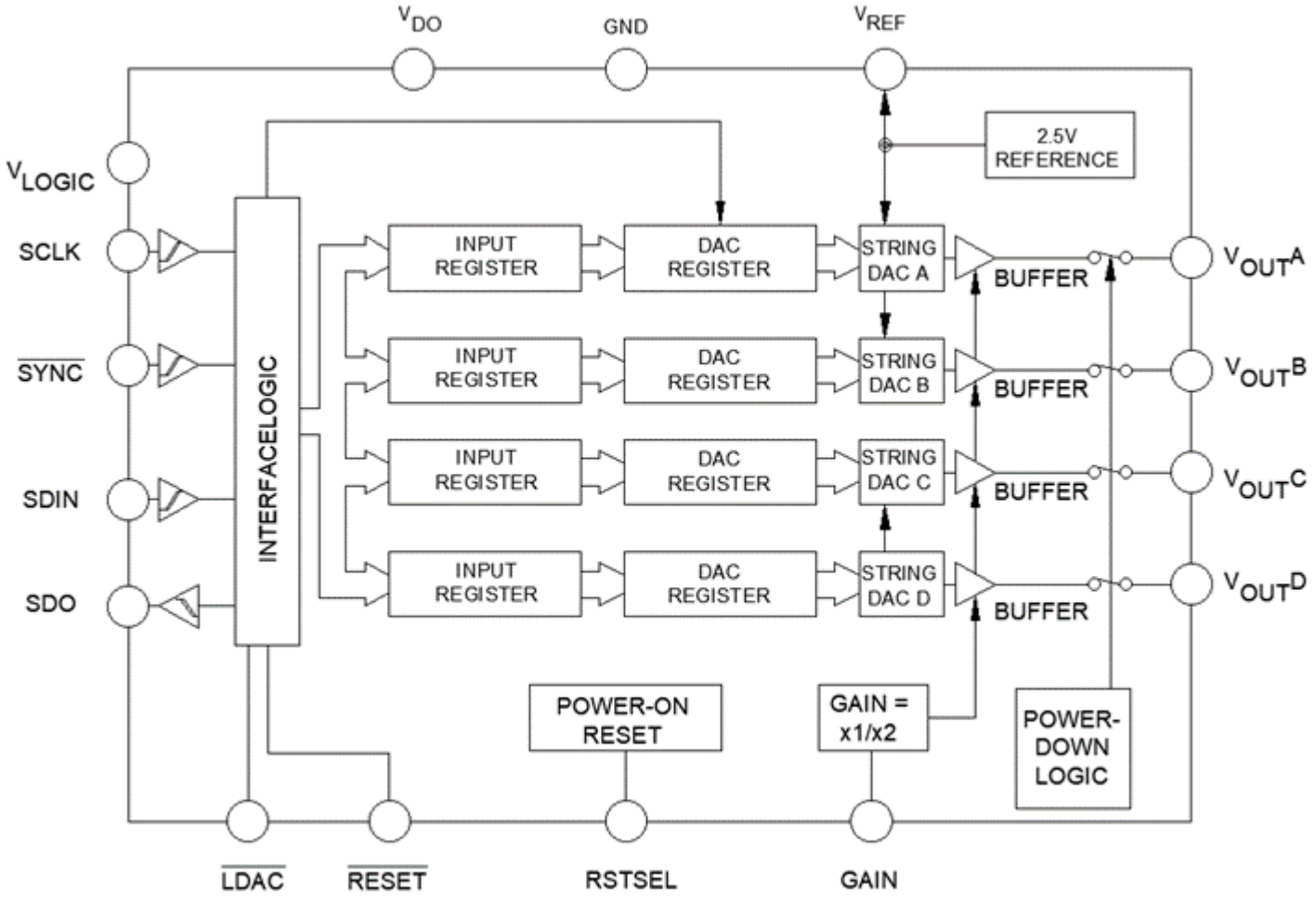
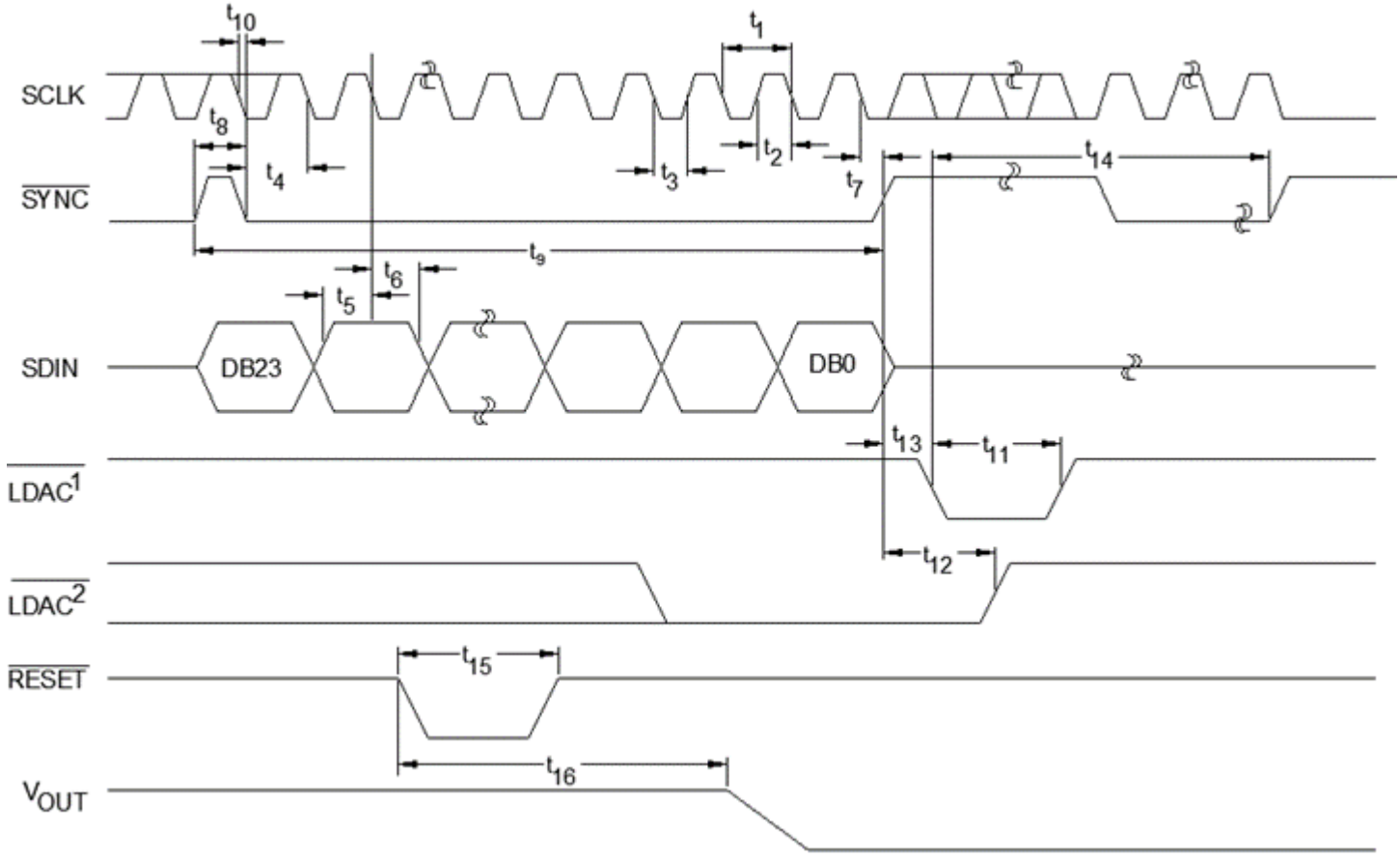


FIGURE 4. Functional block diagram.



1 ASYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.
2 SYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE

FIGURE 5. Serial Write Operation.

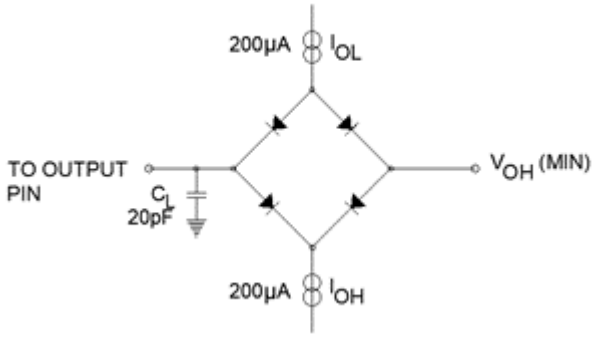


FIGURE 6. Load Circuit for Digital Output (SDO) Timing Specifications.

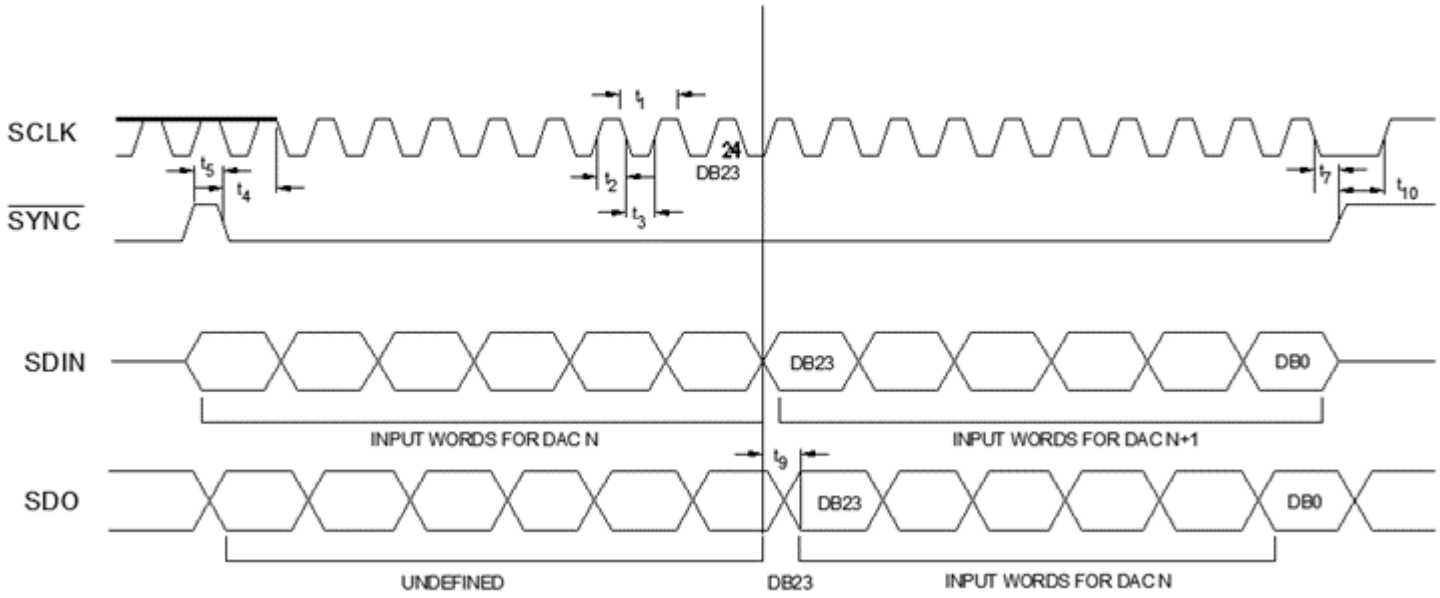


FIGURE 7. Daisy-Chain Timing Diagram.

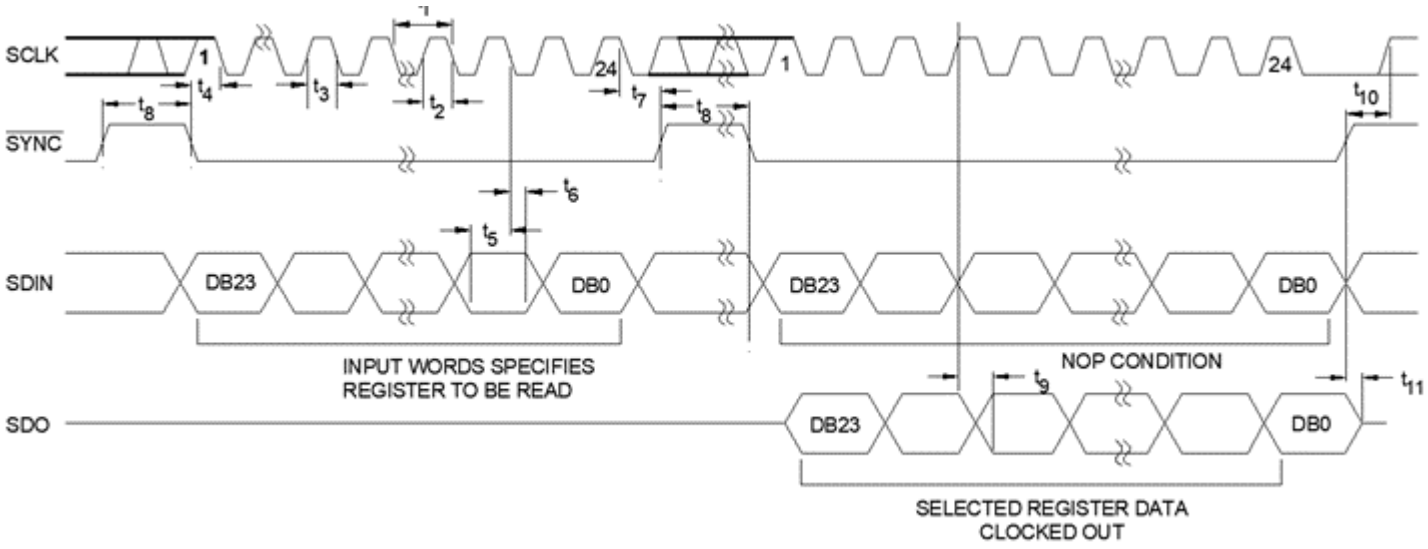


FIGURE 8. Readback Timing Diagram.

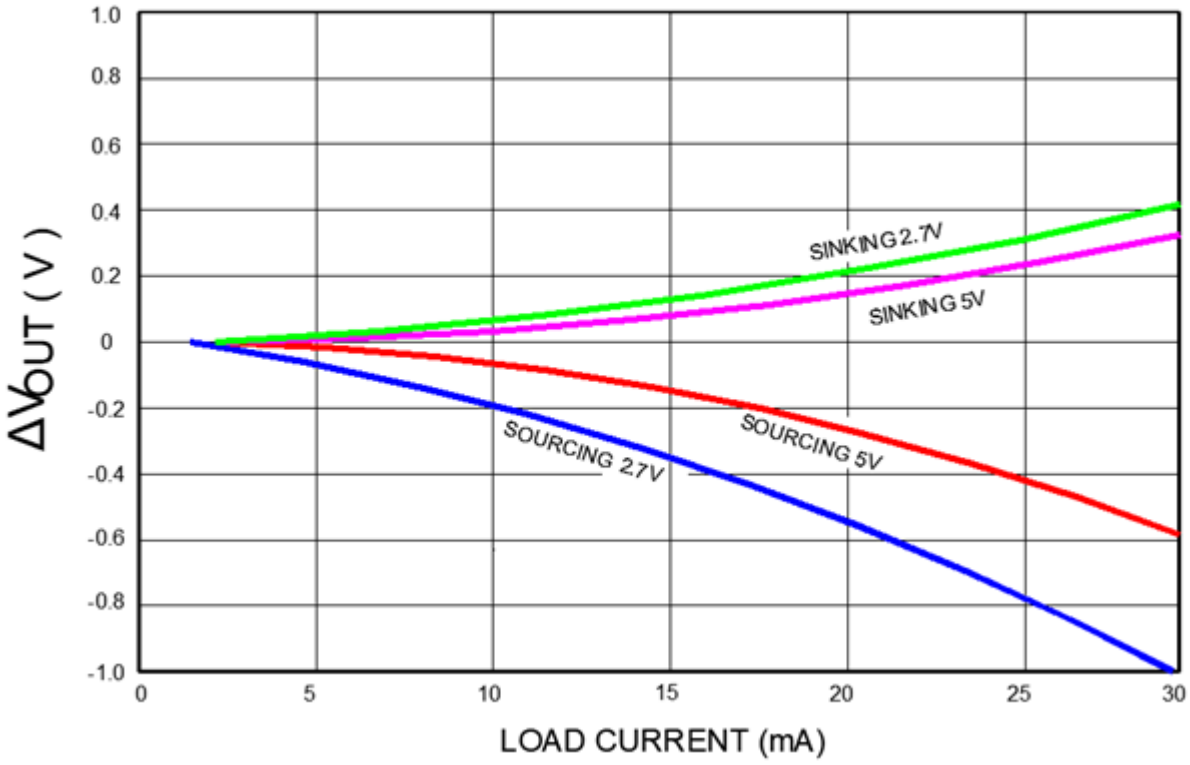


FIGURE 9. Headroom/footroom versus load current.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/14635-01XE	24355	Tape and reel, 1500 units	AD5686RTCPZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying he item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123