

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make following changes to figure 2; ISET and ISHARE descriptions, delete output current limit of 108 μ A and substitute 123 μ A ; VOUT description, delete output voltage limit of 6 V and substitute 7.5 V. Under figure 5, add voltages 6.5 V and 7.5 V. - ro	10-11-23	C. SAFFLE
B	Add device type 02. Split out the input voltage range limits PVIN and VIN under paragraph 1.4. Make following changes to device type 01 parameters; driver bias voltage (delete 3 V and substitute 4.5 V) and signal bias voltage (delete 3 V and substitute 4.5 V) under paragraph 1.3; maximum current (delete 250 mA and substitute 320 mA), maximum current (delete 150 mA entirely), output ripple voltage (delete 30 mVpp and substitute 27 mVpp) under table I; FF (delete 0.7 V and substitute 0.8 V), PVCC (delete 5.5 V and substitute 5.6 V), PVIN (delete 0 V and substitute 3 V), and VCC (delete 2.97 V and substitute 4.5 V) descriptions under figure 2. - ro	12-11-14	C. SAFFLE
C	Update document paragraphs to current requirements. - ro	25-03-20	J. ESCHMEYER



**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		

PMIC N/A Original date of drawing 10-07-15	PREPARED BY RICK OFFICER		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
	CHECKED BY RAJESH PITHADIA		TITLE MICROCIRCUIT, LINEAR, CURRENT SHARING 10 A DC/DC POWER SUPPLY, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE			
	SIZE A	CAGE CODE 16236	DWG NO. V62/10608	
	REV C		PAGE 1 OF 18	

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a current sharing 10 amp (A) DC/DC power supply microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/10608</u>	-	<u>01</u>	<u>X</u>	<u>B</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device types.

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISL8200M	Current sharing 10 A DC/DC power supply
02	ISL8200AM	Current sharing 10 A DC/DC power supply

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	23	See figure 1	Plastic quad leadless flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 2

1.3 Absolute maximum ratings. 1/

Input voltage range PVIN (VIN)	-0.3 V to +27 V
Driver bias voltage, PVCC:	
Device type 01	-0.3 V to +6.5 V
Device type 02	-0.3 V to +6.0 V
Signal bias voltage, VCC	-0.3 V to +6.5 V
BOOT/UGATE voltage, VBOOT	-0.3 V to +36 V
Phase voltage, (VPHASE)	[VBOOT – 7] V to [VBOOT + 0.3] V
BOOT to PHASE voltage (VBOOT - VPHASE)	-0.3 V to [VCC + 0.3] V
Input, output or I/O voltage	-0.3 V to [VCC + 0.3] V
Electrostatic discharge (ESD):	
Human body model (HBM) (tested per JESD22-A114)	2 kV
Machine model (MM) (tested per JESD22-A115)	200 V
Charge device model (CDM) (tested per JESD22-C101)	1 kV
Latch up current (tested per JESD-78, class 2, level A)	100 mA
Power dissipation (PD)	3.2 W 2/
Maximum storage temperature range (TSTG)	-55°C to +150°C
Thermal resistance, junction to case (θJC)	2°C/W 3/
Thermal resistance, junction to ambient (θJA)	13°C/W 4/

1.4 Recommended operating conditions. 5/ 6/

Input voltage range :	
PVIN	3 V to +20 V 7/
VIN	4.5 V to +20 V 7/
Driver bias voltage, PVCC	4.5 V to +5.6 V 7/
Signal bias voltage, VCC	4.5 V to +5.6 V
BOOT to PHASE voltage (overcharged) (VBOOT - VPHASE)	< 6 V
Junction temperature range (TJ)	-55°C to +125°C
Operating ambient temperature range (TA)	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ $P_{VIN} = V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 10\text{ A}$.
- 3/ θJC case temperature location is the center of the package underside.
- 4/ θJA is measured in free air with the component mounted on a high effective thermal conductivity test board (for example, 4 layer type without thermal vias, see manufacturer’s technical brief TB379) per JEDEC standards except that the top and bottom layers assume solid planes.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 6/ The sequence to start up at < - 30°C is to hold EN pin to ground and release it after PVIN and VIN voltage has reached steady state. Utilizing multiple modules to current share below -40°C ambient is not recommended. However, the operation of a single module is acceptable.
- 7/ For 3.3 V PVIN operation, the voltage on PVCC is recommended to be 5 V for sufficient gate drive voltage. This can be accomplished by using a voltage greater than or equal to 5 V on VIN, or directly connect the 5 V source to both VIN and PVCC.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices
JESD78	-	IC Latch-Up test
JESD22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	-	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
JESD22-A115	-	Electrostatic Discharge Sensitivity Testing Machine Model (MM)

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
VCC SUPPLY CURRENT SECTION.							
Nominal supply V _{IN} current	I _{Q_VIN}	PV _{IN} = V _{IN} = 20 V, no load, F _{SW} = 700 kHz	+25°C	01, 02	36 typical		mA
		PV _{IN} = V _{IN} = 4.5 V, no load, F _{SW} = 700 kHz	+25°C		27 typical		
Shutdown supply V _{CC} current	I _{VCC}	EN = 0 V, V _{CC} = 2.97 V	+25°C	01, 02	9 typical		mA
INTERNAL LINEAR REGULATOR SECTION.							
Maximum current	I _{PVCC}	PV _{CC} = 4 V to 5.6 V	+25°C	01, 02	320 typical		mA
Saturated equivalent impedance	R _{LDO}	P-channel MOSFET (V _{IN} = 5 V)	+25°C	01, 02	1 typical		Ω
POWER ON RESET SECTION. <u>3/</u>							
Rising V _{CC} threshold			-55°C to +125°C	01, 02		2.98	V
Falling V _{CC} threshold			-55°C to +125°C	01, 02		2.75	V
Rising PV _{CC} threshold			-55°C to +125°C	01		3.05	V
				02		2.98	
Falling PV _{CC} threshold			-55°C to +125°C	01, 02		2.75	V
System soft start delay	t _{SS_DLY}	After PLL, V _{CC} , and PV _{CC} PORs, and EN above their threshold	+25°C	01, 02	384 typical		cycles
ENABLE SECTION. <u>3/</u>							
Turn on threshold voltage			-55°C to +125°C	01, 02	0.75	0.86	V
Hysteresis sink current	I _{EN_HYS}		-55°C to +125°C	01	21	35	μA
				02	19	35	
Undervoltage lockout hysteresis	V _{EN_HYS}	V _{EN_RTH} = 10.6 V, V _{EN_FTH} = 9 V, R _{UP} = 53.6 kΩ, R _{DOWN} = 5.23 kΩ,	+25°C	01, 02	1.6 typical		V
Sink current	I _{EN_SINK}	V _{EN} = 1 V	-55°C to +125°C	01, 02	10		mA
Sink impedance	R _{EN_SINK}	V _{EN} = 1 V	-55°C to +125°C	01, 02		64	Ω

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
OSCILLATOR SECTION.							
Oscillator frequency	FOSC	R _{FS} = 59 kΩ, see figure 3	+25°C	01, 02	700 typical		kHz
Total variation <u>3/</u>		V _{CC} = 5 V	-55°C to +125°C	01, 02	-12	+12	%
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP (PLL) SECTION. <u>3/</u>							
Synchronization frequency		V _{CC} = 5.4 V	-55°C to +125°C	01, 02	FOSC	1500	kHz
Input signal duty <u>4/</u> cycle range			-55°C to +125°C	01, 02	10	90	%
PULSE WIDTH MODULATION (PWM) SECTION. <u>3/</u>							
Minimum PWM off time	t _{MIN_OFF}		-55°C to +125°C	01, 02	310	425	ns
Current sampling blanking time	t _{BLANKING}		+25°C	01, 02	175 typical		ns
OUTPUT CHARACTERISTICS SECTION.							
Output continuous current range	I _{OUT(DC)}	P _{VIN} = V _{IN} = 12 V, V _{OUT} = 1.2 V, see figures 4 and 5	+25°C	01, 02	0	10	A
Line regulation accuracy	ΔV _{OUT} / ΔV _{IN}	V _{OUT} = 1.2 V, I _{OUT} = 0 A, P _{VIN} = V _{IN} = 3.5 V to 20 V	+25°C	01, 02	0.15 typical		%
		V _{OUT} = 1.2 V, I _{OUT} = 10 A, P _{VIN} = V _{IN} = 5 V to 20 V			0.15 typical		
Load regulation accuracy	ΔV _{OUT} / ΔI _{OUT}	I _{OUT} = 0 A to 10 A, V _{OUT} = 1.2 V, P _{VIN} = V _{IN} = 12 V	+25°C	01, 02	0.1 typical		%
Output ripple voltage	ΔV _{OUT}	I _{OUT} = 10 A, V _{OUT} = 1.2 V, P _{VIN} = V _{IN} = 12 V	+25°C	01, 02	27 typical		mVPP

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
DYNAMICS CHARACTERISTICS SECTION.							
Voltage change for positive load step	ΔV _{OUT-DP}	I _{OUT} = 0 A to 5 A, current slew rate = 2.5 A/μs, P _{VIN} = V _{IN} = 12 V, V _{OUT} = 1.2 V	+25°C	01, 02	45 typical		mVPP
Voltage change for negative load step	ΔV _{OUT-DN}	I _{OUT} = 5 A to 0 A, current slew rate = 2.5 A/μs, P _{VIN} = V _{IN} = 12 V, V _{OUT} = 1.2 V	+25°C	01, 02	55 typical		mVPP
REFERENCE SECTION. <u>3/</u>							
Reference voltage (include error and differential amplifiers' offset)	V _{REF1}		-55°C to +125°C	01	-0.9	0.9	%
				02	-0.95	0.95	
DIFFERENTIAL AMPLIFIER SECTION. <u>3/</u>							
DC gain	U _{G_DA}	Unity gain amplifier	+25°C	01, 02	0 typical		dB
Unity gain bandwidth	U _{GBW_DA}		+25°C	01, 02	5 typical		MHz
Maximum source current for current sharing	I _{VSEN1-}	V _{SEN1-} source current for current sharing when parallel multiple modules each of which has its own voltage loop	+25°C	01	350 typical		μA
Output voltage <u>4/</u> swing			-55°C to +125°C	01, 02	0	V _{CC} - 1.8	V
Disable threshold	V _{VSEN-}	V _{MON1} = tri-state	+25°C	01, 02	V _{CC} - 0.4 typical		V
OVERCURRENT PROTECTION SECTION. <u>3/</u>							
Channel overcurrent limit	I _{SOURCE}	V _{CC} = 2.97 V to 5.6 V	+25°C	01	108 typical		μA
		V _{CC} = 5 V	-55°C to +125°C		84	122	
		V _{CC} = 2.97 V to 5.6 V	+25°C	02	111 typical		
		V _{CC} = 5 V	-55°C to +125°C		84	129	
Share pin OC threshold	V _{OC_ISHARE}	Comparator offset included	-55°C to +125°C	01, 02	1.16	1.22	V

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
POWER GOOD MONITOR SECTION. <u>3/</u>							
Undervoltage (UV) falling trip point	VUVF	Percentage below reference point	-55°C to +125°C	01, 02	-15	-11	%
Undervoltage (UV) rising hysteresis	VUVR_HYS	Percentage above UV trip point	+25°C	01, 02	4 typical		%
Overvoltage (OV) rising trip point	VOVR	Percentage above reference point	-55°C to +125°C	01, 02	11	15	%
Overvoltage (OV) falling hysteresis	VOVF_HYS	Percentage below OV trip point	+25°C	01, 02	4 typical		%
PGOOD low output voltage		IPGOOD = 2 mA	-55°C to +125°C	01, 02		0.35	V
Sinking impedance		IPGOOD = 2 mA	-55°C to +125°C	01, 02		70	Ω
Maximum sinking current		VPGOOD < 0.8 V	+25°C	01, 02	10 typical		mA
OVERVOLTAGE (OV) PROTECTION SECTION. <u>3/</u>							
OV latching trip point		EN = UGATE = LATCH low, LGATE = high	-55°C to +125°C	01, 02	118	122	%
OV non-latching trip point		EN = low, UGATE = low, LGATE = high	+25°C	01, 02	113 typical		%
LGATE release trip point		EN = low/high, UGATE = low, LGATE = low	+25°C	01, 02	87 typical		%
OVER TEMPERATURE PROTECTION SECTION.							
Over temperature trip				01, 02	150 typical		°C
Over temperature release threshold				01, 02	125 typical		°C

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 8

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
INTERNAL COMPONENT VALUES SECTION.							
Internal resistor between PVCC and VCC pin	RCC		+25°C	01, 02	5 typical		Ω
Internal resistor between PHASE and OCSET pin	RISEN-IN		+25°C	01, 02	2.2 typical		kΩ
Internal resistor between FSYNC_IN and SGND pin	RFS		+25°C	01, 02	59 typical		kΩ
Internal resistor between PGOOD and VCC pin	RPG		+25°C	01, 02	10 typical		kΩ
Internal resistor between CLKOUT and VCC pin	RCLK		+25°C	01, 02	10 typical		kΩ
Internal resistor between PH_CNTRL and VCC pin	RPHC		+25°C	01, 02	10 typical		kΩ
Internal resistor between VOUT_SET and VSEN_REM- pin	ROS1		+25°C	01, 02	2.2 typical		kΩ

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, parameters with minimum and maximum limits are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.
- 3/ Parameters are 100% tested for internal integrated circuit prior to module assembly.
- 4/ Limits are considered typical and are not production tested.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 9

Case X

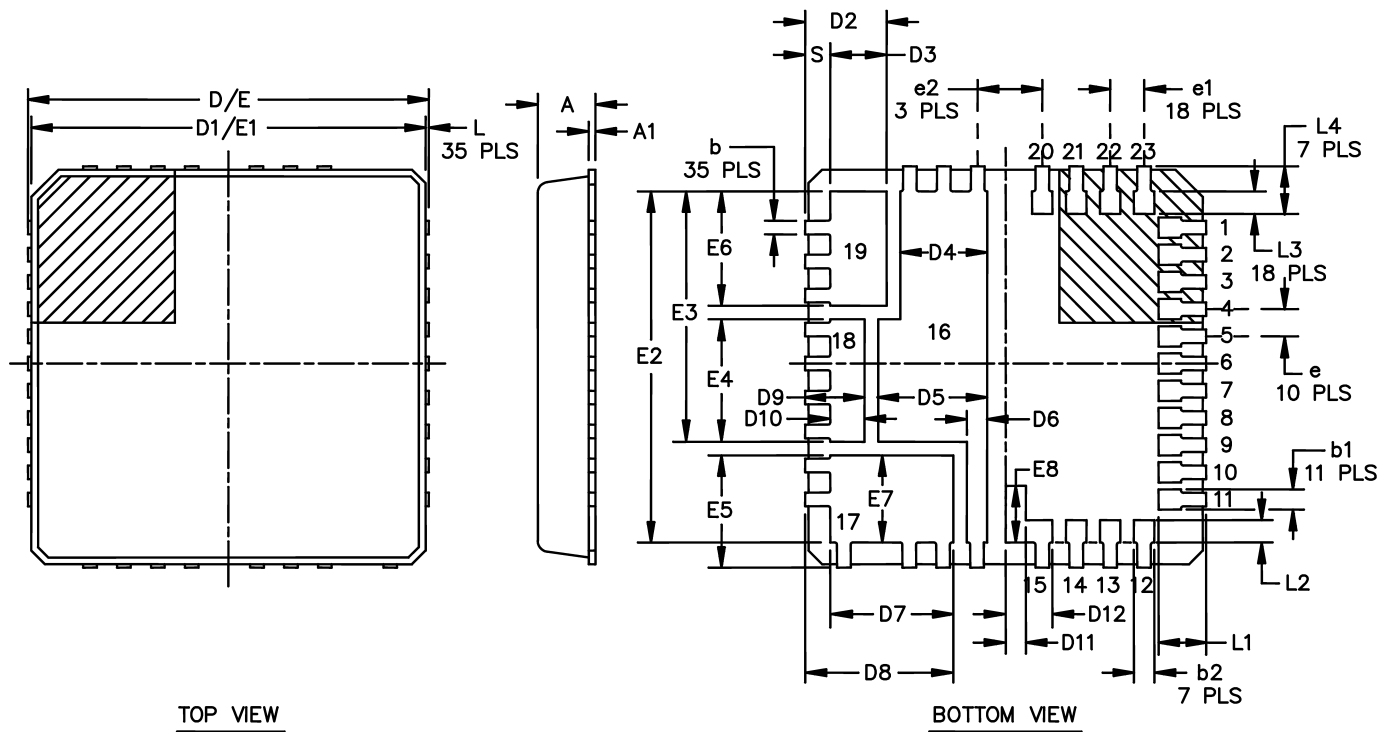


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 10

Case X - continued.

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	2.0	2.4	0.079	0.094
A1	0.25 BSC		0.010 BSC	
b	0.5 BSC		0.020 BSC	
b1	---	0.7	---	0.028
b2	---	0.8	---	0.031
D	15.6	16.0	0.614	0.630
D1	14.8	15.2	0.583	0.598
D2	---	3.22	---	0.127
D3	---	2.2	---	0.087
D4	---	3.4	---	0.134
D5	---	4.26	---	0.168
D6	---	0.8	---	0.031
D7	---	4.8	---	0.189
D8	---	5.82	---	0.229
D9	---	2.36	---	0.093
D10	---	1.34	---	0.053
D11	---	0.82	---	0.032
D12	---	2.0	---	0.079

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
E	15.6	16.0	0.614	0.630
E1	14.8	15.2	0.583	0.598
E2	---	13.8	---	0.543
E3	---	9.9	---	0.390
E4	---	4.7	---	0.185
E5	---	4.38	---	0.172
E6	---	4.7	---	0.185
E7	---	3.4	---	0.134
E8	---	2.28	---	0.090
e	1.0	1.2	0.039	0.047
e1	1.2	1.4	0.047	0.055
e2	2.6 BSC		0.102 BSC	
L	0.2	0.6	0.008	0.024
L1	1.80	1.90	0.070	0.075
L2	---	0.90	---	0.035
L3	---	0.75	---	0.029
L4	1.85	1.95	0.073	0.077
s	---	1.02	---	0.040

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Unless otherwise specified, tolerance: decimal ± 0.2 mm, body tolerance ± 0.2 mm.
3. The configuration of the pin 1 identifier is optional, but must be located within the zone indicated.
The pin 1 identifier may be either a mold or mark feature.
4. See manufacturer's datasheet for the recommended land pattern or stencil pattern.

FIGURE 1. Case outline - continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 11

Device types	01 and 02
Case outline	X
Terminal number	Terminal symbol
1	VOUT_SET
2	VSEN_REM-
3	ISFETDRV
4	PGND1
5	ISET
6	ISHARE
7	FSYNC IN
8	CLKOUT
9	PH_CNTRL
10	ISHARE_BUS
11	FF
12	EN
13	VIN
14	PVCC
15	PGND1
16	PHASE
17	PVIN
18	PGND
19	VOUT
20	OCSET
21	VCC
22	PGOOD
23	NC

FIGURE 2. Terminal connections.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 12

Terminal number	Terminal symbol	Description
1	VOUT_SET	Analog voltage input. Used with VOUT to program the regulator output voltage. The typical input impedance of VOUT_SET with respect to VSEN_REM- is 600 k Ω for device type 01 and VOUT_SET with respect to VSEN_REM- is 500 k Ω for device type 02. Voltage input typically 0.6 V.
2	VSEN_REM-	Analog voltage input. This pin is the negative input of standard unity gain operational amplifier for differential remote sense for the regulator, and should connect to the negative rail of the load / processor. This pin can be used for VOUT trimming by connecting a resistor from this pin to the VOUT_SET pin.
3	ISFETDRV	Digital output. This pin is used to drive an optional NFET, which will connect ISHARE with the system ISHARE bus upon completing a pre-bias startup. Voltage output range: 0 V to 5 V.
4, 15	PGND1	Normal ground. All voltage levels are referenced to this pad. This pad provides a return path for the low side MOSFET drives and internal power circuitries as well as all analog signals. PGND and PGND1 should be connected together with a ground plane.
5	ISET	Analog current output. This pin sources a 15 μ A offset current plus channel 1's average current. The voltage (VISET) set by an external resistor (RISET) represents the average current level of the local active module. For full scale current, RISET should be $\sim$ 10 k Ω . Output current range: 15 μ A to 123 μ A typically for device type 01 and 15 μ A to 126 μ A typically for device type 02. The ISET and ISHARE pins are used for current sharing purposes with multiple device modules. In the single module configuration, this pin can be tied to the ISHARE pin. In multi-phase operation, if noise is a concern, add an additional 10 pF capacitor to the ISET line.
6	ISHARE	Analog current output. Cascaded system level overcurrent shutdown pin. This pin is used where you have multiple modules configured for current sharing and is used with a common current share bus. The bus sums each of the modules' average current contribution to the load to protect for an overcurrent condition at the load. The pin sources 15 μ A plus average module's output current. The shared bus voltage (VISHARE) is developed across an external resistor (RISHARE). VISHARE represents the average current of all active channel(s) that connected together. The ISHARE bus voltage is compared with each module's internal reference voltage set by each module's RISET resistor. This will generate an individual current share error signal in each cascaded controller. The share bus impedance RISHARE should be set as RISET/NCTRL, RISET divided by number of active current sharing controllers. The output current from this pin generates a voltage across the external resistor. This voltage, VISHARE, is compared to an internal 1.2 V threshold for average overcurrent protection. For full-scale current, RISHARE should be $\sim$ 10 k Ω . Typically 10 k Ω is used for RSHARE and RSET. Output current range: 15 μ A to 123 μ A typically for device type 01 and 15 μ A to 126 μ A typically for device type 02.

FIGURE 2. Terminal connections - continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 13

Terminal number	Terminal symbol	Description
7	FSYNC IN	Analog input control pin. An optional external resistor (RFS-ext) connected to this pin and ground will increase the oscillator switching frequency. It has an internal 59 k Ω resistor for a default frequency of 700 kHz. The internal oscillator will lock to an external frequency source when connected to a square waveform. The external source is typically the CLKOUT signal from another identical device or an external clock. The internal oscillator synchronizes with the leading positive edge of the input signal. Input voltage range for external source: 0 V to 5 V square wave. When not synchronized to an external clock, a 100 pF capacitor between FSYNC_IN and PGND1 is recommended.
8	CLKOUT	Digital voltage output. This pin provides a clock signal to synchronize with other identical devices. When there is more than one identical device in the system, the two independent regulators can be programmed via PH_CNTRL for different degrees of phase delay.
9	PH_CNTRL	Analog input. The voltage level on this pin is used to program the phase shift of CLKOUT clock signal to synchronize with other module(s).
10	ISHARE_BUS	Open pin until first PWM pulse is generated. Then, via an internal field effect transistor (FET), this pin connects the module's ISHARE to the system's ISHARE bus after pre-bias is complete and soft-start is initiated.
11	FF	Analog voltage input. The voltages on this pin is fed into the controller, adjusting the sawtooth amplitude to generate the feed forward function. Voltage input 0.8 V to VCC. Typically FF is connected to EN.
12	EN	This is a double function pin: Analog input voltage. The input voltage to this pin is compared with a precision 0.8 V reference and enables the digital soft start. Input voltage range is 0 V to VCC or VIN through a pull up resistor maintaining a typical current of 5 mA. Analog voltage output. This pin can be used as a voltage monitor for input bus undervoltage lockout. The hysteresis levels of the lockout can be programmed via this pin using a resistor divider network. Furthermore, during fault conditions (such as overvoltage, overcurrent, and over temperature), this pin is used to communicate the information to other cascaded modules by pulling low the wired OR as it is an open drain. Output voltage range is 0 V to VCC.
13	VIN	Analog voltage input. This pin should be tied directly to the input rail when using the internal linear regulator. It provides power to the internal linear drive circuitry. When used with an external 5 V supply, this pin should be tied directly to VCC. The internal linear device is protected against the reversed bias generated by the remaining charge of the decoupling capacitor at VCC when losing the input rail. Input voltage range 4.5 V to 20 V.

FIGURE 2. Terminal connections - continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 14

Terminal number	Terminal symbol	Description
14	PVCC	Analog output. This pin is the output of the internal series linear regulator. It provides the bias for both low side and high side drives. Its operational voltage range is 4.5 V to 5.6 V. The decoupling ceramic capacitor in the PVCC pin is 10 μ F
16	PHASE	Analog output. This pin is the phase node of the regulator. Output voltage range 0 V to 30 V.
17	PVIN	Analog input. This input voltage is applied to the power FETS with the FET's ground being the PGND pin. It is recommended to place input decoupling capacitance, 22 μ F, directly between PVIN pin and PGND pin as close as possible to the module. Input voltage range: 3 V to 20 V.
18	PGND	All voltage levels are referenced to this pad. This is the low side MOSFET ground. PGND and PGND1 should be connected together with a ground plane.
19	VOUT	Output voltage from the module. Output voltage range: 0.6 V to 7.5 V.
20	OCSET	Analog input. This pin is used with PHASE pin to set the current limit of the module. Input voltage range 0 V to 30 V.
21	VCC	Analog input. This pin provides bias power for the analog circuitry. Its operational range is 4.5 V to 5.6 V. In 3.3 V application, VCC, PVCC, and VIN should be shorted to allow operation at the low end input as it relates to the VCC falling threshold limit. This pin can be powered either by the internal linear regulator or by an external voltage source.
22	PGOOD	Analog output. This pin, pulled up to VCC via a 10 k Ω resistor, provides an power good signal when the output is within 9% of nominal output regulation point with 4 % hysteresis (13% / 9%), and soft start is complete. PGOOD monitors the outputs (VMON) of the internal differential amplifiers. Output voltage range: 0 V to VCC.
23	NC	Not internally connected.
PD1	PHASE thermal pad	Used for both the PHASE pin (pin 16) and for heat removal connecting to heat dissipation layers using vias. Potential should be floating and not electrically connected to anything except PHASE, pin 16.
PD2	VIN thermal pad	Used for both the PVIN (pin 17) and for heat removal connecting to heat dissipation layers using vias. Potential should be floating and not electrically connected to anything except PVIN, pin 17.
PD3	PGND thermal pad	Used for both the PGND pin (pin 18) and for heat removal connecting to heat dissipation layers using vias. Potential should be floating and not electrically connected to anything except PGND, pin 18.
PD4	VOUT thermal pad	Used for both the VOUT (pin 19) and for heat removal connecting to heat dissipation layers using vias. Potential should be floating and not electrically connected to anything except VOUT, pin 19.

FIGURE 2. Terminal connections - continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 15

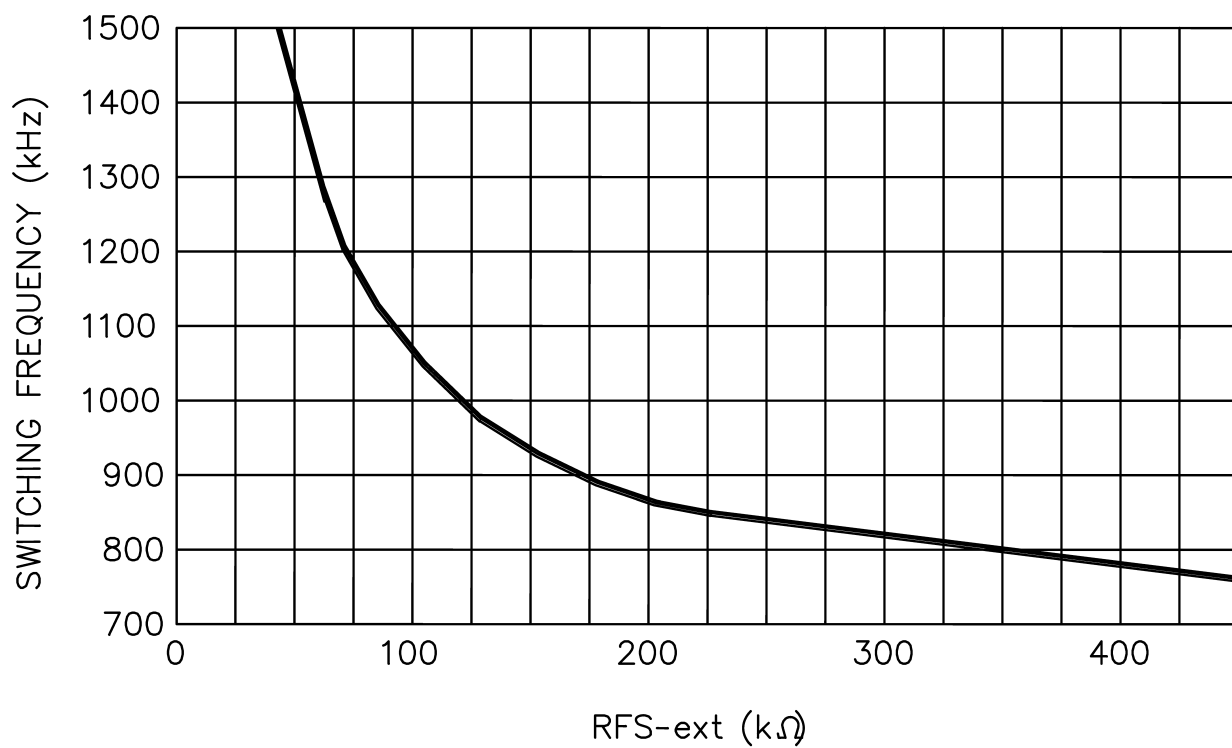


FIGURE 3. External frequency setting resistance versus switching frequency.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 16

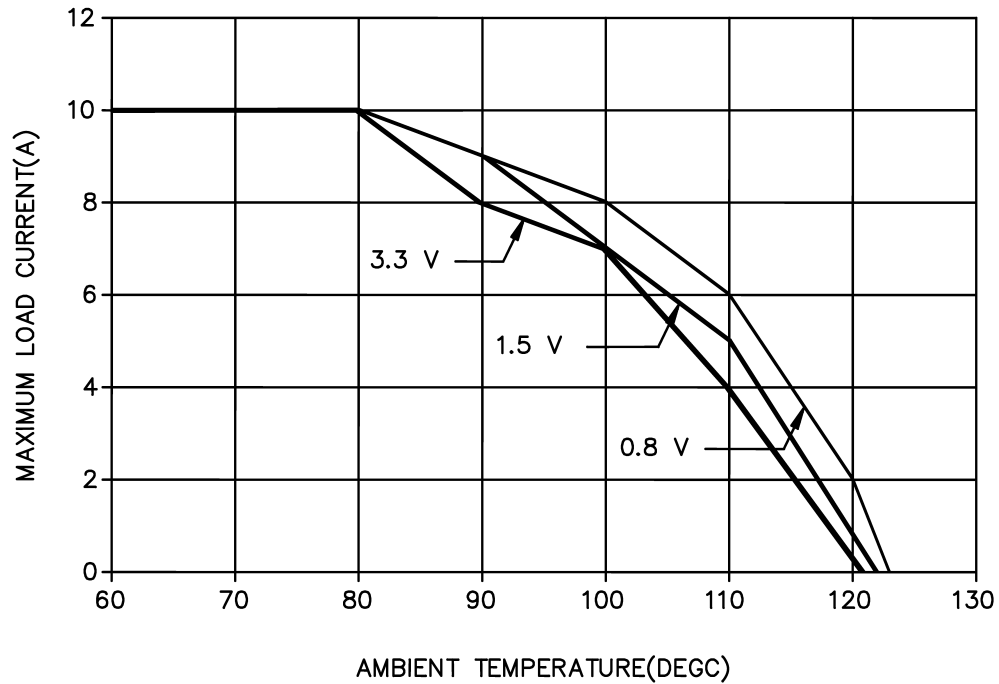


FIGURE 4. Derating curve (5 VIN).

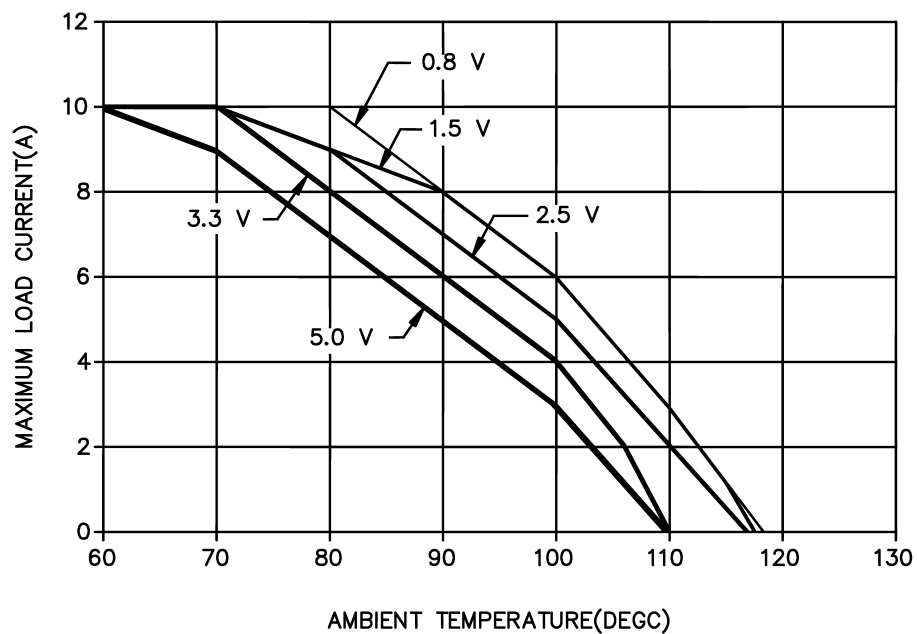


FIGURE 5. Derating curve (12 VIN).

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 17

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Part marking	Vendor part number <u>2/</u>
V62/10608-01XB	<u>3/</u>	8200MMREP	ISL8200MMREP
V62/10608-02XB	<u>3/</u>	ISL8200AMMREP	ISL8200AMMREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add "-T" suffix for tape and reel.

3/ Not available from an approved source of supply. The last known supplier is listed below.

CAGE code

34371

Source of supply

Renesas Electronics America, Inc.
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/10608
		REV C	PAGE 18