

REVISIONS															
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED
A	Update vendor CAGE 1ES66 information. Update boilerplate paragraphs to current VID description requirements. - DRH										22-10-12				Muhammad A. Akbar



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14						

PMIC N/A	PREPARED BY Phu H. Nguyen		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime		
	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, DIGITAL-LINEAR, IMPROVED, 8-CHANNEL/DUAL 4-CHANNEL, CMOS ANALOG MULTIPLEXERS, MONOLITHIC SILICON		
	APPROVED BY Thomas M. Hess				
	Original date of drawing	09-09-16	SIZE A	CAGE CODE 16236	DWG NO. V62/09630
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of an improved, 8-channel/Dual 4-channel, CMOS analog multiplexers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/09630</u>	-	<u>01</u>	<u>X</u>	<u>B</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	DG408	8-channel, CMOS analog multiplexer
02	DG409	Dual 4-channel, CMOS analog multiplexer

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MS012	Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Voltage	
V+	-0.3 V to 44 V
GND	-0.3 V to 25 V
Digital input, S, D	(V- - 2V) to (V+ + 2V) or 30 mA (whichever occurs first) <u>2/</u>
Continuous current (any terminal)	30 mA
Peak current, S, D (pulsed at 1 ms, 10% duty cycle max)	100 mA
Operating temperature range	-55°C to +125°C
Storage temperature range	-55°C to +150°C
Junction temperature	+150°C
Lead temperature (soldering, 10 sec)	+300°C
Electro Static Discharge (ESD)	
Human Body Model (HBM)	2000 V
Class	1C
Moisture Sensitive Level (MSL)	Level 1

1.4 Thermal data table.

Case outline letter	X	X	Units
PC Board	Single Layer	Multi-Layer <u>3/</u>	
Power dissipation (P _D), maximum at +70°C	696	1096	mW
Power dissipation (P _D) derating above +70°C	8.7	13.7	mW/°C
Thermal resistance, junction to case (θ _{JC})	32	23	°C/W
Thermal resistance, junction to ambient (θ _{JA})	115	73	°C/W

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2/ Signals on S₋, D₋, EN, A0, A1, or A2 exceeding V₊ or V₋ are clamped by internal diodes. Limit forward current to maximum current ratings.
- 3/ Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to manufacturer’s website.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Functional diagram. The functional diagram shall be as shown in figure 4.

3.5.5 Test circuits and timing waveforms.

3.5.5.1 Transition time. The transition time shall be as shown in figure 5.

3.5.5.2 Enable switching time. The enable switching time shall be as shown in figure 6.

3.5.5.3 Break before make interval. The break before make interval shall be as shown in figure 7.

3.5.5.4 Charge injection. The charge injection shall be as shown in figure 8.

3.5.5.5 Off isolation. The off isolation shall be as shown in figure 9.

3.5.5.6 Cross talk. The cross talk shall be as shown in figure 10.

3.5.5.7 Source and drain capacitance. The source and drain capacitance shall be as shown in figure 11.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Device type: All 2/	T _A	Limits		Unit
				Min	Max	

DUAL SUPPLIES**Switch**

Analog signal range	V _{ANALOG}	4/		-15	15	V
Drain source on resistance	r _{DS(ON)}	I _S = -1.0 mA, V _D = ±10 V	25°C		100	Ω
			-55°C to 125°C		125	
On resistance matching between channels	Δr _{DS(ON)}	I _S = -1.0 mA, V _D = ±10 V 5/	25°C		8	Ω
			-55°C to 125°C		10	
On resistance flatness	r _{FLAT}	I _S = -1.0 mA, V _D = ±5 V or 0 V	25°C		9	Ω
			-55°C to 125°C		12	
Source off leakage current 6/	I _{S(OFF)}	V _D = ±10 V, V _S = ∓10 V, V _{EN} = 0 V	25°C	-0.5	0.5	nA
			-55°C to 125°C	-50	50	
Drain off leakage current 6/	I _{D(OFF)}	V _D = ±10 V, V _S = ∓10 V, V _{EN} = 0 V	Device type 01	25°C	-1	nA
				-55°C to 125°C	-100	
			Device type 02	25°C	-1	
				-55°C to 125°C	-50	
Drain on leakage current 6/	I _{D(ON)}	V _D = ±10 V, V _S = ±10 V, sequence each switch on	Device type 01	25°C	-1	nA
				-55°C to 125°C	-100	
			Device type 02	25°C	-1	
				-55°C to 125°C	-50	

Input

Input current with input voltage high	I _{AH}	V _A = 2.4 V or 15 V		-1.0	1.0	μA
Input current with input voltage low	I _{AL}	V _{EN} = 0 V or 2.4 V, V _A = 0 V		-1.0	1.0	μA

Supply

Power supply range				±5	±20	V
Positive supply current	I ₊	V _{EN} = V _A = 0 V or 4.5 V	25°C		30	μA
			-55°C to 125°C		75	
		V _{EN} = 2.4 V, V _{A(ALL)} = 0 V or 2.4 V	25°C		0.5	mA
			-55°C to 125°C		2	
Negative supply current	I ₋	V _{EN} = 2.4 V, V _{A(ALL)} = 0 V or 2.4 V	25°C	-1	1	μA
			-55°C to 125°C	-10	10	

Dynamic

Transition time	t _{TRANS}	See figure 5	25°C		175	ns
			-55°C to 125°C		250	
Break before make interval	t _{OPEN}	See figure 7	25°C	10		
Enable turn on time	t _{ON(EN)}	See figure 6	25°C		150	
			-55°C to 125°C		225	
Enable turn off time	t _{OFF(EN)}	See figure 6	25°C		150	
			-55°C to 125°C		300	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions Device type: All <u>2/</u>	T _A	Limits		Unit
				Min	Max	

DUAL SUPPLIES (continued)**Dynamic (continued)**

Charge injection <u>4/</u>	Q	C _L = 1.0 nF, V _S = 0 V, R _S = 0 Ω See figure 8		25°C		15	pC
Off isolation <u>7/</u>	V _{ISO}	V _{EN} = 0 V, R _L = 1 kΩ, f = 100 kHz, See figure 9		25°C	-75 TYP		dB
Cross talk between input channels	V _{CT}	V _{EN} = 2.4 V, f = 100 kHz, V _{GEN} = 1 V _{P-P} , R _L = 1 kΩ, See figure 10		25°C	-92 TYP		dB
Logic input capacitance	C _{IN}	f = 1 MHz		25°C	8 TYP		pF
Source OFF capacitance	C _{S(OFF)}	f = 1 MHz, V _{EN} = V _S = 0 V, See figure 11		25°C	3 TYP		
Drain OFF capacitance	C _{D(OFF)}	f = 1 MHz, V _{EN} = 0.8 V V _D = 0 V, See figure 11	Device type 01		26 TYP		
			Device type 02		14 TYP		
Drain ON capacitance	C _{D(ON)} + C _{S(ON)}	f = 1 MHz, V _{EN} = 2.4 V V _D = 0 V, See figure 11	Device type 01		37 TYP		
			Device type 02		25 TYP		

SINGLE SUPPLY (V₊ = 12 V, V₋ = 0 V)**Switch**

Analog signal range	V _{ANALOG}	<u>4/</u>		0	12	V
Drain source on resistance	r _{DS(ON)}	I _S = -1.0 mA, V _D = 3 V or 10 V	25°C		175	Ω

Dynamic

Transition time <u>4/</u>	t _{TRANS}	V _{S1} = 8 V, V _{S8} = 0 V, V _A = 0 V See figure 5	25°C		450	ns
Enable turn ON time <u>4/</u>	t _{ON(EN)}	V _{AL} = 0 V, V _{S1} = 5 V, See figure 6	25°C		600	
Enable turn OFF time <u>4/</u>	t _{OFF(EN)}	V _{AL} = 0 V, V _{S1} = 5 V, See figure 6	25°C		300	
Charge injection	Q	C _L = 1.0 nF, V _S = 0 V, R _S = 0 Ω, See figure 8	25°C	2 TYP		pC

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V₊ = 15 V, V₋ = -15 V, GND = 0 V, V_{AH} = +2.4 V, V_{AL} = +0.8 V, T_A = -55°C to 125°C (unless otherwise noted).

3/ The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

4/ Guaranteed by design.

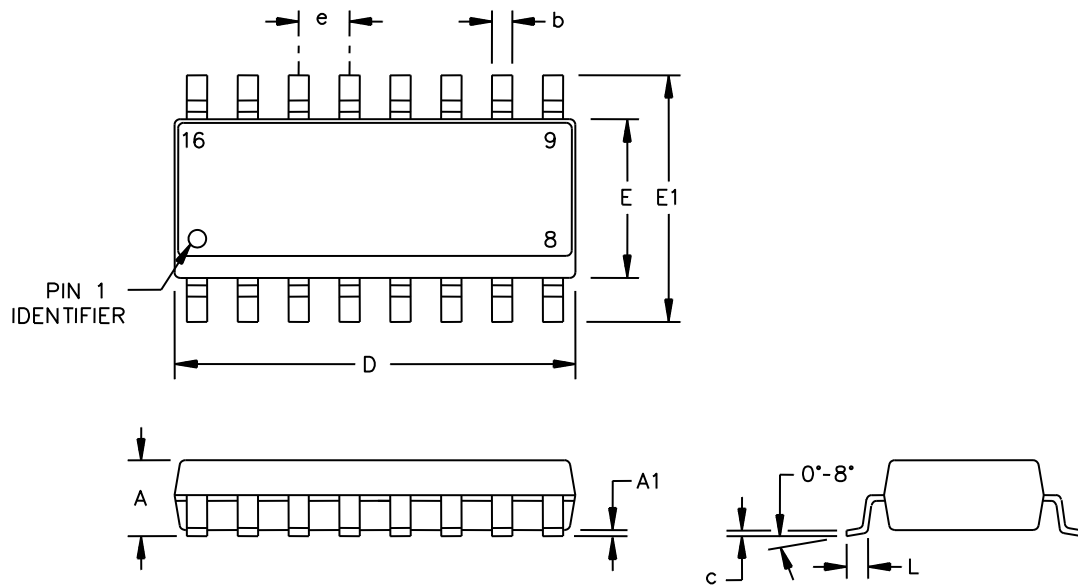
5/ ΔR_{ON} = R_{ON(MAX)} – R_{ON(MIN)}. On resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured at the extremes of the specified analog signal range.

6/ Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

7/ Off isolation = 20log V_D/V_S, where V_D = output and V_S = input to off switch.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.053	.069	1.35	1.75	E	.150	.157	3.80	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.014	.019	0.35	0.49	e	.050 BSC		1.27 BSC	
c	.007	.010	0.19	0.25	L	.016	.050	0.40	1.27
D	.386	.394	9.80	10.00					

NOTES:

1. D and E do not include mold flash.
2. Mold flash or protrusions not to exceed 0.15 mm (.006").
3. Leads to be coplanar within 0.10 mm (.004").
4. Meets JEDEC MS012.
5. Controlling dimensions are millimeters. Inch dimensions are given for reference only.

FIGURE 1. Case outline.

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Case outlines: X					
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
	Device type 01	Device type 02		Device type 01	Device type 02
1	A0	A0	9	S8	DB
2	EN	EN	10	S7	S4B
3	V-	V-	11	S6	S3B
4	S1	S1A	12	S5	S2B
5	S2	S2A	13	V+	S1B
6	S3	S3A	14	GND	V+
7	S4	S4A	15	A2	GND
8	D	DA	16	A1	A1

FIGURE 2. Terminal connections.

Device type 01					Device type 02			
A2	A1	A0	EN	ON Switch	A1	A0	EN	ON Switch
X	X	X	0	None	X	X	0	None
0	0	0	1	1	0	0	1	1
0	0	1	1	2	0	1	1	2
0	1	0	1	3	1	0	1	3
0	1	1	1	4	1	1	1	4
1	0	0	1	5				
1	0	1	1	6				
1	1	0	1	7				
1	1	1	1	8				

Logic "0" VAL ≤ 0.8 V
Logic "1" VAH ≥ 2.4 V

FIGURE 3. Truth table.

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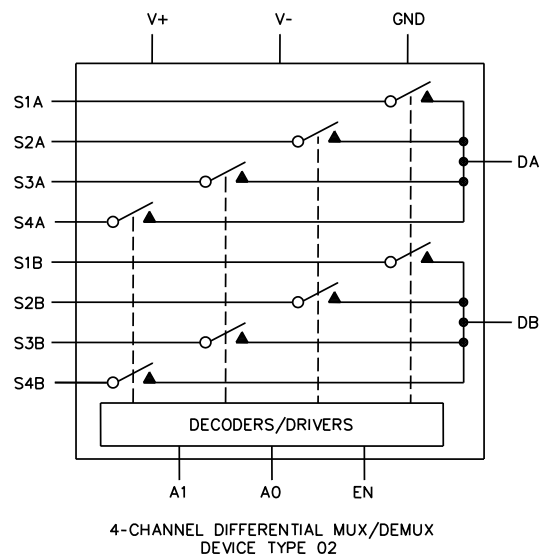
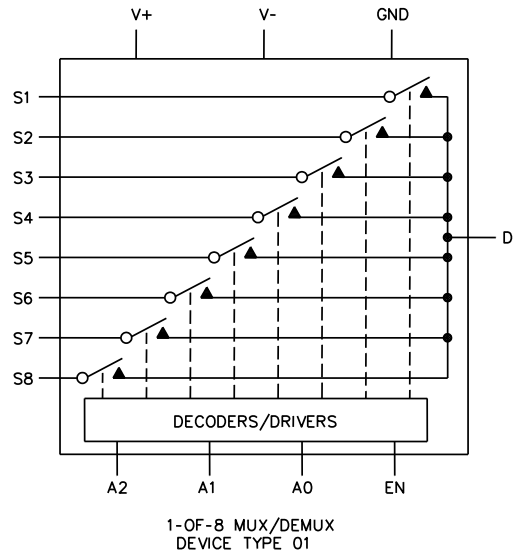


FIGURE 4. Functional diagrams.

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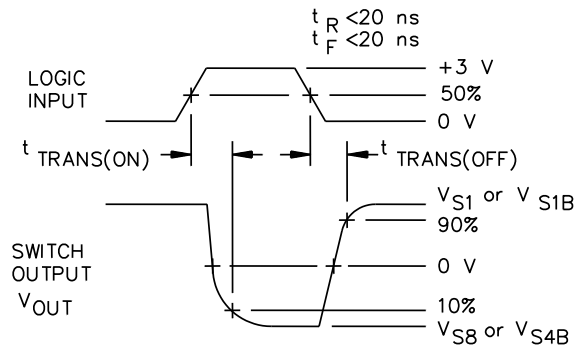
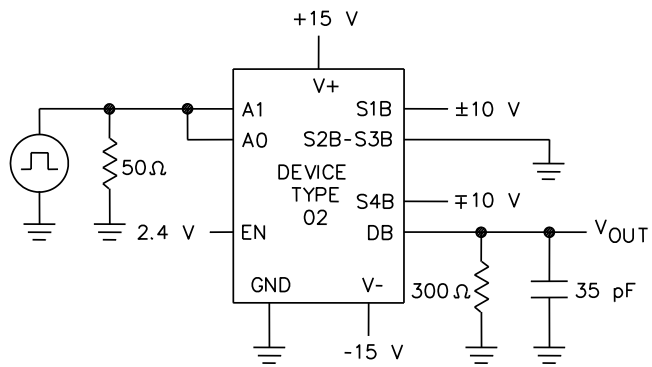
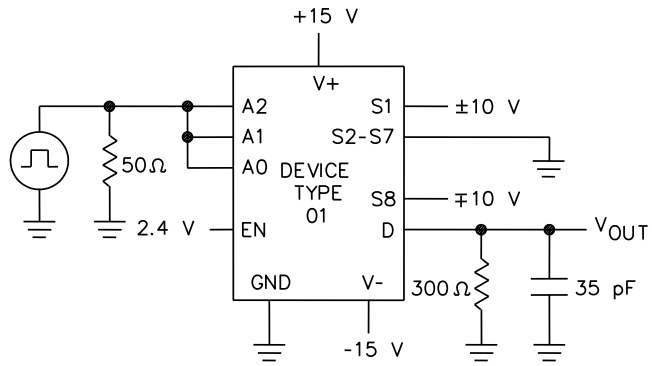


FIGURE 5. Transition time.

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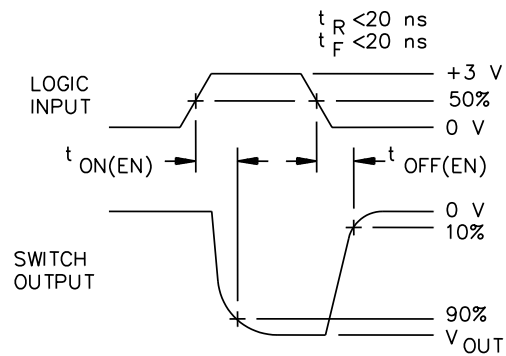
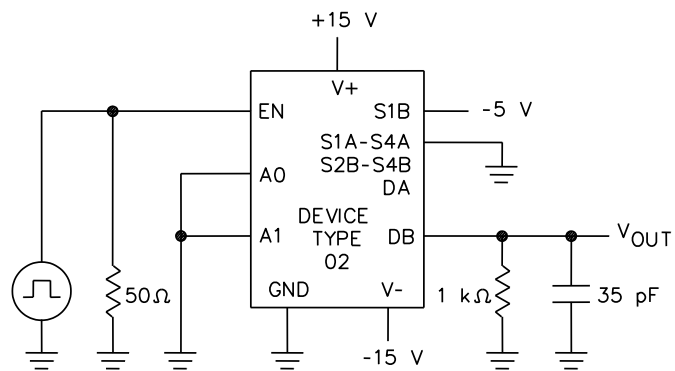
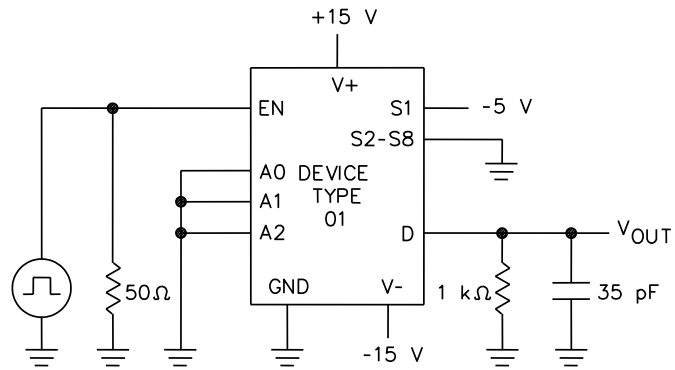


FIGURE 6. Enable switching time.

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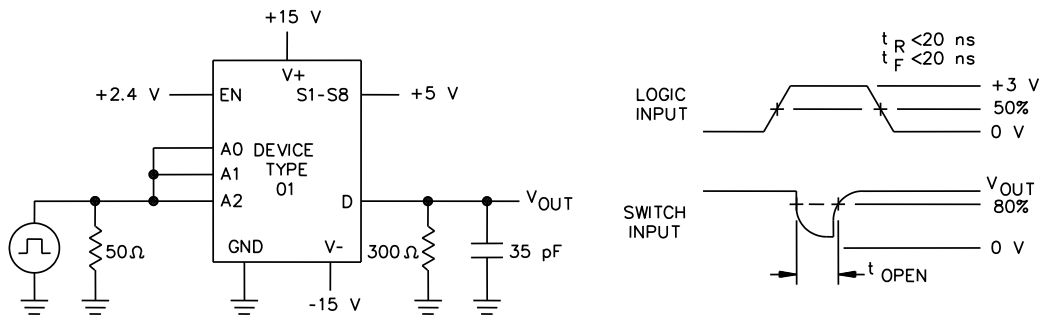


FIGURE 7. Break before make interval.

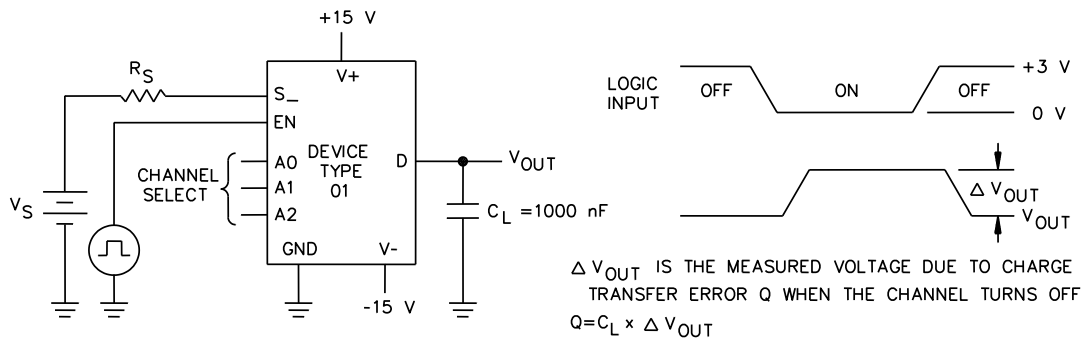


FIGURE 8. Charge injection.

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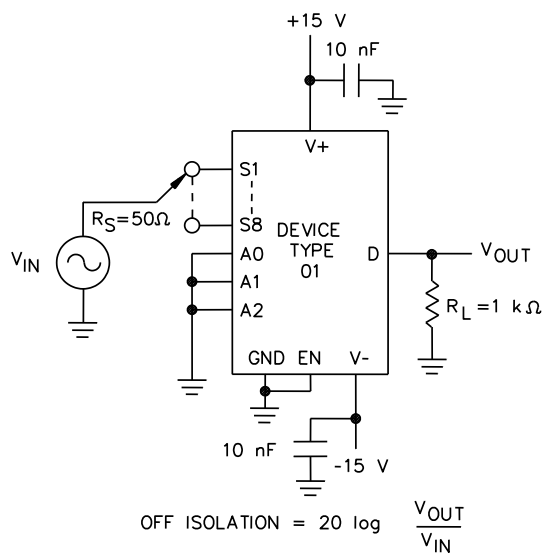


FIGURE 9. Off Isolation.

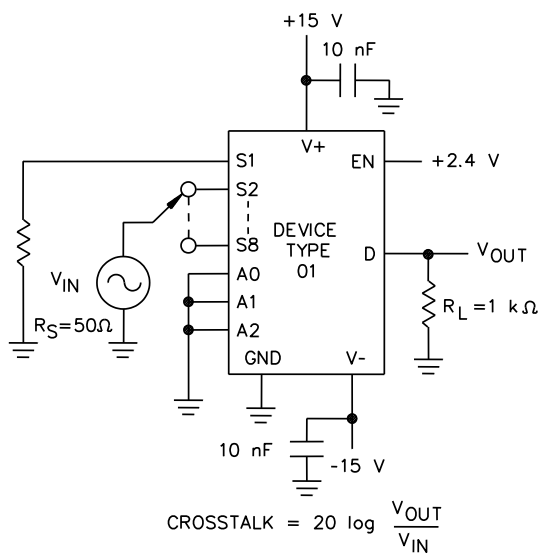


FIGURE 10. Crosstalk.

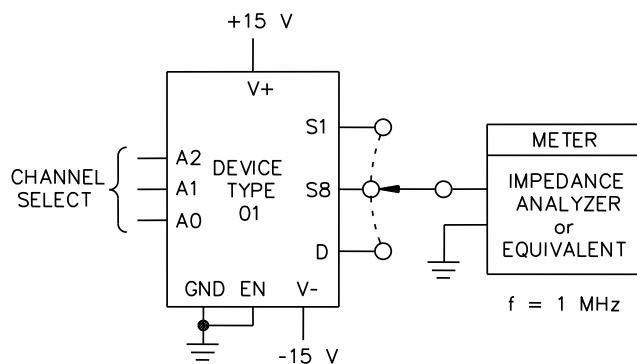


FIGURE 11. Source and drain capacitance.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

6.4 Reliability. These /PR devices (100%) pass through 120 hours burn-in at 135°C after which they are 100% tri-temp tested at room temperature with PDA, +125°C, and -55°C.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	
V62/09630-01XB	1ES66	DG408MY/PR	DG408MY/PR-T <u>2/</u>
V62/09630-02XB	1ES66	DG409MY/PR	DG409MY/PR-T <u>2/</u>

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For tape and reel.

CAGE code

1ES66

Source of supply

Maxim Integrated
160 Rio Robles
San Jose, CA 95134

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