REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update paragraphs to current requirements. - ro	13-04-04	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	18-06-19	C. SAFFLE
C	Update document to current requirements. - ro	25-03-24	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing (YR-MO-DA)

07-12-18

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TITLE

MICROCIRCUIT, LINEAR, DC/DC POWER SWITCHING REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/08608
REV C		PAGE 1 OF 14

AMSC N/A

5962-V006-25

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance DC/DC power switching regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08608	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	ISL8560	DC/DC power switching regulator

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-220	Plastic quad leadless package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage (V_{IN})	[GND – 0.3] V to 72 V
Voltage at BOOT pin	[GND – 0.3] V to 82 V
LX and RTCT pins	[GND – 0.3] V to 60 V
REF, FB, SS, $\overline{EN}$, SYNC, PGOOD pins	8 V
VCC5 pin	[GND – 0.3] V to 5.5 V
Power dissipation (P_D) :	
At +25°C	3 W
At +125°C	0.5 W
Junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to case (θ_{JC})	1.5°C/W 2/
Thermal resistance, junction to ambient (θ_{JA})	30°C/W 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	9.0 V to 60 V
Ambient temperature range (T_A)	-55°C to +125°C

_____

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3/ The θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See manufacturer’s technical brief TB379.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
V_{IN} SUPPLY SECTION.							
Input voltage range	V_{IN}		-55°C to +125°C	01	9.0	60	V
V_{IN} SUPPLY CURRENT SECTION.							
Shut down current	I_{DD}	V_{IN} = 9 V, $\overline{EN}$ = high	-55°C to +125°C	01		62	µA
		V_{IN} = 60 V, $\overline{EN}$ = high				145	
Operating current	I_{DD}	V_{IN} = 9 V, V_{FB} = 1.5 V	-55°C to +125°C	01		4	mA
		V_{IN} = 60 V, V_{FB} = 1.5 V				8.0	
VCC5 SUPPLY SECTION. A 1 µF capacitor is needed from VCC5 to GND.							
VCC5 output voltage		V_{IN} = 9.0 V to 60 V, I_L = 0 mA to 5 mA	-55°C to +125°C	01	4.9	5.1	V
Maximum output current		V_{IN} = 24 V	-55°C to +125°C	01		1.4	mA
INPUT UNDERVOLTAGE (UV) SECTION.							
Rising UV threshold			-55°C to +125°C	01	7.76	8.91	V
UV threshold hysteresis			-55°C to +125°C	01	0.17	0.55	V
BUCK THRESHOLD SECTION.							
Output voltage 3/		I_{OUT} = 2 A	-55°C to +125°C	01	1.2	V_{IN} - 5	V
Maximum duty cycle		F = 300 kHz	-55°C to +125°C	01	90		%
Minimum controllable on time		F = 300 kHz	+25°C	01	150 typical		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
OSCILLATOR SECTION.							
Total variation on set frequency		Over the V_{IN} range with frequency set by external resistor and capacitor at RTCT	+25°C	01	±10 typical		%
Frequency range (set by RTCT)	f_{OSC}		-55°C to +125°C	01	100	600	kHz
SYNC range	f_{OSC}		-55°C to +125°C	01	100	600	kHz
Tested oscillation frequency	f_{OSC}	V_{IN} = 9 V to 60 V, R_T = 100 kΩ, C_T = 1200 pF	+25°C	01	60 typical		kHz
		V_{IN} = 9 V to 60 V, R_T = 27.4 kΩ, C_T = 220 pF			275 typical		
Maximum ramp amplitude	ΔV_{OSC}	V_{IN} = 9 V	+25°C	01	1 typical		V_P
Modular gain	V_{VIN} / ΔV_{OSC}		+25°C	01	9 typical		
Minimum off time			-55°C to +125°C	01		300	ns
REFERENCE AND SOFT START SECTION.							
Internal reference voltage	V_{REF}		+25°C	01	1.21 typical		V
Soft start current	I_{SS}		-55°C to +125°C	01	8	12	μA
Soft start threshold	V_{SOFT}		-55°C to +125°C	01	0.8		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
ERROR AMPLIFIER SECTION.							
Transconductance	gm		-55°C to +125°C	01	3.9	7.2	mMho
Gain bandwidth product	GBW		+25°C	01	6 typical		MHz
Slew rate	SR		+25°C	01	15 typical		V/μs
COMP pin drive	I_{COMP}		+25°C	01	±200 typical		μA
Internal feedback voltage	V_{FB}	V_{IN} = 9.0 V to 60 V	-55°C to +125°C	01	1.194	1.222	V
Internal feedback bias current	I_{FB}	V_{FB} = 1.20 V	-55°C to +125°C	01		±100	nA
OVERCURRENT PROTECTION SECTION.							
Dynamic current limit on time	t_{OCON}		+25°C	01	16 typical		Clock pulse
Dynamic current limit off time	t_{OCOFF}		+25°C	01	4 typical		SS cycle
Switch current limit	I_{LIMIT}		+25°C	01	3.2	4.8	A
POWER GOOD (OPEN DRAIN) SECTION.							
Power good lower threshold	V_{PG-}	Fraction of the V_{OUT} set point, ~3 μs noise filter	-55°C to +125°C	01	85	89	%
	V_{PG+}				111	115	
PGOOD leakage current	I_{PGLKG}	V_{PULLUP} = 5.5 V	-55°C to +125°C	01		1	μA
PGOOD voltage low		I_{PGOOD} = 4 mA	-55°C to +125°C	01		0.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
MOSET SECTION.							
Switch on resistance	$r_{DS(ON)}$	I_{OUT} = 2 A, V_{BOOT} = [V_{IN} + 5.0] V, tested at wafer level	-55°C to +125°C	01		0.355	Ω
$\overline{EN}$ SECTION.							
Input high level (asserted)	VINHIGH		-55°C to +125°C	01	2.6		V
Input low level (unasserted)	VINLOW		-55°C to +125°C	01		1.2	V
Input current high	I_{ENHIGH}	V_{IN} = 24 V	-55°C to +125°C	01		30	µA
Input current low	I_{ENLOW}	V_{IN} = 24 V	-55°C to +125°C	01		30	µA
SYNC SECTION.							
Input high level (asserted)	VINHIGH		-55°C to +125°C	01	2.6		V
Input low level (unasserted)	VINLOW		-55°C to +125°C	01		1.2	V
Input current high	$I_{SYNCHIGH}$		-55°C to +125°C	01		0.2	µA
Input current low	$I_{SYNCLOW}$		-55°C to +125°C	01		0.2	µA
THERMAL SHUT DOWN SECTION.							
Thermal shut down temperature		Rising threshold	+25°C	01	150 typical		°C
Thermal shut down hysteresis			+25°C	01	15 typical		°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IN} = 48 V, V_{OUT} = 5.0 V, and I_{OUT} = 0 A.

3/ Additional heat sinking may be required to ensure that the junction temperature does not exceed above +125°C.

Case X

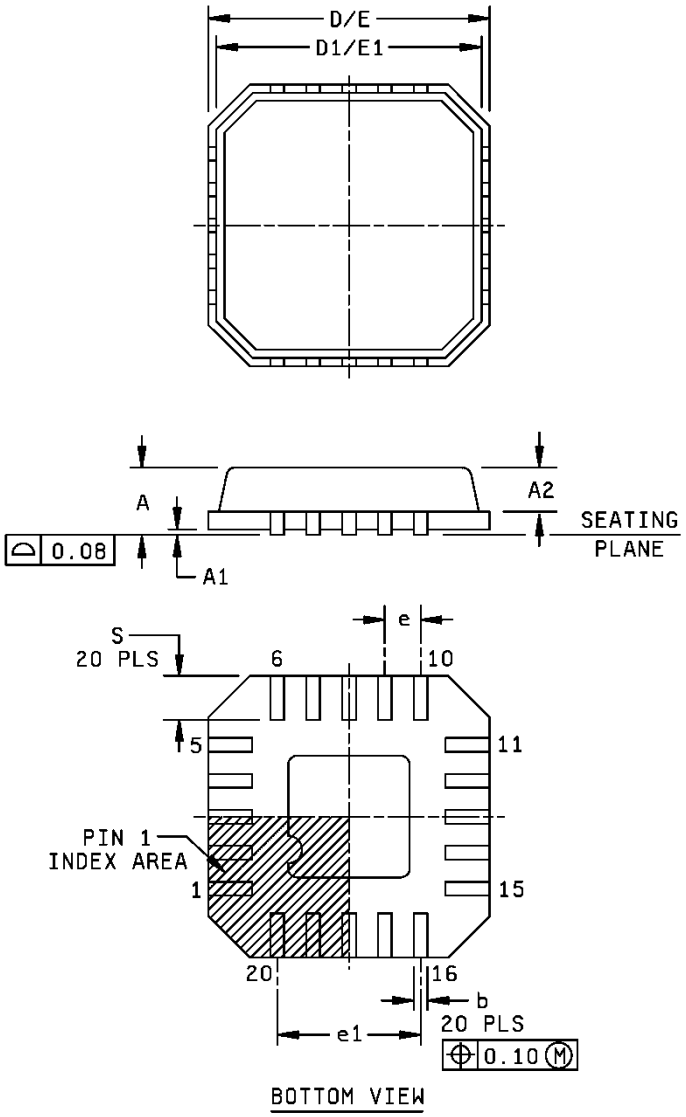


FIGURE 1. Case outline.

Symbol	Dimensions				Notes
	Millimeters		Inches		
	Min	Max	Min	Max	
A	0.80	1.00	0.031	0.039	
A1	---	0.05	---	0.001	
A2	---	1.00	---	0.039	6
b	0.28	0.38	0.011	0.014	3, 5
D	6.00 BSC		0.236 BSC		
D1	5.75 BSC		0.226 BSC		6
E	6.00 BSC		0.236 BSC		
E1	5.75 BSC		0.226 BSC		6
e	0.80 BSC		0.031 BSC		
e1	3.20 BSC		0.125 BSC		
S	---	0.60	---	0.024	6

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerancing conform to ASME Y 14.5M-1994.
3. Dimension “b” lead width applies to the metallized terminal and is measured between 0.15 mm (0.005 inch) and 0.30 mm (0.011 inch) from the terminal tip.
4. The configuration of the pin 1 identifier is optional, but must be located within the zone indicated. The pin 1 identifier may be either a mold or mark feature.
5. Nominal dimensions are provide to assist with printed circuit board land pattern design efforts, see manufacturer’s technical brief TB389.
6. Features and dimensions A2, D1, E1 and S are present when anvil singulation method is used and not present for saw singulation.
7. Falls within JEDEC MO-220VJJB.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	LX
2	LX
3	BOOT
4	$\overline{EN}$
5	VCC5
6	SYNC
7	RTCT
8	SGND
9	FB
10	COMP
11	REF
12	PGOOD
13	PGND
14	SS
15	LX
16	LX
17	V_{IN}
18	V_{IN}
19	V_{IN}
20	V_{IN}

FIGURE 2. Terminal connections.

Terminal symbol	Description
LX	There are four output pins that must be connected together externally in normal operation.
BOOT	A capacitor is connected from this pin to the output pin. An internal 10 V supply and an internal schottky diode provide the high side voltage to drive the gate of the output DMOS device.
$\overline{EN}$	The $\overline{EN}$ input will disable the part and shut down all function when it is held high or left open. The $\overline{EN}$ current will be 10 μA typical. An internal pull up resistor will hold the pin high. When $\overline{EN}$ = low, the part is enabled. Connect to GND for auto start up.
VCC5	VCC5 is the +5.0 V output pin which provides an output of an internal supply for supply filtering purposes. A 1 μF capacitor should be connected from this pin to GND. Internal V_{DD} supply is set at 5.0 V (not planned that the user would use this supply).
SYNC	This pin provides a digital input pin to synchronize the internal oscillator to an external signal. When the sync function is not used, this pin can be left open or tied to GND. If the sync function is used, the RTCT timing must be set to a frequency lower than the sync input frequency. The termination of the ramp is synchronized with the rising edge of the sync input signal. There are no duty cycle restrictions on the input sync signal. Input thresholds are TTL compatible.
RTCT	A resistor to V_{IN} and a capacitor to GND determine the frequency of the saw tooth oscillator. Resistor range, R = 20 kΩ to 100 kΩ. Capacitor range, C = 470 pF to 1.2 nF. The oscillator amplitude will vary from approximately 0.9 V to 10 V as V_{IN} changes from 8.5 V to 60 V to maintain constant frequency and provide feed forward. The oscillator will have a fixed off time, which will establish the maximum on time for the regulator. This off time will be < 200 ns. The maximum duty cycle for a 500 kHz system will therefore be approximately 90% as the frequency of the maximum duty cycle will increase (95% for 25 kHz system). The minimum duty cycle is zero.
SGND	The SGND terminal of the device provides the return path for the control and monitor portions of the integrated circuit.
FB	This is the feedback pin. The feedback ratio is set by an external resistor divider connected to the load.
COMP	This pin is connected to the output of the error amplifier and is used to compensate the loop. The error amplifier is a GM amplifier.
REF	1.20 V reference output. Bypass to GND with 0.01 μF capacitor.
PGOOD	This pin is open drain output that is turned on when the feedback voltage is more than ±10% from the reference voltage, indicating that the output is not within 10% of set point.
PGND	This pin is used as the ground connection of the power train.
SS	A capacitor is connected from this pin to GND to determine the soft start timing. The soft start pin internal charging current is 10 μA.
V_{IN}	The input supply for the pulse width modulator (PWM) regulator power stage. Connected to drain of the high side MOSFET.

FIGURE 2. Terminal connections –continued.

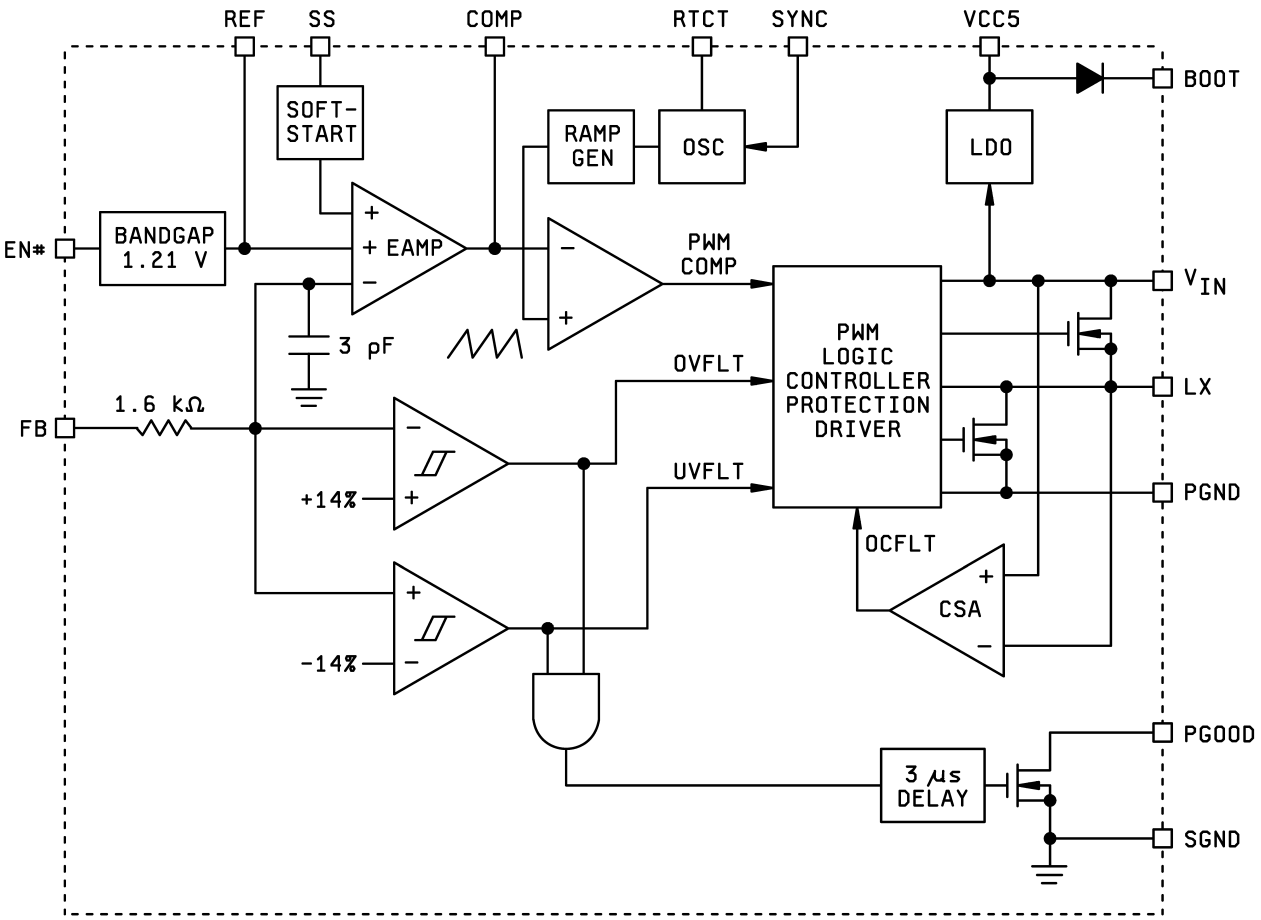


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/08608-01XB	34371	ISL8560MREP 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Add –TK suffix to this vendor part number to order a 1000-piece quantity with tape and reel packing option.

CAGE code	Source of supply
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406