

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct front page title. – PHN	06-08-09	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	13-12-11	Thomas M. Hess
C	JEDEC package MS-013-AA has been updated to MS-013. Add note to Figure 1. Update document paragraphs to current requirements. - ro	19-06-13	C. SAFFLE

**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Vendor item drawing

PMIC N/A	PREPARED BY Phu H. Nguyen		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 06-06-06	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, DIGITAL-LINEAR, CURRENT MODE PWM CONTROLLER, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/06606	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance current mode PWM controller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/06606</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	UC1846-EP	Current mode PWM controller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-013	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/ 2/

Maximum supply voltage (VIN).....	40.0 V
Maximum collector supply voltage (VC)	40.0 V
Output current, source or sink (IO)	500 mA
Analog inputs	-0.3 V to VIN
Maximum reference output current (VREF)	-30 mA
Maximum synchronous output current (SYNC)	-5 mA
Maximum error amplifier output current (COMP)	-5 mA
Maximum soft start sink current (C/S SS)	50 mA
Maximum oscillator charging current (RT)	5 mA
Maximum power dissipation:	
TA = 25°C	1000 mW
TC = 25°C	2000 mW
Storage temperature range (TSTG).....	-65°C to 150°C
Lead temperature (soldering, 10 seconds)	300°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Device life at elevated temperature. The device life at elevated temperature shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Conditions <u>2/</u>	Limits		Unit
		Min	Max	
Reference				
Output voltage	T _J = 25°C, I _O = 1 mA	5.05	5.15	V
Line regulation	V _{IN} = 8 V to 40 V		20	mV
Load regulation	I _L = 1 mA to 10 mA		15	mV
Temperature stability	Over operating range <u>3/</u>	0.4 typical		mV/°C
Total output variation	Line, load, and temperature <u>3/</u>	5.0	5.2	V
Output noise voltage	10 Hz ≤ f ≤ 10 kHz, T _J = 25°C <u>3/</u>	100 typical		μV
Long term stability	T _J = 125°C, 1000 hours	5 typical		mV
Short circuit output current	V _{REF} = 0 V	-10		mA
Oscillator				
Initial accuracy	T _J = 25°C	39	47	kHz
Voltage stability	V _{IN} = 8 V to 40 V		2	%
Temperature stability	Over operating range <u>3/</u>	-1 typical		%
Sync output high level		3.9		V
Sync output low level			2.5	V
Sync input high level	Pin 8 = 0 V	3.9		V
Sync input low level	Pin 8 = 0 V		2.5	V
Sync input current	Sync voltage = 3.9 V, Pin 8 = 0 V		1.5	mA
Error Amplifier				
Input offset voltage			5	mV
Input bias current			-1	μA
Input offset current			250	nA
Common mode range	V _{IN} = 8 V to 40 V	0	V _{IN} - 2	V
Open loop voltage gain	ΔV _O = 1.2 V to 3 V, V _{CM} = 2 V	80		dB
Unity gain bandwidth	T _J = 25°C <u>3/</u>	0.7		MHz
CMRR	V _{CM} = 0 V to 38 V, V _{IN} = 40 V	75		dB
PSRR	V _{IN} = 8 V to 40 V	80		dB
Output sink current	V _{ID} = -15 mV to -5 V, V _{PIN7} = 1.2 V	2		mA
Output source current	V _{ID} = -15 mV to -5 V, V _{PIN7} = 2.5 V	-0.4		mA
High level output voltage	R _L = 15 kΩ (pin 7)	4.3		V
Low level output voltage	R _L = 15 kΩ (pin 7)		1	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Conditions <u>2/</u>	Limits		Unit
		Min	Max	
Current sense amplifier				
Amplifier gain	V _{PIN3} = 0 V, Pin 1 open <u>4/</u> <u>5/</u>	2.5	3	V
Maximum differential input signal (V _{PIN4} – V _{PIN3})	Pin 1 open <u>4/</u> , R _L (pin 7) = 15 kW	1.1		V
Input offset voltage	V _{PIN1} = 0.5 V, Pin 7 open <u>4/</u>		25	mV
CMRR	V _{CM} = 1 V to 12 V	60		dB
PSRR	V _{IN} = 8 V to 40 V	60		dB
Input bias current	V _{PIN1} = 0.5 V, Pin 7 open <u>4/</u>		-10	μA
Input offset current	V _{PIN1} = 0.5 V, Pin 7 open <u>4/</u>		1	μA
Input common mode range		0	V _{IN} - 3	V
Delay to outputs	T _J = 25°C <u>3/</u>		500	ns
Current limit adjust				
Current limit offset	V _{PIN3} = 0 V, V _{PIN4} = 0 V, Pin 7 open <u>4/</u>	0.45	0.55	V
Input bias current	V _{PIN5} = V _{REF} , V _{PIN6} = 0 V		-30	μA
Shutdown terminal				
Threshold voltage		250	400	mV
Input voltage range		0	V _{IN}	V
Minimum, latching current (I _{PIN1}) <u>6/</u>		3		mA
Maximum nonlatching current (I _{PIN1}) <u>7/</u>			0.8	mA
Delay to outputs	T _J = 25°C <u>3/</u>		600	ns
Output				
Collector emitter voltage		40		V
Collector leakage current	V _C = 40 V		200	μA
Output low level	I _{SINK} = 20 mA		0.4	V
	I _{SINK} = 100 mA		2.1	
Output high level	I _{SOURCE} = 20 mA	13		V
	I _{SOURCE} = 100 mA	12		
Rise time	C _L = 1 nF, T _J = 25°C <u>3/</u>		300	ns
Fall time			300	
Undervoltage lockout				
Start up threshold			8	V
Threshold hysteresis		0.75 typical		V
Total standby current				
Supply current			21	mA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $T_A = -55^\circ\text{C}$ to 150°C , $V_{IN} = 15\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 4.7\text{ nF}$, $T_A = T_J$ (unless otherwise noted).

3/ These parameters, although specified over the recommended operating conditions, are not 100% tested in production.

4/ Parameter measured at trip point of latch with $V_{PIN5} = V_{REF}$, $V_{PIN6} = 0\text{ V}$.

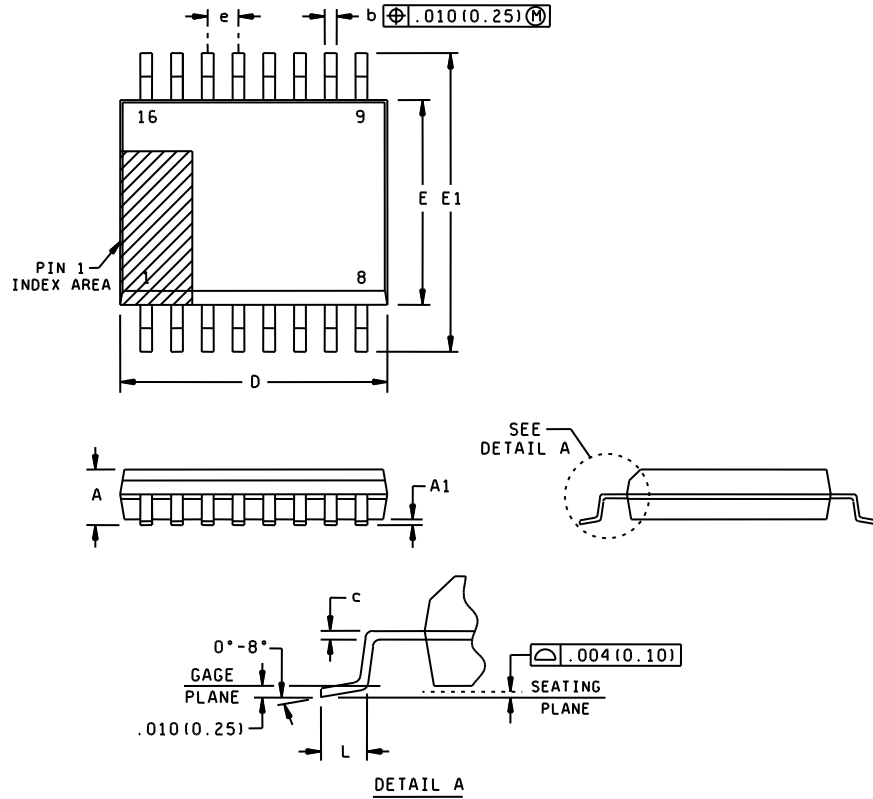
5/ Amplifier gain defined as: $\left(\frac{\Delta V_{PIN7}}{\Delta V_{PIN4}} \right)$ where $V_{PIN4} = 0$ to 1 V.

6/ Current into Pin 1 is ensured to latch circuit in shutdown state.

7/ Current into Pin 1 is ensured not to latch circuit in shutdown state.

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Case X



Dimension									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.104		2.65	E	.291	.299	7.40	7.60
A1	.004	.012	0.10	0.30	E1	.393	.419	9.97	10.63
b	.012	.020	0.31	0.51	e	0.50 NOM		1.27 NOM	
c	.008	.013	0.20	0.33	L	.016	.050	0.40	1.27
D	.398	.413	10.10	10.50					

NOTES:

1. This drawing is subject to change without notice.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
3. For dimension E does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.009 inch) per side.
4. Falls within JEDEC MS-013.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	C/S SS	9	R _T
2	VREF	10	Sync
3	C/S-	11	A Out
4	C/S+	12	GND
5	E/A+	13	V _C
6	E/A-	14	B Out
7	COMP	15	V _{IN}
8	C _T	16	Shutdown

FIGURE 2. Terminal connections.

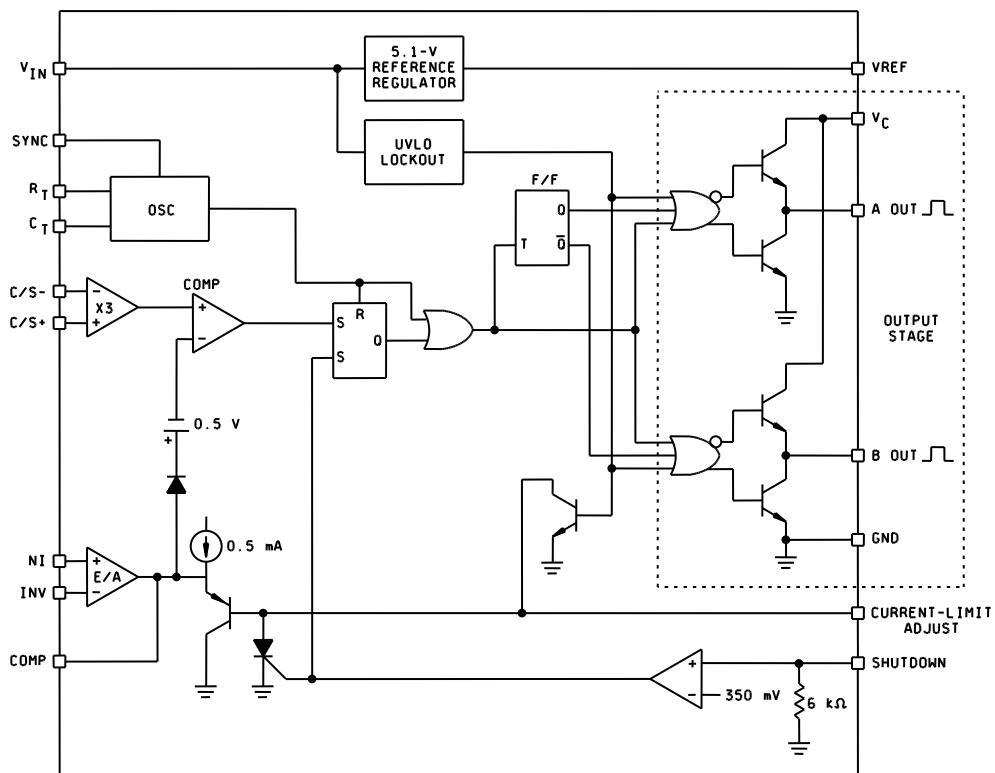


FIGURE 3. Block diagram.

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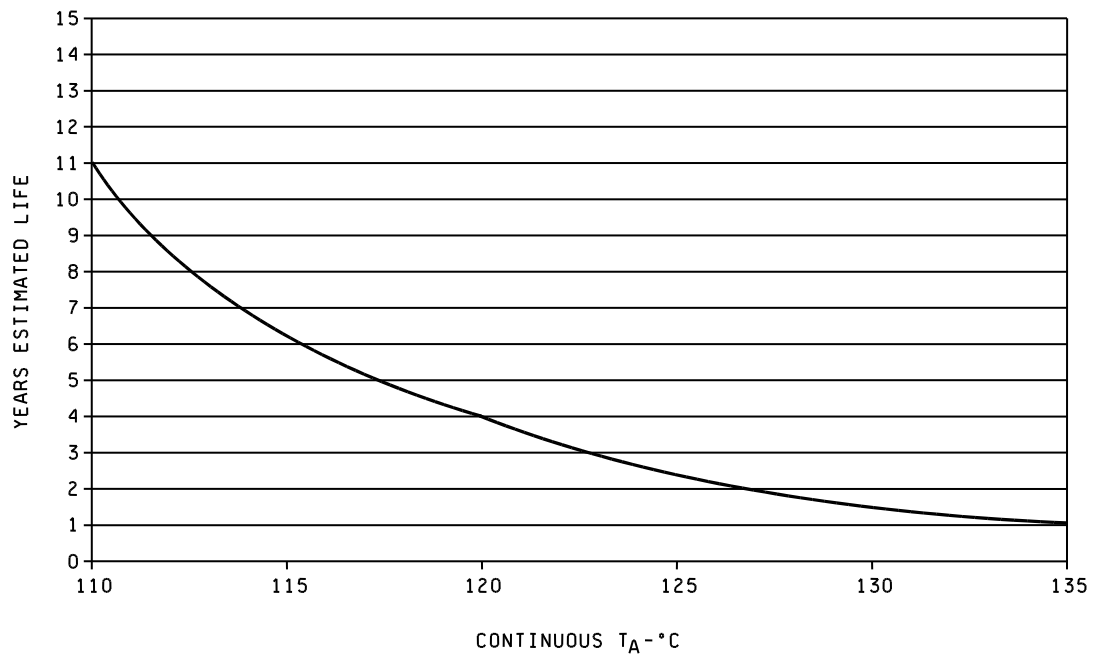


FIGURE 4. Device life at elevated temperature.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/06606-01XE	01295	UC1846MDWREP	UC1846MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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