

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make a correction under paragraph 6.3 to change the lead finish from "A" to "E". Add a footnote under Table I and two notes under figure 1. Add paragraph 1.5. Make changes to CMRR and I _{DD} (SHDN) tests under the conditions column. - ro	05-10-11	R. MONNIN
B	Add device types 06 and 07. Add case outline Z. - ro	05-11-01	R. MONNIN
C	Update document to current requirements. - ro	14-06-05	C. SAFFLE
D	Case X JEDEC package MS-012 has been updated to MS-012-AA along with b, c, and L dimensions. Case Y JEDEC package MS-012 has been updated to MS-012-AB along with b, c, and L dimensions. Add notes to all case outlines under Figure 1. Update document paragraphs to current requirements. - ro	19-09-10	J. ESCHMEYER



**CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990**

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES			REV		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
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PMIC N/A	PREPARED BY RICK OFFICER		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 03-01-28	CHECKED BY TOM HESS		TITLE MICROCIRCUIT, LINEAR, LOW POWER, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03619	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power operational amplifier microcircuit, with an operating temperature range of -40°C to +125°C for device types 01, 02, 03, 04, 05 and -55°C to +125°C for device types 06 and 07.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03619</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TLV2460AQ-EP 1/	Low power operational amplifier with shutdown mode
02	TLV2461AQ-EP 1/	Low power operational amplifier
03	TLV2462AQ-EP	Dual, low power operational amplifier
04	TLV2463AQ-EP	Dual, low power operational amplifier with shutdown mode
05	TLV2464AQ-EP 1/	Quad, low power operational amplifier
06	TLV2462AM-EP	Dual, low power operational amplifier
07	TLV2464AM-EP	Quad, low power operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Plastic small outline
Y	14	MS-012-AB	Plastic small outline
Z	14	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1/ Not yet available from a source of supply.

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1.3 Absolute maximum ratings. 2/

Supply voltage (+V _{DD})	+6 V dc 3/
Differential input voltage (V _{ID})	-0.2 V to V _{DD} + 0.2 V
Input current (I _I) (any input)	±200 mA
Output current (I _O)	±175 mA
Total input current (I _I) (into +V _{DD})	175 mA
Total output current (I _O) (out of GND)	175 mA
Continuous total power dissipation T _A ≤ +25°C	
Case X	710 mW
Case Y	1022 mW
Maximum junction temperature (T _J)	+150°C
Storage temperature range (T _{stg})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction-to-case (θ _{JC}):	See dissipation rating table 4/
Thermal resistance, junction-to-ambient (θ _{JA}):	See dissipation rating table 4/

1.4 Recommended operating conditions. 5/

Supply voltage (V _{DD}):	
Single supply	2.7 V dc minimum to 6 V dc maximum
Split supply	±1.35 V dc minimum to ±3 V dc maximum
Common mode input voltage range (V _{ICR})	-0.2 V minimum to +V _{DD} + 0.2 V dc maximum
Shutdown on/off voltage level: 6/	
V _{IH}	2 V minimum
V _{IL}	0.7 V maximum
Operating free-air temperature (T _A)	
Device types 01, 02, 03, 04, and 05	-40°C minimum to +125°C maximum
Device types 06 and 07	-55°C minimum to +125°C maximum

1.5 Dissipation rating table. 7/

Package	θ _{JC}		θ _{JA} 0 air flow		Units
	High K	Low K	High K	Low K	
X	39.4	42.4	97.1	165.5	°C/W
Y	51.5	53.7	86.2	133.5	°C/W
Z	45.8	46.6	111.7	131.4	°C/W

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ All voltage values, except differential voltages, are with respect to GND.

4/ Thermal resistances are not production tested and are for informational purposes only.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ Relative to voltage on the GND terminal of the device.

7/ High K specifies a high thermal conductivity printed circuit board used to measure theta parameters.
Low K specifies a low thermal conductivity printed circuit board used to measure theta parameters.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V _{IO}	V _{DD} = 3 V, V _{IC} = 1.5 V, V _O = 1.5 V, R _S = 50 Ω	25°C	All		1500	μV
			-40°C to +125°C	01 - 05		1700	
			-55°C to +125°C	06, 07		1700	
		V _{DD} = 5 V, V _{IC} = 2.5 V, V _O = 2.5 V, R _S = 50 Ω	25°C	All		1500	
			-40°C to +125°C	01 - 05		1700	
			-55°C to +125°C	06, 07		1700	
Temperature coefficient of input offset voltage	αV _{IO}	V _{DD} = 3 V, V _{IC} = 1.5 V, V _O = 1.5 V, R _S = 50 Ω	25°C	All	2 typical		μV/°C
		V _{DD} = 5 V, V _{IC} = 2.5 V, V _O = 2.5 V, R _S = 50 Ω			2 typical		
Input offset current	I _{IO}	V _{DD} = 3 V, V _{IC} = 1.5 V, V _O = 1.5 V, R _S = 50 Ω	25°C	All		7	nA
			-40°C to +125°C	01 - 05		75	
			-55°C to +125°C	06, 07		75	
		V _{DD} = 5 V, V _{IC} = 2.5 V, V _O = 2.5 V, R _S = 50 Ω	25°C	All		7	
			-40°C to +125°C	01 - 05		60	
			-55°C to +125°C	06, 07		60	
Input bias current	I _{IB}	V _{DD} = 3 V, V _{IC} = 1.5 V, V _O = 1.5 V, R _S = 50 Ω	25°C	All		14	nA
			-40°C to +125°C	01 - 05		75	
			-55°C to +125°C	06, 07		75	
		V _{DD} = 5 V, V _{IC} = 2.5 V, V _O = 2.5 V, R _S = 50 Ω	25°C	All		14	
			-40°C to +125°C	01 - 05		60	
			-55°C to +125°C	06, 07		60	

See footnote at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{DD} = 3 V, I _{OH} = -2.5 mA	25°C	All	2.9 typical		V
			-40°C to +125°C	01 - 05	2.8		
			-55°C to +125°C	06, 07	2.8		
		V _{DD} = 3 V, I _{OH} = -10 mA	25°C	All	2.7 typical		
			-40°C to +125°C	01 - 05	2.5		
			-55°C to +125°C	06, 07	2.5		
		V _{DD} = 5 V, I _{OH} = -2.5 mA	25°C	All	4.9 typical		
			-40°C to +125°C	01 - 05	4.8		
			-55°C to +125°C	06, 07	4.8		
		V _{DD} = 5 V, I _{OH} = -10 mA	25°C	All	4.8 typical		
			-40°C to +125°C	01 - 05	4.7		
			-55°C to +125°C	06, 07	4.7		
Low level output voltage	V _{OL}	V _{DD} = 3 V, V _{IC} = 1.5 V, I _{OL} = 2.5 mA	25°C	All	0.1 typical		V
			-40°C to +125°C	01 - 05		0.2	
			-55°C to +125°C	06, 07		0.2	
		V _{DD} = 3 V, V _{IC} = 1.5 V, I _{OL} = 10 mA	25°C	All	0.3 typical		
			-40°C to +125°C	01 - 05		0.5	
			-55°C to +125°C	06, 07		0.5	
		V _{DD} = 5 V, V _{IC} = 2.5 V, I _{OL} = 2.5 mA	25°C	All	0.1 typical		
			-40°C to +125°C	01 - 05		0.2	
			-55°C to +125°C	06, 07		0.2	
		V _{DD} = 5 V, V _{IC} = 2.5 V, I _{OL} = 10 mA	25°C	All	0.2 typical		
			-40°C to +125°C	01 - 05		0.3	
			-55°C to +125°C	06, 07		0.3	

See footnote at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Short circuit output current	I _{OS}	V _{DD} = 3 V, sourcing	25°C	All	50 typical		mA
			-40°C to +125°C	01 - 05	20		
			-55°C to +125°C	06, 07	20		
		V _{DD} = 3 V, sinking	25°C	All	40 typical		
			-40°C to +125°C	01 - 05	20		
			-55°C to +125°C	06, 07	20		
		V _{DD} = 5 V, sourcing	25°C	All	145 typical		
			-40°C to +125°C	01 - 05	60		
			-55°C to +125°C	06, 07	60		
		V _{DD} = 5 V, sinking	25°C	All	100 typical		
			-40°C to +125°C	01 - 05	60		
			-55°C to +125°C	06, 07	60		
Output current	I _O	V _{DD} = 3 V, measured 1 V from rail	25°C	All	±40 typical		mA
		V _{DD} = 5 V, measured 1 V from rail			±80 typical		
Large signal differential voltage amplification	A _{VD}	V _{DD} = 3 V, R _L = 10 kΩ	25°C	All	90		dB
			-40°C to +125°C	01 - 05	89		
			-55°C to +125°C	06, 07	89		
		V _{DD} = 5 V, R _L = 10 kΩ, V _{IC} = 2.5 V, V _O = 1 V to 4 V	25°C	All	92		
			-40°C to +125°C	01 - 05	90		
			-55°C to +125°C	06, 07	90		
Differential input resistance	r _{i(d)}	V _{DD} = 3 V	25°C	All	10 ⁹ typical		Ω
		V _{DD} = 5 V			10 ⁹ typical		
Common mode input capacitance	C _{i(c)}	V _{DD} = 3 V, f = 10 kHz	25°C	All	7 typical		pF
		V _{DD} = 5 V, f = 10 kHz			7 typical		

See footnote at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Closed loop output impedance	z _o	V _{DD} = 3 V, f = 100 kHz, A _V = 10	25°C	All	33 typical		Ω
		V _{DD} = 5 V, f = 100 kHz, A _V = 10			29 typical		
Common mode rejection ratio	CMRR	V _{DD} = 3 V, R _S = 50 Ω, V _{ICR} = 0 V to 3V	25°C	All	66		dB
			-40°C to +125°C	01 - 05	60		
			-55°C to +125°C	06, 07	60		
		V _{DD} = 5 V, R _S = 50 Ω, V _{ICR} = 0 V to 5 V	25°C	All	71		
			-40°C to +125°C	01 - 05	60		
			-55°C to +125°C	06, 07	60		
Supply voltage rejection ratio (ΔV _{DD} / ΔV _{IO})	k _{SVR}	V _{DD} = 2.7 V to 6 V, no load, V _{IC} = V _{DD} / 2	25°C	All	80		dB
			-40°C to +125°C	01 - 05	75		
			-55°C to +125°C	06, 07	75		
		V _{DD} = 3 V to 5 V, no load, V _{IC} = V _{DD} / 2	25°C	All	85		
			-40°C to +125°C	01 - 05	80		
			-55°C to +125°C	06, 07	80		
Supply current (per channels)	I _{DD}	V _{DD} = 3 V, V _O = 1.5 V, no load	25°C	All		0.575	mA
			-40°C to +125°C	01 - 05		0.9	
			-55°C to +125°C	06, 07		0.9	
		V _{DD} = 5 V, V _O = 2.5 V, no load	25°C	All		0.65	
			-40°C to +125°C	01 - 05		1	
			-55°C to +125°C	06, 07		1	
Supply current in shutdown	I _{DD} (SHDN)	V _{DD} = 3 V, $\overline{\text{SHDN}}$ < 0.7 V, per channel in shutdown	25°C	01,04	0.3 typical		μA
			-40°C to +125°C			2.5	
		V _{DD} = 5 V, $\overline{\text{SHDN}}$ < 0.7 V, per channels in shutdown	25°C		1 typical		
			-40°C to +125°C			3	

See footnote at end of table.

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See footnote at end of table.

Test	Symbol	Conditions	Temperature, TA	Device type	Limits		Unit	
Slew rate at unity gain	SR	VDD = 3 V, VO(PP) = 2 V, CL = 160 pF, RL = 10 kΩ	25°C	All	1	Min	V/μs	
					0.8	Max		
					0.8			
					1			
					0.8			
					0.8			
Equivalent input noise voltage	Vn	VDD = 3 V, f = 100 Hz	25°C	All	16 typical		nV / √Hz	
					11 typical			
					14 typical			
					11 typical			
					11 typical			
					11 typical			
Equivalent input noise current	In	VDD = 3 V, f = 1 kHz	25°C	All	0.13 typical		pA / √Hz	
					0.13 typical			
					0.13 typical			
					0.13 typical			
Total harmonic distortion plus noise	THD + N	VDD = 3 V, VO(PP) = 2 V, RL = 10 kΩ, f = 1 kHz	25°C	All	0.006 % typical			
					0.02 % typical			
					0.08 % typical			
		0.004 % typical						
		0.01 % typical						
		0.04 % typical						
	N	VDD = 5 V, VO(PP) = 4 V, RL = 10 kΩ, f = 10 kHz	25°C	All	7.6 typical			
					7.65 typical			
Amplifier turn on time	t(on)	VDD = 3 V, AV = 1, RL = 10 kΩ	25°C	All			μs	
		Both channels			Channel 1 only, Channel 2 on			

TABLE I. Electrical performance characteristics – continued. 1/

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions		Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Amplifier turn on time	t _(on)	V _{DD} = 5 V,	Both channels	25°C	All	7.6 typical		μs
		A _V = 1,	Channel 1 only, Channel 2 on			7.65 typical		
		R _L = 10 kΩ	Channel 2 only, Channel 1 on			7.25 typical		
Amplifier turn off time	t _(off)	V _{DD} = 3 V,	Both channels	25°C	All	333 typical		ns
		A _V = 1,	Channel 1 only, Channel 2 on			328 typical		
		R _L = 10 kΩ	Channel 2 only, Channel 1 on			329 typical		
		V _{DD} = 5 V,	Both channels			333 typical		
		A _V = 1,	Channel 1 only, Channel 2 on			328 typical		
		R _L = 10 kΩ	Channel 2 only, Channel 1 on			329 typical		
Gain bandwidth product	GBWP	V _{DD} = 3 V, f = 10 kHz, C _L = 160 pF, R _L = 10 kΩ		25°C	All	5.2 typical		MHz
		V _{DD} = 5 V, f = 10 kHz, C _L = 160 pF, R _L = 10 kΩ				6.4 typical		
Settling time	t _s	V _{DD} = 3 V, A _V = -1,	0.1 %	25°C	All	1.47 typical		μs
		V _{(STEP)PP} = 2 V, C _L = 10 pF, R _L = 10 kΩ	0.01 %			1.78 typical		
		V _{DD} = 3 V, A _V = -1,	0.1 %			1.77 typical		
		V _{(STEP)PP} = 2 V, C _L = 56 pF, R _L = 10 kΩ	0.01 %			1.98 typical		

See footnote at end of table.

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TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions		Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Settling time	t _s	V _{DD} = 5 V, A _V = -1,	0.1 %	25°C	All	1.53 typical		μs
		V _{(STEP)PP} = 2 V, C _L = 10 pF, R _L = 10 kΩ	0.01 %			1.83 typical		
		V _{DD} = 5 V, A _V = -1,	0.1 %			3.13 typical		
		V _{(STEP)PP} = 2 V, C _L = 56 pF, R _L = 10 kΩ	0.01 %			3.33 typical		
Phase margin at unity gain	φ _m	V _{DD} = 3 V, C _L = 160 pF, R _L = 10 kΩ		25°C	All	44° typical		
		V _{DD} = 5 V, C _L = 160 pF, R _L = 10 kΩ				45° typical		
Gain margin		V _{DD} = 3 V, C _L = 160 pF, R _L = 10 kΩ		25°C	All	7 typical		dB
		V _{DD} = 5 V, C _L = 160 pF, R _L = 10 kΩ				7 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X

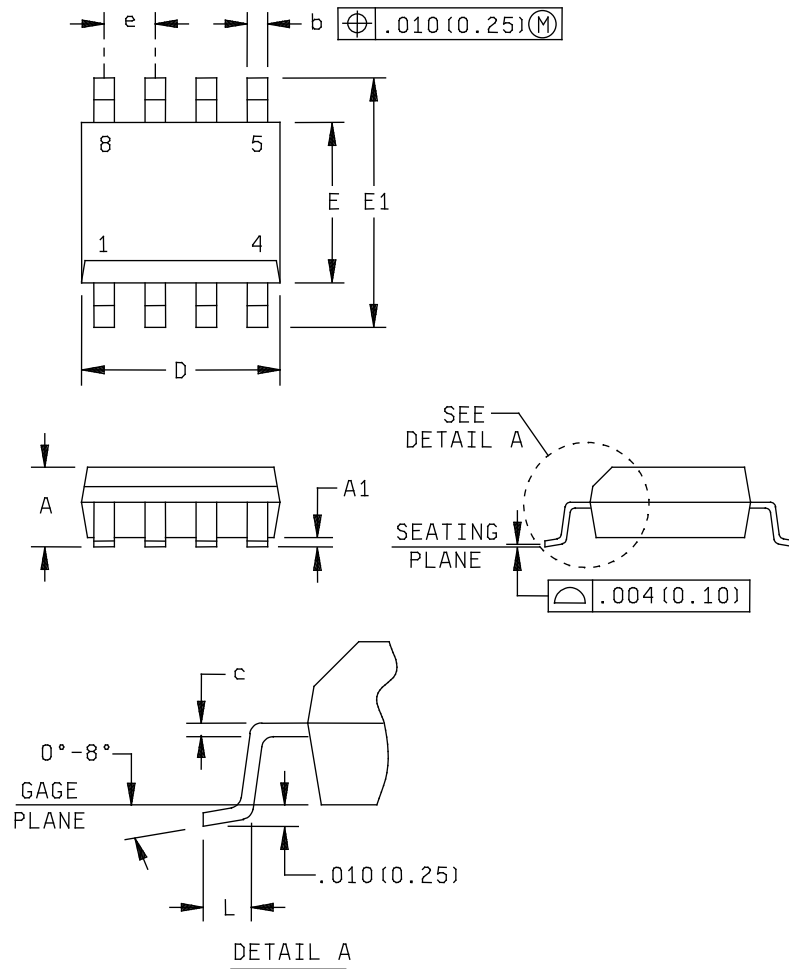


FIGURE 1. Case outlines.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.11	0.25
b	0.012	0.020	0.31	0.51
c	0.010 nominal		0.25 nominal	
D	0.189	0.197	4.81	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.81	3.98
E1	0.228	0.244	5.80	6.19
L	0.016	0.050	0.40	1.27
n	8 leads		8 leads	

NOTE:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. The E dimension does not include interlead flash.
4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outlines. – continued.

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Case Y

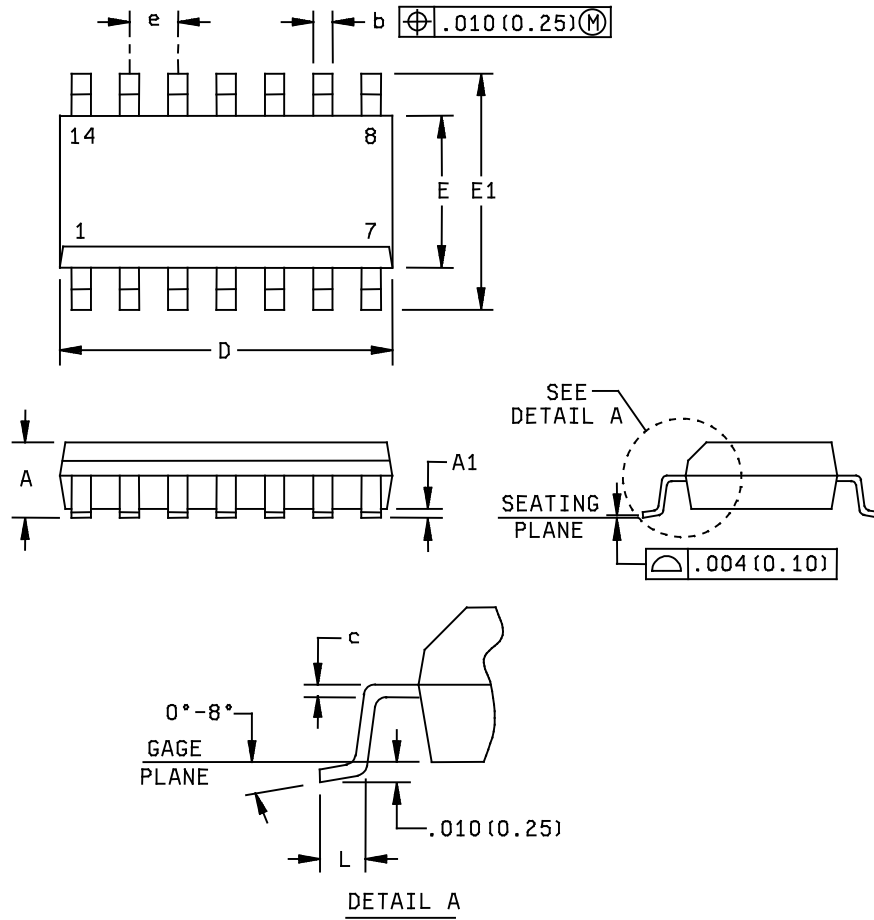


FIGURE 1. Case outlines – continued.

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Case Y – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.337	0.344	8.55	8.75
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
n	14 leads		14 leads	

NOTE:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls with JEDEC MS-012-AB.

FIGURE 1. Case outlines. – continued.

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Case Z

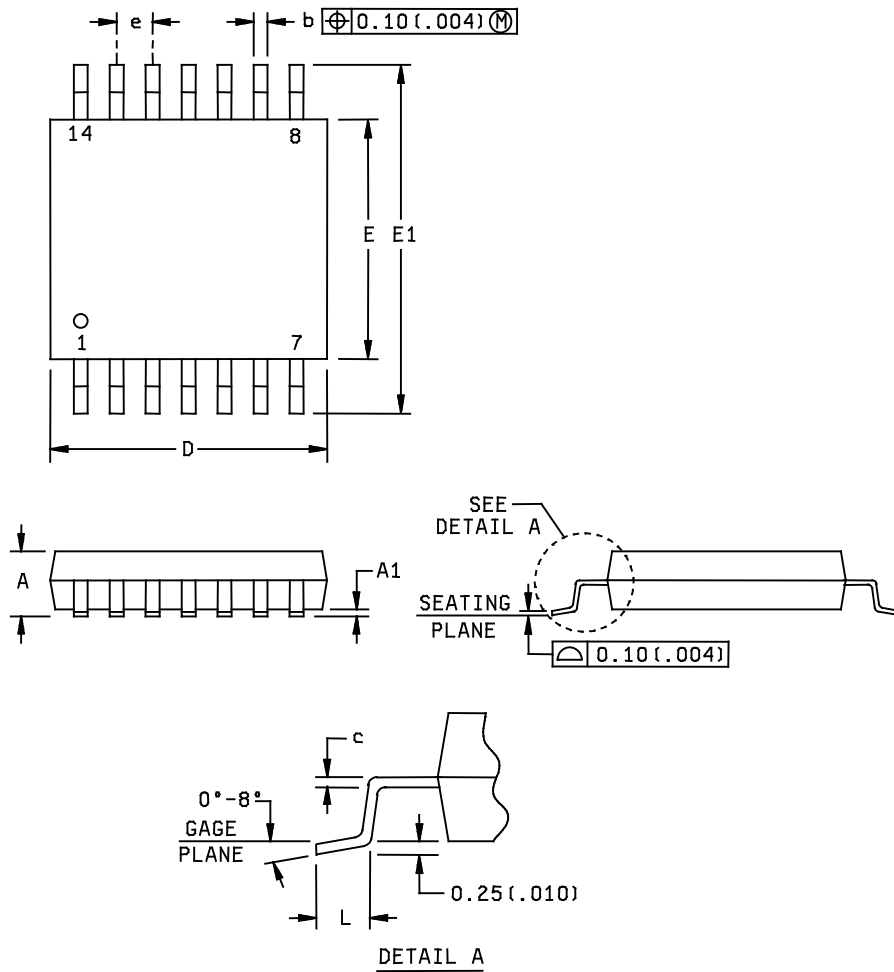


FIGURE 1. Case outlines - Continued.

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Case Z – continued.

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		1.20		.047
A1	0.05	0.15	.002	.006
b	0.19	0.30	.007	.012
c	0.15 nominal		.006 nominal	
D	4.90	5.10	.193	.201
E	4.30	4.50	.169	.177
E1	6.20	6.60	.244	.260
e	0.65 BSC		.026 BSC	
L	0.50	0.75	.020	.030

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) each end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 mm (0.010 inch) each side.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

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Device types	01	02	03, 06	04	05, 07	07
Case outlines	X	X	X	Y	Y	Z
Terminal number	Terminal symbol					
1	NC	NC	1 OUT	1 OUT	1 OUT	1 OUT
2	-IN	-IN	1 -IN	1 -IN	1 -IN	1 -IN
3	+IN	+IN	1 +IN	1 +IN	1 +IN	1 +IN
4	GND	GND	GND	GND	+V _{DD}	+V _{DD}
5	NC	NC	2 +IN	NC	2 +IN	2 +IN
6	OUT	OUT	2 -IN	$\overline{1 \text{ SHDN}}$	2 -IN	2 -IN
7	+V _{DD}	+V _{DD}	2 OUT	NC	2 OUT	2 OUT
8	$\overline{\text{SHDN}}$	NC	+V _{DD}	NC	3 OUT	3 OUT
9	---	---	---	$\overline{2 \text{ SHDN}}$	3 -IN	3 -IN
10	---	---	---	NC	3 +IN	3 +IN
11	---	---	---	2 +IN	GND	GND
12	---	---	---	2 -IN	4 +IN	4 +IN
13	---	---	---	2 OUT	4 -IN	4 -IN
14	---	---	---	+V _{DD}	4 OUT	4 OUT

NC = No internal connection

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/03619-01XE	01295		<u>2/</u>
V62/03619-02XE	01295		<u>2/</u>
V62/03619-03XE	01295	2462AE	TLV2462AQDREP
V62/03619-04YE	01295	V2463AQE	TLV2463AQDREP
V62/03619-05YE	01295		<u>2/</u>
V62/03619-06XE	01295	2462AM	TLV2462AMDREP
V62/03619-07YE	01295	V2464AME	TLV2464AMDREP
V62/03619-07ZE	01295	2464AME	TLV2464AMPWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Not yet available from a source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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