

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12-bit parallel digital to analog converter with power down microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03615</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TLV5619-EP	12-bit parallel digital to analog converter with power down

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MS-013	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD} to GND).....	7 V
Analog input voltage range	-0.3 V to $V_{DD} + 0.3$ V
Reference input voltage	$V_{DD} + 0.3$ V
Digital input voltage range to GND	-0.3 V to $V_{DD} + 0.3$ V
Storage temperature range (T_{STG})	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction to case (θ_{JC})	29.8°C/W

1.4 Recommended operating conditions. 2/

Supply voltage (V_{DD})	
5 V supply	4.5 V dc to 5.5 V dc
3 V supply	2.7 V dc to 3.3 V dc
High-level digital input voltage, (V_{IH}):	
With $V_{DD} = 2.7$ V	2.0 V dc minimum <u>3/</u>
With $V_{DD} = 5.5$ V	2.4 V dc minimum <u>3/</u>
Low-level digital input voltage, (V_{IL}):	
With $V_{DD} = 2.7$ V	0.6 V dc maximum <u>3/</u>
With $V_{DD} = 5.5$ V	0.8 V dc minimum <u>3/</u>
Reference voltage,	
V_{ref} to REFIN pin, 5 V supply	0 V to $V_{DD} - 1.5$ V <u>4/</u>
V_{ref} to REFIN pin, 3 V supply	0 V to $V_{DD} - 1.5$ V <u>4/</u>
Load resistance (R_L)	2 k Ω
Load capacitance (C_L)	100 pF
Operating free-air temperature range (T_A)	-40°C to +125°C

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 3/ The recommended operating levels for both V_{IH} and V_{IL} apply to all values of V_{DD} .
- 4/ Reference input voltages greater than $V_{DD} / 2$ will cause output saturation for large DAC codes.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4 .

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -40°C ≤ T _A ≤ +125°C	Device type	Limits		Unit
				Min	Max	
Static DAC specification section						
Resolution	RES	V _{ref} (REFIN) = 2.048 V at 5 V, V _{ref} (REFIN) = 1.024 V at 3 V	01	12		Bits
Integral nonlinearity	INL	V _{ref} (REFIN) = 2.048 V at 5 V, <u>1/</u> V _{ref} (REFIN) = 1.024 V at 3 V			±4	LSB
Differential nonlinearity	DNL	V _{ref} (REFIN) = 2.048 V at 5 V, <u>2/</u> V _{ref} (REFIN) = 1.024 V at 3 V			±1	LSB
Zero scale error (offset error at zero scale)	EZS	V _{ref} (REFIN) = 2.048 V at 5 V, <u>3/</u> V _{ref} (REFIN) = 1.024 V at 3 V			±20	mV
Zero scale error temperature coefficient		V _{ref} (REFIN) = 2.048 V at 5 V, <u>4/</u> V _{ref} (REFIN) = 1.024 V at 3 V		3 typical		ppm/°C
Gain error	EG	V _{ref} (REFIN) = 2.048 V at 5 V, <u>5/</u> V _{ref} (REFIN) = 1.024 V at 3 V			±0.5	% of FS voltage
Gain error temperature coefficient	EG	V _{ref} (REFIN) = 2.048 V at 5 V, <u>6/</u> V _{ref} (REFIN) = 1.024 V at 3 V		1 typical		ppm/°C
Power supply rejection ratio	PSRR	Zero scale <u>7/</u> , <u>8/</u>		65 typical		dB
		Gain <u>7/</u> , <u>8/</u>	65 typical			
Output specifications section						
Voltage output range	V _O	R _L = 10 kΩ	01	0	V _{DD} – 0.4	V
Output load regulation accuracy		V _O (OUT) = 4.096, 2.048 V, R _L = 2 kΩ			0.29	% of FS voltage
Output short circuit source current	I _{OSC} (source)	5 V supply, V _O (OUT) = 0 V, full scale code		100 typical		mA
		3 V supply, V _O (OUT) = 0 V, full scale code		25 typical		
Output source current	I _O (source)	5 V supply, R _L = 100 Ω		10 typical		mA
		3 V supply, R _L = 100 Ω		10 typical		

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 5

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -40°C ≤ T _A ≤ +125°C	Device type	Limits		Unit
				Min	Max	
Reference input (REFIN) section						
Reference input voltage	V _{ref}	<u>9/</u>	01	0	V _{DD} – 1.5	V
Reference input resistance	R _I			10 typical		MΩ
Reference input capacitance	C _I			5 typical		pF
Reference feed through		REFIN = 1 V _{PP} at 1 kHz + 1.024 V dc <u>10/</u>		-60 typical		dB
Reference input bandwidth		REFIN = 0.2 V _{PP} + 1.024 V dc at –3 dB		1.4 typical		MHz
Digital inputs section (D0 – D11, $\overline{\text{CS}}$, $\overline{\text{WE}}$, $\overline{\text{LDAC}}$, $\overline{\text{PD}}$) section						
High level digital input current	I _{IH}	V _I = V _{DD}	01		1	μA
Low level digital input current	I _{IL}	V _I = 0 V			-1	μA
Input capacitance	C _I			8 typical		pF
Power supply section						
Power supply current	I _{DD}	5 V supply, no load, all inputs 0 V or V _{DD}	01		3	mA
		3 V supply, no load, all inputs 0 V or V _{DD}			2.7	
Power down supply current						10
Analog output dynamic performance section						
Slew rate	SR	5 V supply, V _{ref} (REFIN) = 2.048, 1.024 V, V _O from 10% to 90%, 90% to 10% C _L = 100 pF, R _L = 10 kΩ, code 32 to code 4095, code 4095 to code 32		8		V/μs
		3 V supply, V _{ref} (REFIN) = 2.048, 1.024 V, V _O from 10% to 90%, 90% to 10% C _L = 100 pF, R _L = 10 kΩ, code 32 to code 4095, code 4095 to code 32		6		
Output settling time (full scale)	t _s	To ±0.5 LSB, R _L = 10 kΩ, C _L = 100 pF <u>11/</u>			3	μs
Glitch energy		DIN = all 0s to all 1s		5 typical		nV-s
Signal to noise	S/N	5 V supply, f _s = 480 kSPS, f _{OUT} = 1 kHz, R _L = 10 kΩ, C _L = 100 pF, BW = 20 kHz, T _A = 25°C <u>12/</u>		65		dB

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 6

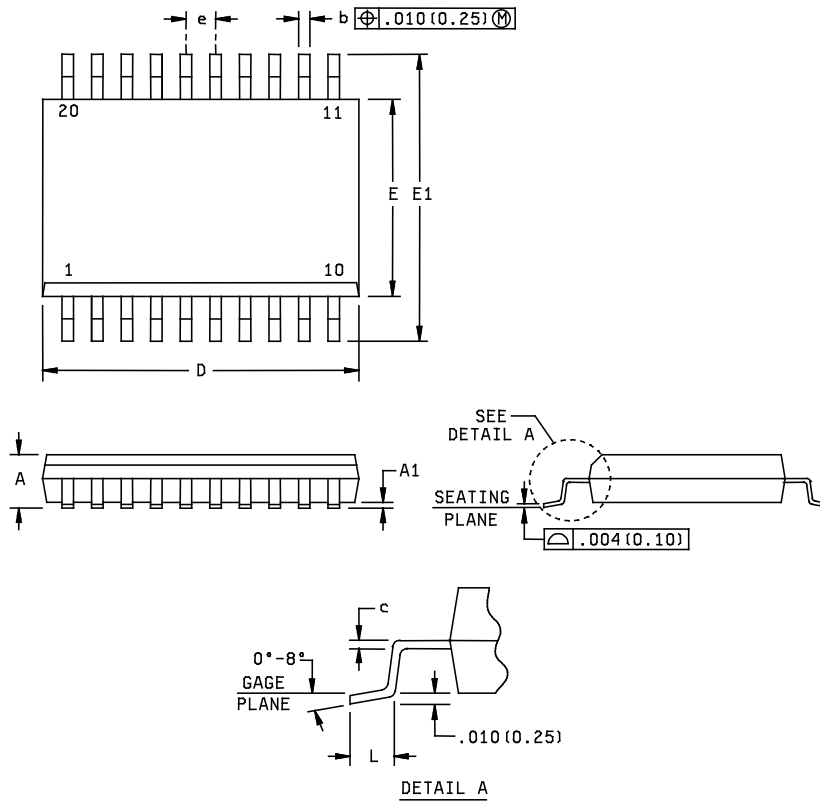
TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions -40°C ≤ T _A ≤ +125°C	Device type	Limits		Unit		
				Min	Max			
Analog output dynamic performance section								
Signal to noise + distortion	S /(N+D)	f _S = 480 kSPS, f _{OUT} = 1 kHz, R _L = 10 kΩ, C _L = 100 pF, BW = 20 kHz, T _A = 25°C <u>12/</u>	5 V supply	01	58	dB		
			3 V supply		58			
Total harmonic distortion							-60	dB
Spurious free dynamic range							60	dB
Digital inputs section								
Setup time, $\overline{CS}$ low before positive $\overline{WE}$ edge	t _{su} (CS-WE)		01	13		ns		
Setup time, data ready before positive $\overline{WE}$ edge	t _{su} (D)			9				
Hold time, data held after positive $\overline{WE}$ edge	t _h (D)			0				
Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	t _{su} (WE-LD)			0				
Pulse width, $\overline{WE}$ high	t _{wh} (WE)			25				
Pulse width, $\overline{LDAC}$ low	t _w (LD)			25				

- 1/ The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code full-scale errors.
- 2/ The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
- 3/ Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
- 4/ Zero-scale error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.
- 5/ Gain error is the deviation from the ideal output (2 x V_{ref} – 1 LSB) within output load 10 kΩ excluding the effects of the zero error.
- 6/ Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.
- 7/ Zero scale error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero code output voltage.
- 8/ Gain error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full scale output voltage after subtracting the zero scale change.
- 9/ Reference input voltages greater than V_{DD} / 2 will cause output saturation for large DAC codes.
- 10/ Reference feedthrough is measured at the DAC output with an input code = 0x000 and a V_{ref}(REFIN) input = 1.024 V dc + 1 V_{pp} at 1 kHz.
- 11/ Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0x3DF or 0x3DF to 0x020. Limits are ensured by design and characterization, but are not production tested.
- 12/ 1 kHz sinewave generated by DAC, reference voltage = 1.024 V at 3 V and 2.048 V at 5 V.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 7

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.104		2.65	E	0.293	0.299	7.45	7.59
A1	0.004	0.012	0.10	0.30	E1	0.400	0.419	10.15	10.65
b	0.014	0.020	0.35	0.51	e	0.050		1.27	
c	0.010 nominal		0.25 nominal		L	0.016	0.050	0.40	1.27
D	0.500	0.510	12.70	12.95	n	20 leads		20 leads	

NOTE:

1. Body dimensions do not include mold flash or protrusion.

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 8

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D2	11	V _{DD}
2	D3	12	REFIN
3	D4	13	OUT
4	D5	14	GND
5	D6	15	$\overline{\text{PD}}$
6	D7	16	$\overline{\text{LDAC}}$
7	D8	17	$\overline{\text{WE}}$
8	D9	18	$\overline{\text{CS}}$
9	D10	19	D0
10	D11	20	D1

Terminal symbol	I/O	Description
$\overline{\text{CS}}$	I	Chip select
D0 (LSB) – D11 (MSB)	I	Parallel data input
GND		Ground
$\overline{\text{LDAC}}$	I	Load DAC
OUT	O	Analog output
$\overline{\text{PD}}$	I	When low, disables all buffer amplifier voltages to reduce supply current
REFIN	I	Voltage reference input
V _{DD}		Positive power supply
$\overline{\text{WE}}$	I	Write enable

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 9

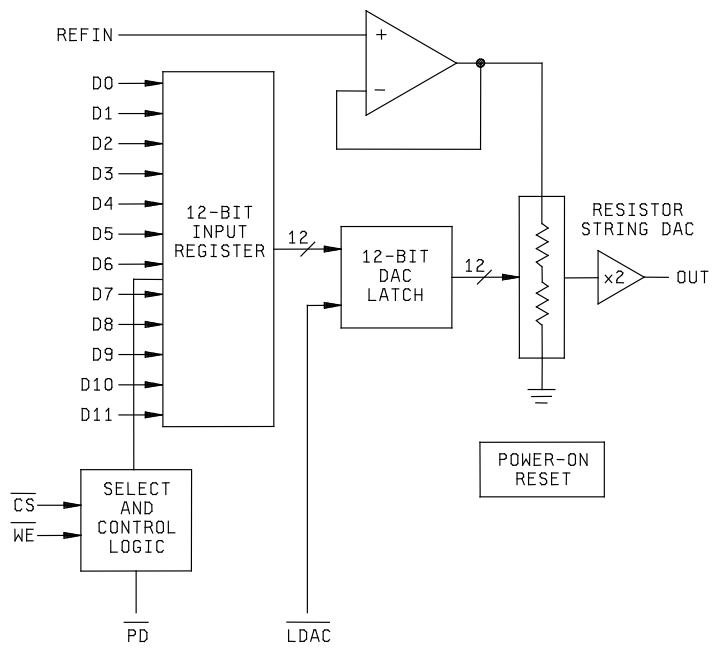


FIGURE 3. Block diagram.

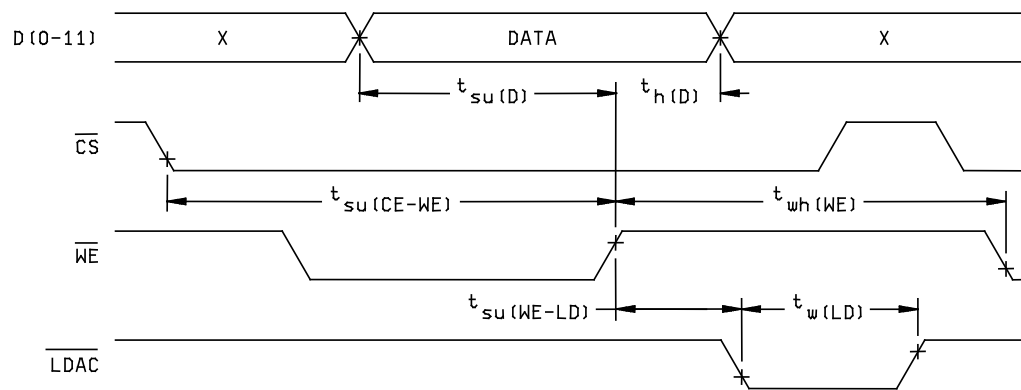


FIGURE 4. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 10

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03615-01XE	01295	TLV5619QDWREP	TLV5619QEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03615
		REV C	PAGE 11