

REVISIONS																					
LTR	DESCRIPTION														DATE (YR-MO-DA)				APPROVED		
A	Update boilerplate to current revision. - CFS														07-09-12				Thomas M. Hess		
B	Add devive type 02 - CFS														08-07-15				Thomas M. Hess		
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN														14-12-22				Thomas M. Hess		
D	Update boilerplate paragraphs to current VID description requirements. - PHN														22-04-26				Muhammad A. Akbar		

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

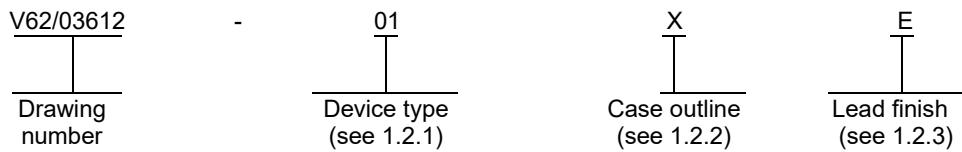
Revision Status of Sheets																					
REV																					
SHEET																					
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15						

PMIC N/A Original date of drawing YY MM DD 02-12-12	PREPARED BY Charles F. Saffle				DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990																
	CHECKED BY Thomas M. Hess				TITLE MICROCIRCUIT, DIGITAL, CMOS, THREE-PORT CABLE TRANSCEIVER/ARBITER, MONOLITHIC SILICON																
	APPROVED BY Thomas M. Hess																				
	SIZE A		CAGE CODE 16236		DWG NO. V62/03612																
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Three-Port Cable Transceiver/Arbiter microcircuit, with an operating temperature range of -40°C to +85°C for device type 01, and an operating temperature range of -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TSB41AB3-EP	Three-Port Cable Transceiver/Arbiter
02	TSB41AB3-EP	Three-Port Cable Transceiver/Arbiter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	80	JEDEC MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V to +4.0 V <u>2/</u>
Input voltage range (V_I)	-0.5 V to $V_{DD} + 0.5$ V <u>2/</u>
5 V tolerant I/O supply voltage range ($V_{DD(5V)}$)	-0.3 V to +5.5 V
5 V tolerant input voltage range ($V_{I(5V)}$)	-0.5 V to $V_{DD(5V)} + 0.5$ V
Output voltage range at any output (V_O)	-0.5 V to $V_{DD} + 0.5$ V
Continuous total power dissipation: <u>3/</u>	
$T_A \leq +25^\circ\text{C}$	5.05 W
$T_A = +70^\circ\text{C}$	2.69 W
$T_A = +85^\circ\text{C}$	1.90 W
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +85°C
Device type 02	-55°C to +125°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential I/O bus voltages, are with respect to network ground.

3/ Dissipation values are with a 2 oz. trace and copper pad with solder.

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1.4 Recommended operating conditions. 1/

Supply voltage range (V_{DD})	
Source power node	+3.0 V to +3.6 V
Non-source power node	+3.0 V to +3.6 V 2/
Minimum high level input voltage (V_{IH}):	
Case 1 (bus holder): $\overline{ISO} = V_{DD}$, $V_{DD(5V)} = V_{DD}$	
Case 2 (5 V Tolerant): $\overline{ISO} = V_{DD}$, $V_{DD(5V)} = 5\text{ V}$	
LREQ, CTL0, CTL1, D0-D7	+2.6 V
C/LKON, PC0, PC1, PC2, $\overline{ISO}$, PD	$0.7 \times V_{DD}$
RESET	$0.6 \times V_{DD}$
Maximum low level input voltage (V_{IL}):	
Case 1 (bus holder): $\overline{ISO} = V_{DD}$, $V_{DD(5V)} = V_{DD}$	
Case 2 (5 V Tolerant): $\overline{ISO} = V_{DD}$, $V_{DD(5V)} = 5\text{ V}$	
LREQ, CTL0, CTL1, D0-D7	+1.2 V
C/LKON, PC0, PC1, PC2, $\overline{ISO}$, PD	$0.2 \times V_{DD}$
RESET	$0.3 \times V_{DD}$
Output current (I_O) (TPBIAS outputs)	-5.6 mA to +1.3 mA
Operating free-air temperature range (T_A):	
Device type 01	-40°C to +85°C
Device type 02	-55°C to +125°C
Differential input voltage range (V_{ID}):	
Cable inputs, during data reception	118 mV to 260 mV
Cable inputs, during arbitration	168 mV to 265 mV
Common-mode input voltage (V_{IC}):	
TPB cable inputs, source power node	0.4706 V to 2.515 V
TPB cable inputs, non-source power node	0.4706 V to 2.015 V 2/
Minimum power-up reset time ($t_{(pu)}$) (RESET input)	2 ms
Maximum receive input jitter:	
TPA, TPB cable inputs, S100 operation	$\pm 1.08\text{ ns}$
TPA, TPB cable inputs, S200 operation	$\pm 0.5\text{ ns}$
TPA, TPB cable inputs, S400 operation	$\pm 0.315\text{ ns}$
Maximum receive input skew:	
Between TPA and TPB cable inputs, S100 operation	$\pm 0.8\text{ ns}$
Between TPA and TPB cable inputs, S200 operation	$\pm 0.55\text{ ns}$
Between TPA and TPB cable inputs, S400 operation	$\pm 0.5\text{ ns}$

1/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2/ For a node that does not source power; see Section 4.2.2.2 in IEEE 1394a-2000.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1394-1995 - (1394) Standard for High-Performance Serial Bus

IEEE 1394a-2000 - (1394) Standard for High-Performance Serial Bus Supplement

(Copies of these documents are available online at <https://www.ieee.org> .

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Limits		Unit
						Min	Max	
Supply current	I _{DD}	<u>2</u> /	3.3 V	25°C	All	115	TYP	mA
		<u>3</u> /				97	TYP	
		<u>4</u> /				75	TYP	
Supply current – ultralow power mode	I _{DD(ULP)}	Ports disabled, PD = 0 V, LPS = 0 V	3.3 V	25°C		150	TYP	µA
Power status threshold, CPS input	V _(TH) <u>5</u> /	400 k□resistor	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C		4.7	7.5	V
High level output voltage	V _{OH}	I _{OH} = -4 mA For CTL0, CTL1, D0-D7, CNA, C/LKON, SYSCLK outputs.	2.7 V			2.2		V
			3.0 V and 3.6 V			2.8		
Low level output voltage	V _{OL}	I _{OL} = 4 mA For CTL0, CTL1, D0-D7, CNA, C/LKON, SYSCLK outputs.	3.0 V and 3.6 V				0.4	V
High level Annex J output voltage	V _{OH(AJ)}	Annex J: I _{OH} = -9 mA ISO = 0 V, V _{DD(5V)} = V _{DD} For CTL0, CTL1, D0-D7, C/LKON, SYSCLK outputs.	3.0 V and 3.6 V			V _{DD} – 0.4		V
Low level Annex J output voltage	V _{OL(AJ)}	Annex J: I _{OL} = 9 mA ISO = 0 V, V _{DD(5V)} = V _{DD} For CTL0, CTL1, D0-D7, C/LKON, SYSCLK outputs.	3.0 V and 3.6 V				0.4	V
Positive peak bus holder current	I _(BH+)	ISO = 3.6 V V _I = 0 V to V _{DD} , V _{DD(5V)} = V _{DD} For CTL0, CTL1, D0-D7, LREQ.	3.6 V		0.05	1	mA	
Negative peak bus holder current	I _(BH-)	ISO = 3.6 V V _I = 0 V to V _{DD} , V _{DD(5V)} = V _{DD} For CTL0, CTL1, D0-D7, LREQ.	3.6 V		-1	-0.05	mA	
Input current	I _I	ISO = 0 V For LREQ, LPS, PD, TESTM, SM, SE, PCO-PC2 inputs.	3.6 V			1	µA	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Lim its		Unit
						Min	Max	
Off-state output current	I _{OZ}	V _O = V _{DD} or 0 V For CTL0, CTL1, D0-D7, C/LKON I/O's.	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All		±5	μA
Pullup current, RESET input	I _(RST)	V _I = 1.5 V or 0 V			01	-90	±20	μA
					02	-110	-20	
Positive input threshold voltage	V _{IT+}	ISO = 0 V, V _{DD(5V)} = V _{DD} For LREQ, CTL0, CTL1, D0-D7 inputs. 6/			All	V _{DD} /2 + 0.3	V _{DD} /2 + 0.9	V
		ISO = 0 V, V _{DD(5V)} = V _{DD} V _{ref} = V _{DD} x 0.4 For LPS inputs.					V _{ref} + 1	
Negative input threshold voltage	V _{IT-}	ISO = 0 V, V _{DD(5V)} = V _{DD} For LREQ, CTL0, CTL1, D0-D7 inputs. 6/				V _{DD} /2 - 0.9	V _{DD} /2 - 0.3	V
		ISO = 0 V, V _{DD(5V)} = V _{DD} V _{ref} = V _{DD} x 0.4 For LPS inputs.				V _{ref} + 0.2		
Output voltage, TPBIAS	V _O	At rated I _O current.				1.665	2.015	V

Driver

Differential output voltage	V _{OD}	R _L = 56Ω See figure 4.	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All	172	265	mV
Driver difference current	I _(DIFF)	Drivers enabled, speed signaling off For TPA+, TPA-, TPB+, TPB-.				-1.05	1.05	mA
Common-mode speed signaling current	I _(SP200)	S200 speed signaling enabled For TPB+, TPB-.				<u>7/</u>	<u>7/</u>	
	I _(SP400)	S400 speed signaling enabled For TPB+, TPB-.				-4.84	-2.53	mA
						<u>8/</u>	<u>8/</u>	
Off state differential voltage	V _{OFF}	Drivers disabled. See figure 4.					20	mV

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Lim its		Unit
						Min	Max	
Receiver								
Differential impedance	Z _{id}	Drivers disabled.	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All	4		kΩ
							4	pF
Common-mode impedance	Z _{ic}	Drivers disabled.				20		kΩ
							24	pF
Receiver input threshold voltage	V _(TH_R)	Drivers disabled.				-30	30	mV
Cable bias detect threshold voltage	V _(TH_CB)	Drivers disabled. For TPB+ and TPB- cable inputs				0.6	1	V
Positive arbitration comparator threshold voltage	V _(TH+)	Drivers disabled.				89	168	mV
Negative arbitration comparator threshold voltage	V _(TH-)	Drivers disabled.				-168	-89	mV
Speed signal threshold	V _(TH_SP200)	TPBIAS-TPA common- mode voltage, drivers disabled.				49	131	mV
	V _(TH_SP400)	TPBIAS-TPA common- mode voltage, drivers disabled.				314	396	mV
Thermal Characteristics								
Junction-to-ambient thermal resistance	R _{□JA}	<u>9/</u>	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All	19.04 TYP	°C/W	
Junction-to-case thermal resistance	R _{□JC}					0.17 TYP	°C/W	
Junction-to-ambient thermal resistance	R _{□JA}	<u>10/</u>				31.52 TYP	°C/W	
Junction-to-case thermal resistance	R _{□JC}					0.17 TYP	°C/W	
Junction-to-ambient thermal resistance	R _{□JA}	<u>11/</u>				49.17 TYP	°C/W	
Junction-to-case thermal resistance	R _{□JC}					3.11 TYP	°C/W	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{DD}	Temperature, T _A	Device type	Lim its		Unit
						Min	Max	
Switching Characteristics								
Jitter, transmit		Between TPA and TPB.	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All		±0.15	ns
Skew, transmit		Between TPA and TPB.					±0.1	ns
TP differential rise time, transmit	t _r	10% to 90% At 1394 connector.				0.5	1.2	ns
TP differential fall time, transmit	t _f	90% to 10% At 1394 connector.				0.5	1.2	ns
Setup time,	t _{su}	50% to 50%, See figure 4. For CTL0, CTL1, D1-D7, LREQ to SYSCLK.				5		ns
Hold time	t _h	50% to 50%, See figure 4. For CTL0, CTL1, D1-D7, LREQ after SYSCLK.		2		ns		
Delay time	t _d	50% to 50%, See figure 4. For SYSCLK to CTL0, CTL1, D1-D7.	3.3 V	+25°C		2		ns
LPS Timing Parameters								
LPS low time	T _{LPSL}	When pulsed. <u>12/</u>	3.0 V and 3.6 V	Device type 01: -40°C to +85°C, Device type 02: -55°C to +125°C	All	0.09	2.6	μs
LPS high time	T _{LPSH}	When pulsed. <u>12/</u>				0.021	2.6	μs
LPS duty cycle		When pulsed. <u>13/</u>				20%	55%	
LPS reset time	T _{LPS_RESET}	Time for PHY to recognize LPS deasserted and reset the interface.				2.6	2.68	μs
LPS disable time,	T _{LPS_DISABLE}	Time for PHY to recognize LPS deasserted and disable the interface.				26.03	26.11	μs
Restore time	T _{RESTORE}	Time to permit optional isolation circuits to restore during an interface reset.				15	23 <u>14/</u>	μs
SYSCLK activation time	T _{CLK_ACTIVATE}	Time for SYSCLK to be activated from reassertion of LPS. PHY not in low-power state.					60	ns
		Time for SYSCLK to be activated from reassertion of LPS. PHY in low-power state.	5.3	7.3	ms			

See footnotes on next sheet.

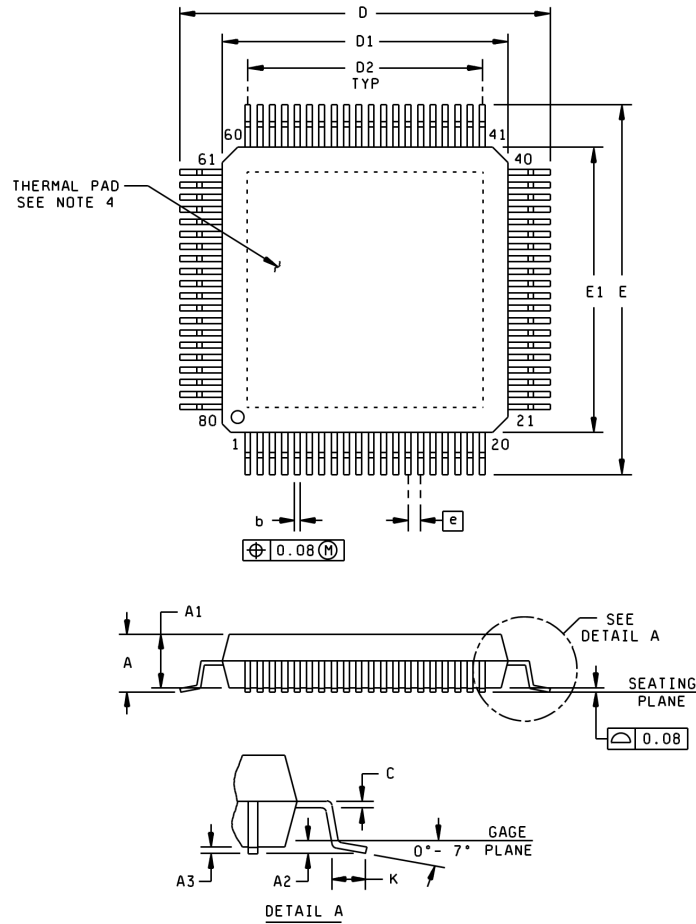
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TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Transmit max packet (three ports transmitting max size isochronous packet – 4096 bytes, sent on every isochronous interval, S400, data value of 0xCCCCCCCCCh).
- 3/ Repeat typical packet (one port receiving DV packets on every isochronous interval, two ports repeating the packet, S100).
- 4/ Idle (three ports transmitting cycle starts).
- 5/ Measured at cable power side of resistor.
- 6/ This parameter applicable only when $\overline{\text{ISO}}$ is low.
- 7/ Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.
- 8/ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.
- 9/ Board mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land with 2 oz. copper.
- 10/ Board mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land with 2 oz. copper.
- 11/ Board mounted, no air flow, high conductivity JEDEC test board with 1 oz. copper.
- 12/ The specified T_{LPSL} and T_{LPSH} times are worst-case values appropriate for operation with the TSB41AB3. These values are broader than those specified for the same parameters in the 1394a-2000 Supplement (i.e., an implementation of LPS that meets the requirements of 1394a-2000 operates correctly with the TSB41AB3).
- 13/ A pulsed LPS signal must have a duty cycle (ratio of T_{LPSH} to cycle period) in the specified range to ensure proper operation when using an isolation barrier on the LPS signal.
- 14/ The maximum value for T_{RESTORE} does not apply when the PHY-LLC interface is disabled, in which case an indefinite time may elapse before LPS is reasserted. Otherwise, in order to reset but not disable the interface it is necessary that the LLC ensure that LPS is deasserted for less than $T_{\text{PLS\_DISABLE}}$.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.047		1.20	D1	0.465	0.480	11.80	12.20
A1	0.037	0.41	0.95	1.05	D2	0.374	TYP	9.50	TYP
A2	0.010	TYP	0.25	TYP	E	0.543	0.559	13.80	14.20
A3	0.002	0.006	0.05	0.15	E1	0.465	0.480	11.80	12.20
b	0.007	0.011	0.17	0.27	e	0.020	TYP	0.50	TYP
C	0.005	NOM	0.13	NOM	K	0.018	0.030	0.45	0.75
D	0.543	0.559	13.80	14.20					

NOTES:

1. This drawing is subject to change without notice.
2. Falls within JEDEC MS-026.
3. All linear dimensions are shown in millimeters.
4. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
5. Body dimensions include mold flash or protrusions.

FIGURE 1. Case outline.

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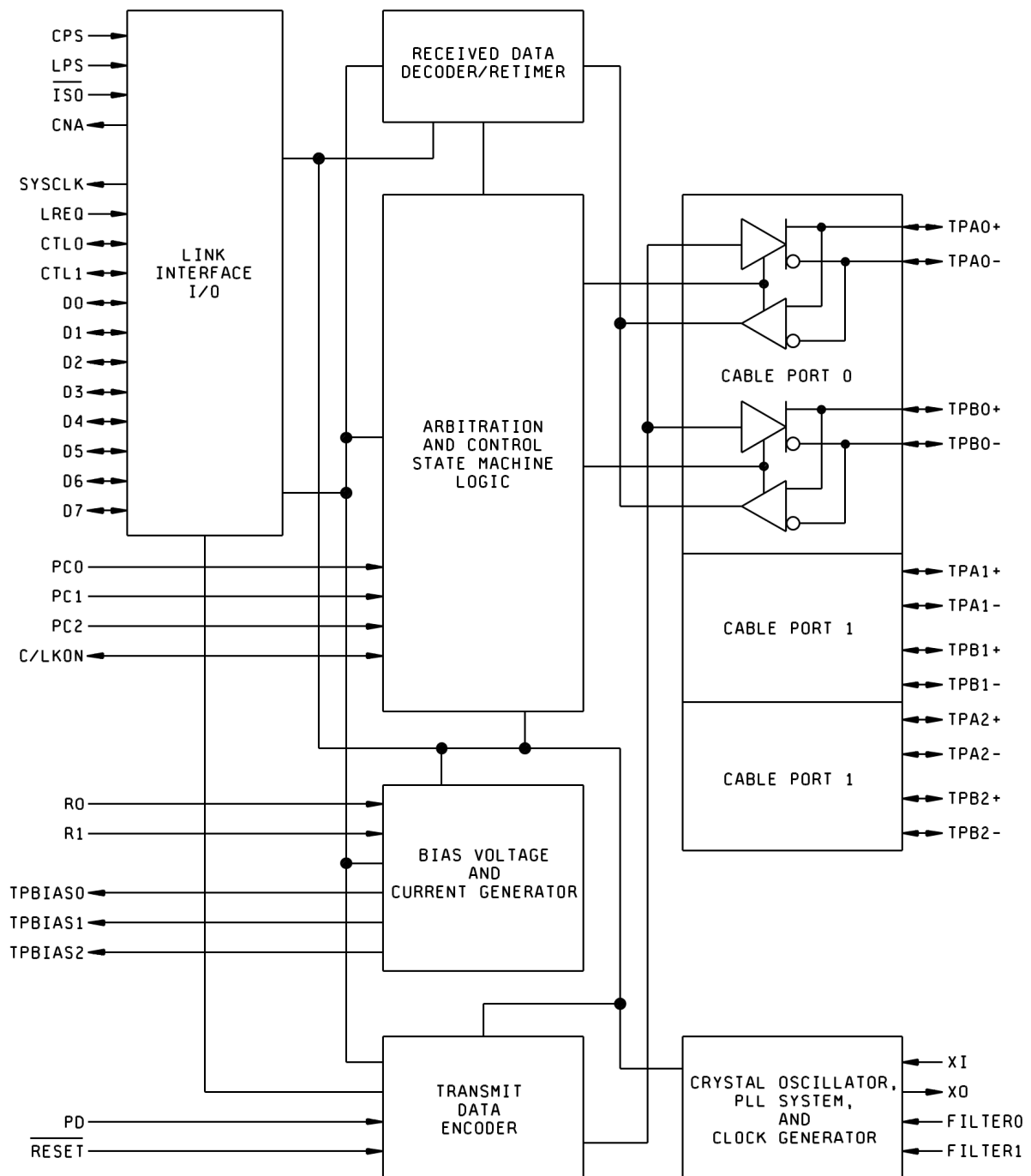


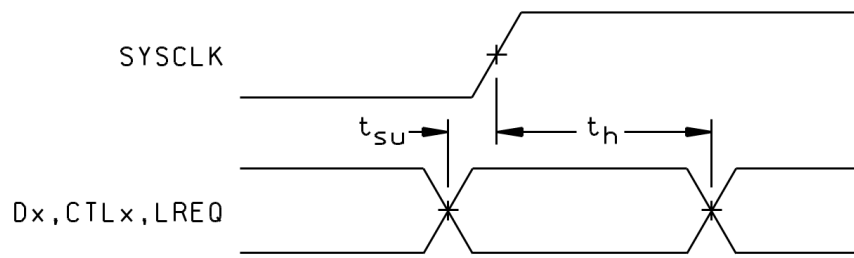
FIGURE 2. Block diagram.

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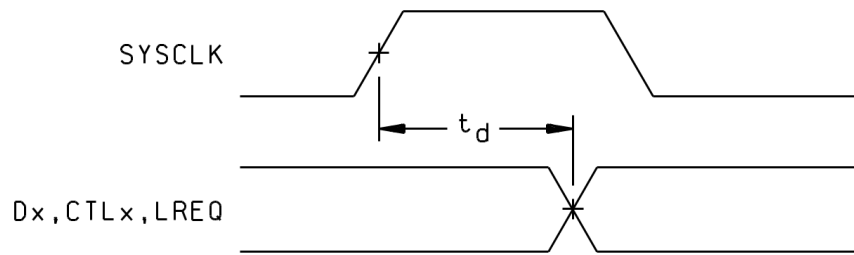
Device types	All						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	LREQ	21	DGND	41	AGND	61	AGND
2	SYSCLK	22	C/LKON	42	TPB0-	62	AV _{DD}
3	DGND	23	PC0	43	TPB0+	63	AV _{DD}
4	CTL0	24	PC1	44	TPA0-	64	AGND
5	CTL1	25	PC2	45	TPA0+	65	AGND
6	DV _{DD}	26	ISO	46	TPBIAS0	66	R0
7	D0	27	CPS	47	AV _{DD}	67	R1
8	D1	28	DGND	48	AV _{DD}	68	DV _{DD}
9	V _{DD-5V}	29	DV _{DD}	49	TPB1-	69	DV _{DD}
10	D2	30	DV _{DD}	50	TPB1+	70	DGND
11	D3	31	TESTM	51	TPA1-	71	FILTER0
12	D4	32	SE	52	TPA1+	72	FILTER1
13	D5	33	SM	53	TPBIAS1	73	PLL _{VDD}
14	D6	34	AV _{DD}	54	AV _{DD}	74	PLL _{GND}
15	D7	35	AV _{DD}	55	TPB2-	75	PLL _{GND}
16	DGND	36	AGND	56	TPB2+	76	XI
17	CNA	37	AGND	57	TPA2-	77	XO
18	PD	38	AGND	58	TPA2+	78	RESET
19	LPS	39	AGND	59	TPBIAS2	79	DV _{DD}
20	DGND	40	AGND	60	AGND	80	DGND

FIGURE 3. Terminal connections.

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Dx,CTLx,LREQ INPUT SETUP AND HOLD TIME WAVEFORMS



Dx AND CTLx OUTPUT DELAY RELATIVE TO SYSCLK WAVEFORMS

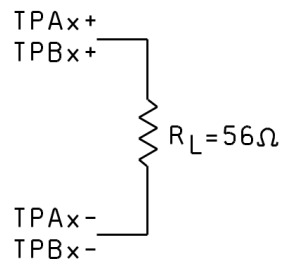


FIGURE 4. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03612-01XE	01295	TSB41AB3IPFPEP	TSB41AB3IEP
V62/03612-02XE	01295	TSB41AB3MPFPEP	TSB41AB3MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/03612
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