

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current revision. - CFS	07-09-12	Thomas M. Hess
B	Update boilerplate paragraphs to current requirements. - PHN	12-04-10	Thomas M. Hess
C	Update boilerplate paragraphs to current requirements. - PHN	18-01-16	Thomas M. Hess
D	Update boilerplate paragraphs to current VID description requirements. - PHN	23-08-24	Muhammad A. Akbar



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
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REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17					

PMIC N/A	PREPARED BY Charles F. Saffle		DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY Thomas M. Hess		TITLE MICROCIRCUIT, DIGITAL, CMOS, HIGH-SPEED SERIAL-BUS LINK-LAYER CONTROLLER, MONOLITHIC SILICON		
	APPROVED BY Thomas M. Hess				
	Original date of drawing YY MM DD 02-12-12	SIZE A	CAGE CODE 16236	DWG NO. V62/03611	
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AMSC N/A

5962-V139-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high-speed serial-bus link-layer controller microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03611	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TSB12LV01B-EP	High-Speed Serial-Bus Link-Layer Controller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	100	JEDEC MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}).....	-0.5 V to +3.6 V
Supply voltage range (V_{CC5V}).....	-0.5 V to +5.5 V
Input voltage range (V_I).....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range (V_O).....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current (I_{IK}) ($V_I < 0$ or $V_I > V_{CC}$).....	±20 mA 2/
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$).....	±20 mA 3/
Maximum power dissipation:	
T_A □ +25□C.....	1500 mW
T_A □ +70□C.....	739.5 mW
T_A □ +85□C.....	486 mW
Operating free-air temperature range (T_A).....	-40°C to +85°C
Storage temperature range (T_{STG}).....	-65°C to +150°C

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC}).....	+3.0 V to +3.6 V
Supply voltage range (V_{CC5V}):	
(5 V tolerant).....	+3.0 V to +5.5 V
(Non 5 V tolerant).....	+3.0 V to +3.6 V
Minimum high level input voltage (V_{IH}).....	+2.0 V
Maximum low level input voltage (V_{IL}).....	+0.8 V
Transition time (t_i) (10% to 90%).....	0 to 6 ns
Operating free-air temperature range (T_A).....	-40°C to +85°C
Junction temperature range (T_J).....	0°C to +115°C 5/

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ This applies to external input and bidirectional buffers. For 5 V tolerant terminals, use $V_I > V_{CC5V}$.
- 3/ This applies to external output and bidirectional buffers. For 5 V tolerant terminals, use $V_O > V_{CC5V}$.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 5/ The junction temperatures listed reflect simulation conditions. The absolute maximum junction temperature is 150°C. The customer is responsible for verifying the junction temperature.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1394-1995 - (1394) Standard for High-Performance Serial Bus

(Copies of these documents are available online at <https://www.ieee.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Block diagram. The block diagram shall be as shown in figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions unless otherwise specified		V _{CC}	Temperature T _A	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	I _{OH} = -8 mA <u>2</u> /		3.0 V and 3.6 V	-40°C to +85°C	V _{CC} – 0.6		V
		I _{OH} = -4 mA <u>3</u> /				V _{CC} – 0.6		V
Low level output voltage	V _{OL}	I _{OL} = 8 mA <u>2</u> /		3.0 V and 3.6 V			0.5	V
		I _{OL} = 4 mA <u>3</u> /					0.5	V
Low level input current	I _{IL} <u>4</u> /	V _I = GND	TTL/LVCMOS	3.0 V and 3.6 V			-1	μA
			5-V tolerant	3.0 V and 3.6 V			-20	μA
			D0-D7, CTL0, CTL1	3.0 V and 3.6 V			-20	μA
High level input current	I _{IH}	V _I = V _{CC} V _I = V _{CC} , 5V	TTL/LVCMOS	3.0 V and 3.6 V			1	μA
			5-V tolerant	3.0 V and 3.6 V			20	μA
			D0-D7, CTL0, CTL1	3.0 V and 3.6 V			20	μA
High-impedance state output current	I _{oz} <u>5</u> /	V _O = V _{CC} or GND		3.0 V and 3.6 V		±20	μA	
Static supply current	I _{CC(Q)}	I _O = 0		3.0 V and 3.6 V	88	TYP	μA	
Dynamic supply current	I _{CC(Dynamic)}			3.0 V and 3.6 V	120	TYP	mA	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{CC}	Temperature T _A	Limits		Unit
					Min	Max	
Host-Interface Timing Requirements 6/							
Cycle time, BCLK	t _{c1}	See figure 4.	3.0 V and 3.6 V	+25°C	20	111	ns
Pulse duration, BCLK high	t _{w1(H)}				8.6		ns
Pulse duration, BCLK low	t _{w1(L)}				8.6		ns
Setup time, DATA0-DATA31 valid before BCLK↑	t _{su1}				4		ns
Hold time, DATA0-DATA31 valid after BCLK↑	t _{h1}				2		ns
Setup time, ADDR0-ADDR7 valid before BCLK↑	t _{su2}				8		ns
Hold time, ADDR0-ADDR7 valid after BCLK↑	t _{h2}				2		ns
Setup time, $\overline{\text{CS}}$ low before BCLK↑	t _{su3}				8		ns
Hold time, $\overline{\text{CS}}$ low after BCLK↑	t _{h3}				2		ns
Setup time, $\overline{\text{WR}}$ valid before BCLK↑	t _{su4}				8		ns
Hold time, $\overline{\text{WR}}$ valid after BCLK↑	t _{h4}				2		ns
Host-Interface Switching Characteristics							
Delay time, BCLK↑ to $\overline{\text{CA}}\downarrow$	t _{d1}	See figure 4 C _L = 45 pF	3.0 V and 3.6 V	-40°C to +85°C	2.5	8	ns
Delay time, BCLK↑ to CA↑	t _{d2}				2.5	8	ns
Delay time, BCLK↑ to DATA0-DATA31 valid	t _{d3} 6/				2.5	10	ns
Delay time, BCLK↑ to DATA0-DATA31 invalid	t _{d4} 6/				2.5	10	ns
Cable PHY-Layer-Interface Timing Requirements 6/							
Cycle time, SCLK	t _{c2}	See figure 4.	3.0 V and 3.6 V	-40°C to +85°C	20.347	20.343	ns
Pulse duration, SCLK high	t _{w2(H)}				9		ns
Pulse duration, SCLK low	t _{w2(L)}				9		ns
Setup time, D0-D7 valid before SCLK↑	t _{su5}				4		ns
Hold time, D0-D7 valid after SCLK↑	t _{h5}				0		ns
Setup time, CTL0-CTL1 valid before SCLK↑	t _{su6}				4		ns
Hold time, CTL0-CTL1 valid after SCLK↑	t _{h6}				0		ns

See footnotes at end of table

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions unless otherwise specified	V _{CC}	Temperature T _A	Limits		Unit
					Min	Max	
Cable PHY-Layer-Interface Switching Characteristics 6/							
Delay time, SCLK↑ to D0-D7 valid	t _{d5}	See figure 4 C _L = 45 pF	3.0 V and 3.6 V	-40°C to +85°C	1	11	ns
Delay time, SCLK↑ to D0-D7 invalid	t _{d6}				1	11	ns
Delay time, SCLK↑ to D0-D7 invalid	t _{d7}				1	11	ns
Delay time, SCLK↑ to CTL0-CTL1 valid	t _{d8}				1	11	ns
Delay time, SCLK↑ to CTL0-CTL1 invalid	t _{d9}				1	11	ns
Delay time, SCLK↑ to CTL0-CTL1 invalid	t _{d10}				1	11	ns
Delay time, SCLK↑ to LREQ↓	t _{d11}				1	11	ns
Miscellaneous Timing Requirements 6/							
Cycle time, CYCLEIN	t _{c3}	See figure 4.	3.0 V and 3.6 V	-40°C to +85°C	124.99	125.01	□§
Pulse duration, CYCLEIN high	t _{w3(H)}				0.08	120	□§
Pulse duration, CYCLEIN low	t _{w3(L)}				4		□§
Miscellaneous Signal Switching Characteristics 6/							
Delay time, SCLK↑ to INT↓	t _{d12}	See figure 4.	3.0 V and 3.6 V	-40°C to +85°C	4	18	ns
Delay time, SCLK↑ to INT↑	t _{d13}				4	18	ns
Delay time, SCLK↑ to CYCLEOUT↑	t _{d14}				4	16	ns
Delay time, SCLK↑ to CYCLEOUT↓	t _{d15}				4	16	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This test condition is for terminals D0-D7, CTL0, CTL1, and POWERON.

3/ This test condition is for terminals DATA0-DATA31, $\overline{CA}$, $\overline{INT}$, CYCLEOUT, GRFEMP, CYDNE, and CYST.

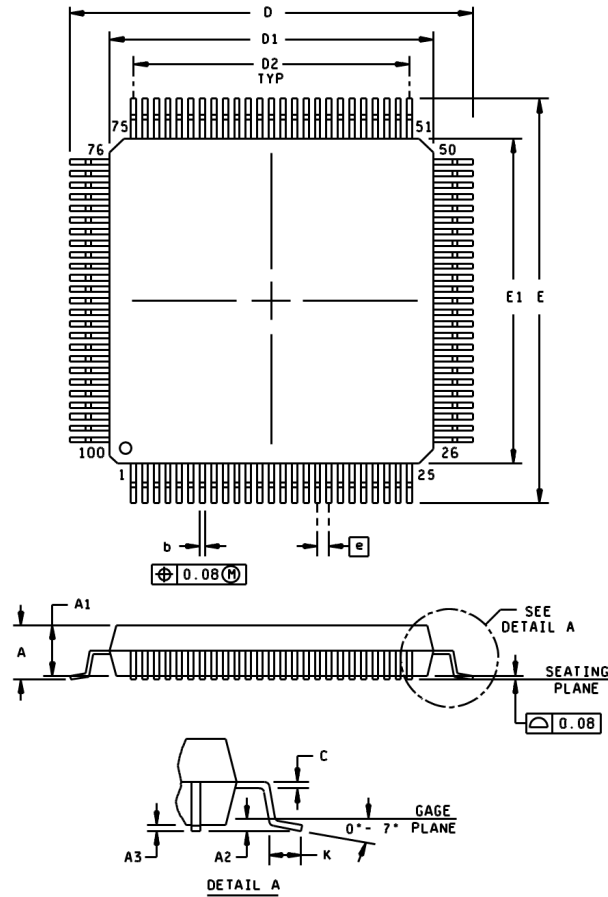
4/ This specification only applies when pull-up and pull-down terminator is turned off.

5/ Three-state output must be in high-impedance mode.

6/ These parameters are not production tested.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		0.047		1.20	D1	0.543	0.559	13.80	14.20
A1	0.053	0.057	1.35	1.45	D2	0.472	TYP	12.00	TYP
A2	0.010	TYP	0.25	TYP	E	0.622	0.638	15.80	16.20
A3	0.002		0.05		E1	0.543	0.559	13.80	14.20
b	0.007	0.011	0.17	0.27	e	0.020	TYP	0.50	TYP
c	0.005	NOM	0.13	NOM	K	0.018	0.030	0.45	0.75
D	0.622	0.638	15.80	16.20					

NOTES:

1. This drawing is subject to change without notice.
1. Falls within JEDEC MS-026.
2. All linear dimensions are shown in millimeters.

FIGURE 1. Case outline.

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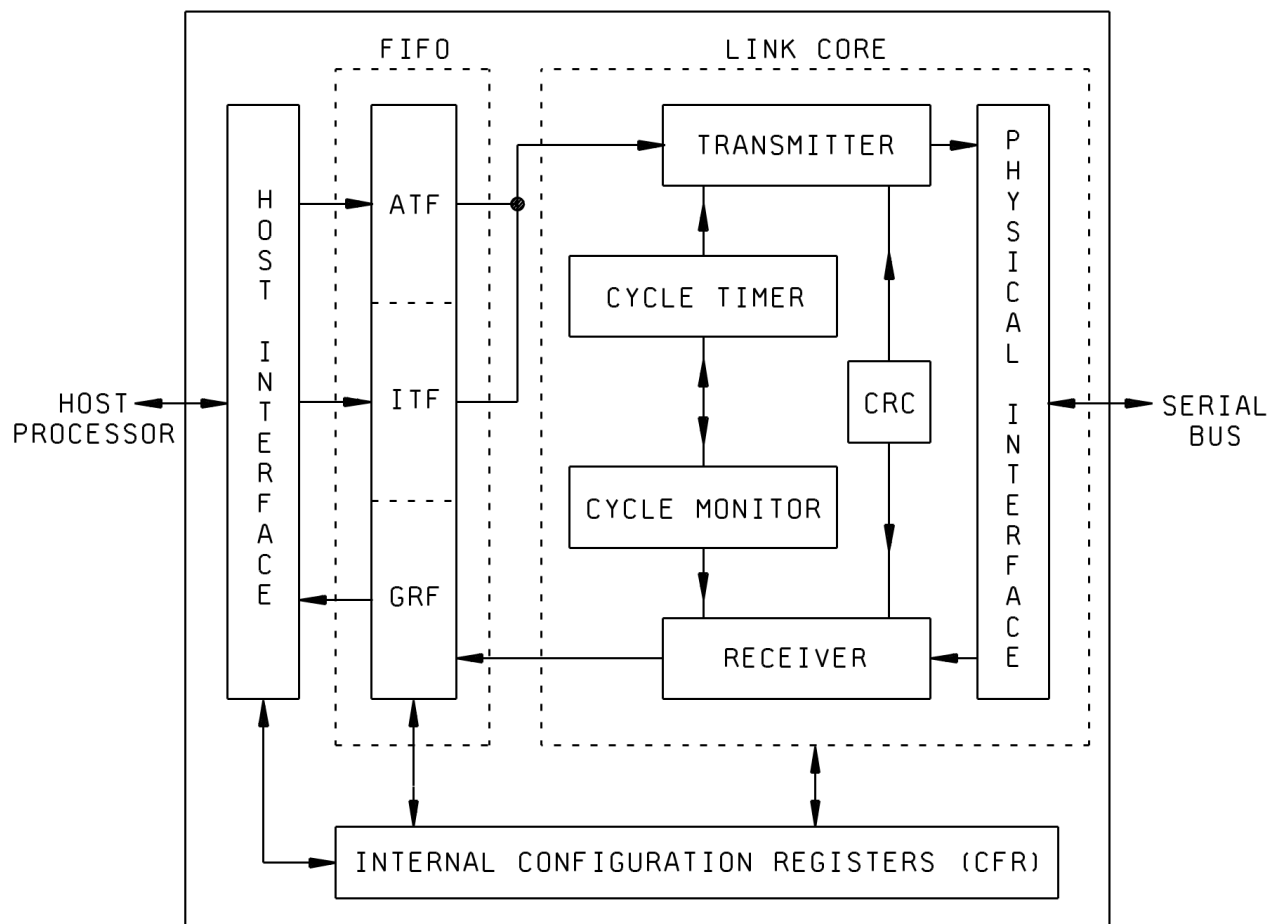


FIGURE 2. Block diagram.

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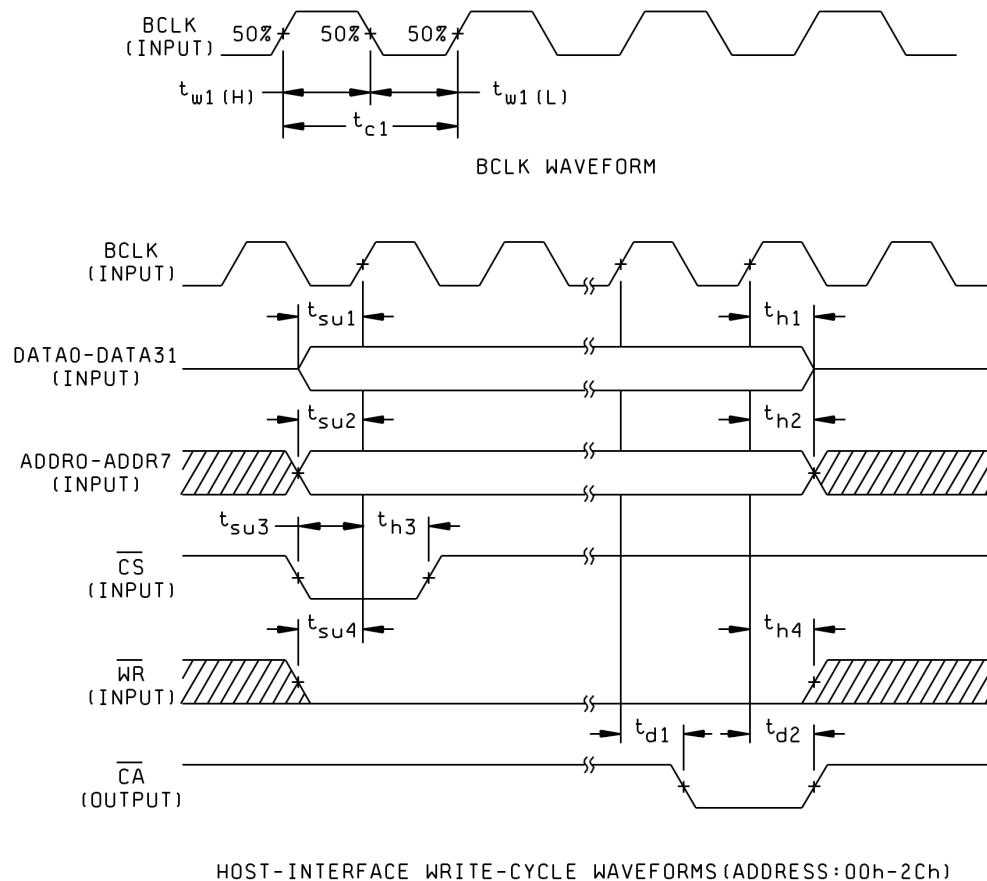
Device Type 01

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	26	V _{CC}	51	GND	76	POWERON
2	DATA16	27	ADDR4	52	D7	77	MTEST3
3	DATA17	28	ADDR5	53	D6	78	GND
4	DATA18	29	ADDR6	54	D5	79	GND
5	DATA19	30	ADDR7	55	D4	80	GND
6	V _{CC}	31	GND	56	V _{CC}	81	GND
7	DATA20	32	BCLK	57	D3	82	DATA0
8	DATA21	33	V _{CC} +5	58	D2	83	DATA1
9	DATA22	34	$\overline{\text{CS}}$	59	D1	84	DATA2
10	DATA23	35	$\overline{\text{CA}}$	60	D0	85	DATA3
11	GND	36	$\overline{\text{WR}}$	61	GND	86	V _{CC} +5
12	DATA24	37	$\overline{\text{INT}}$	62	CTL1	87	DATA4
13	DATA25	38	GND	63	CTL0	88	DATA5
14	DATA26	39	RESET	64	V _{CC} +5	89	DATA6
15	DATA27	40	GND	65	SCLK	90	DATA7
16	V _{CC} +5V	41	GND	66	GND	91	GND
17	DATA28	42	CYCLEIN	67	LREQ	92	DATA8
18	DATA29	43	V _{CC}	68	GND	93	DATA9
19	DATA30	44	CYCLEOUT	69	V _{CC}	94	DATA10
20	DATA31	45	GND	70	GND	95	DATA11
21	GND	46	GND	71	MTEST0	96	V _{CC}
22	ADDR0	47	GND	72	MTEST1	97	DATA12
23	ADDR1	48	GRFEMP/ GPO0	73	MTEST2	98	DATA13
24	ADDR2	49	CYDNE/ GPO1	74	V _{CC}	99	DATA14
25	ADDR3	50	CYST/GPO 2	75	Reserved	100	DATA15

FIGURE 3. Terminal connections.

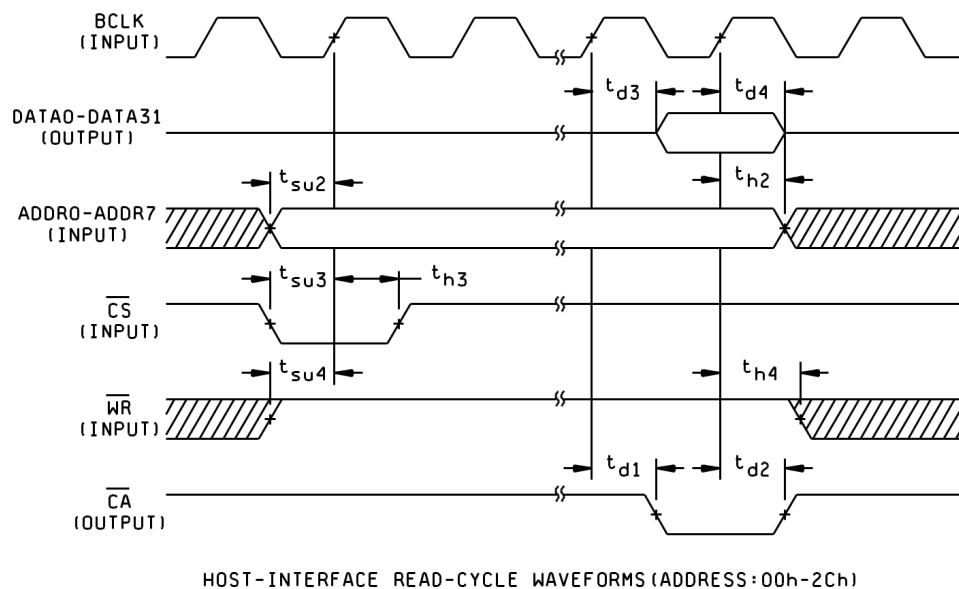
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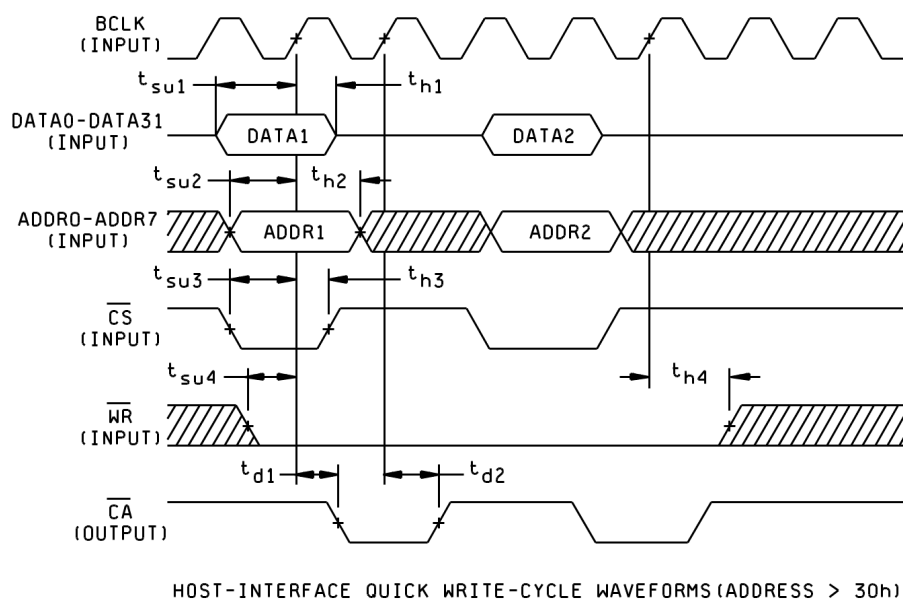
NOTE: Following a $\overline{\text{CS}}$ assertion, there may be a maximum of 9 rising edges of BCLK before a $\overline{\text{CA}}$ is returned. $\overline{\text{CA}}$ must be returned before another CS may be asserted.

FIGURE 4. Timing waveforms.

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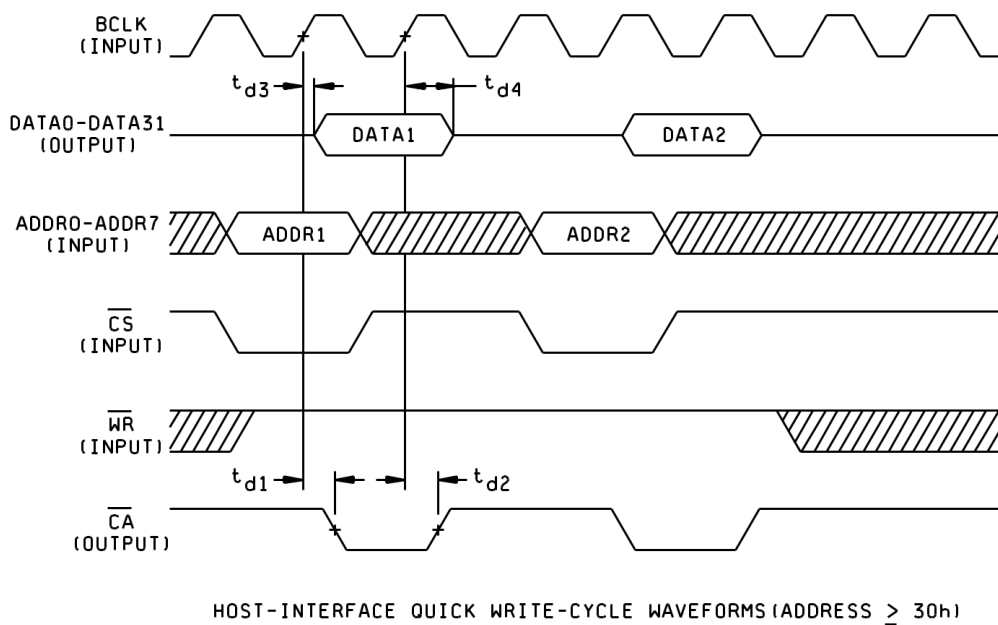
NOTE: Following a $\overline{\text{CS}}$ assertion, there may be a maximum of 9 rising edges of BCLK before a $\overline{\text{CA}}$ is returned. $\overline{\text{CA}}$ must be returned before another CS may be asserted.



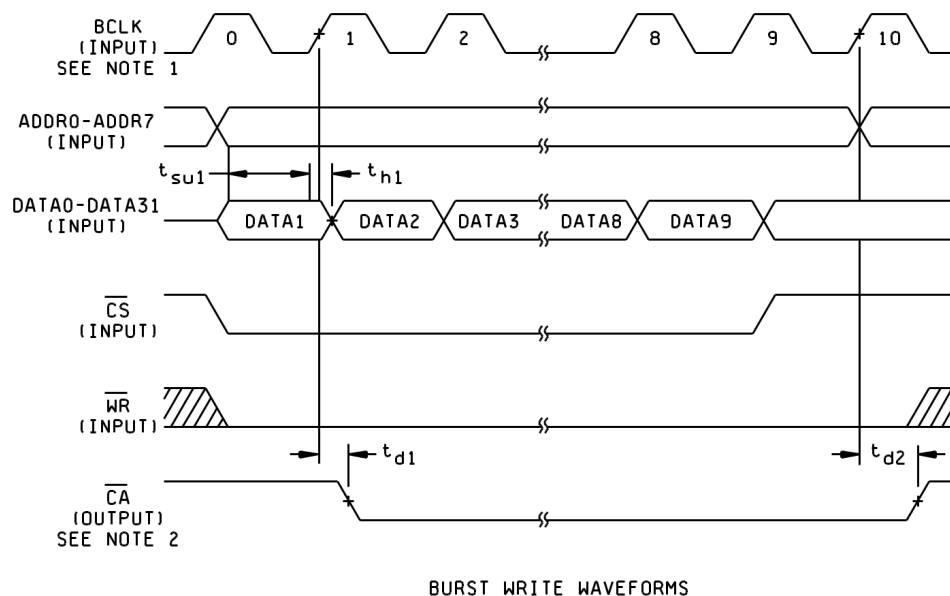
NOTE: There must be a minimum of 3 rising edges of BCLK between assertions of $\overline{\text{CS}}$.

FIGURE 4. Timing waveforms - Continued.

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NOTE: There must be a minimum of 3 rising edges of BCLK between assertions of $\overline{CS}$.

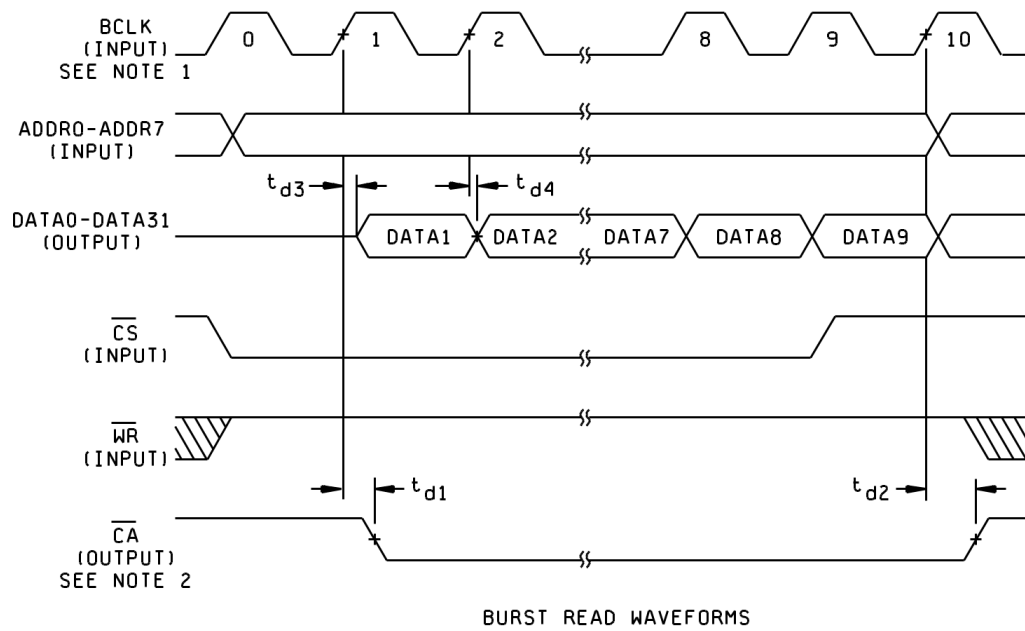


NOTES:

1. At the nth BCLK rising edge, DATA_n is written into the FIFO.
2. CA is one cycle delay from respective $\overline{CS}$.

FIGURE 4. Timing waveforms - Continued.

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- NOTES:
1. At the (nth+1) BCLK rising edge, host bus should latch DATA_n.
 2. CA is one cycle delay from respective CS.
 3. These waveforms only apply to address C0h.

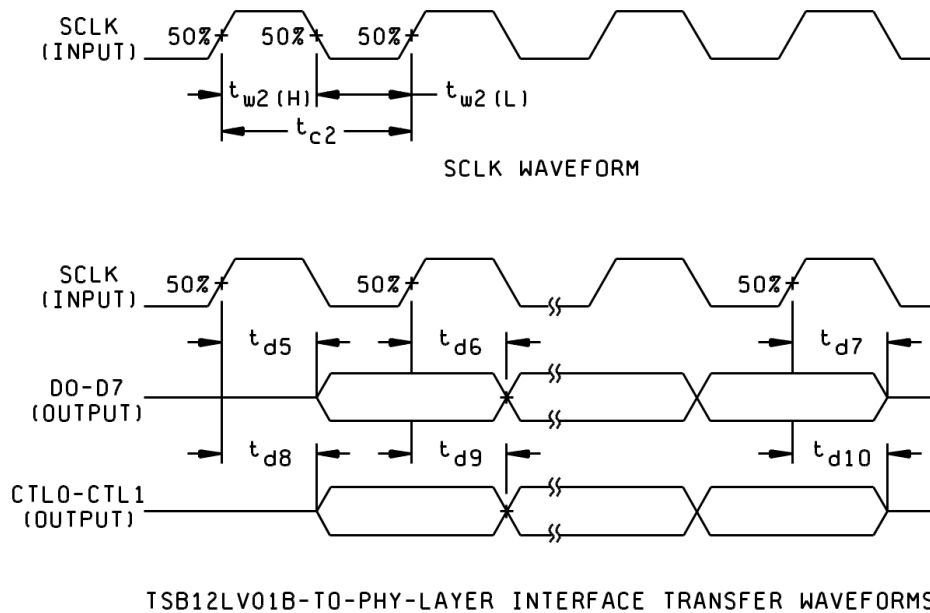
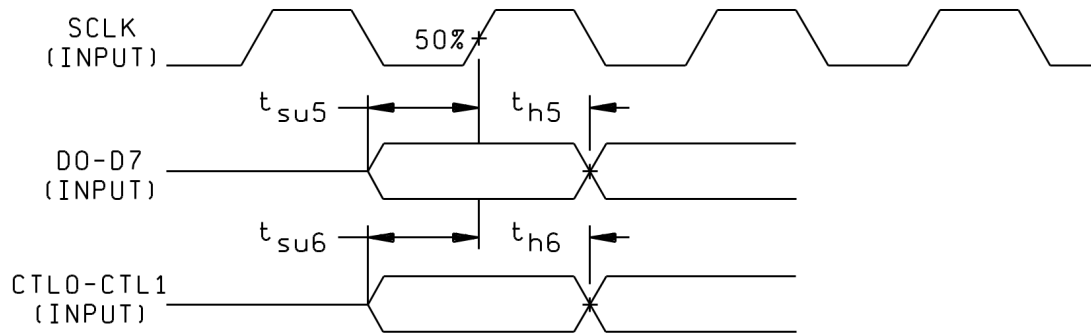
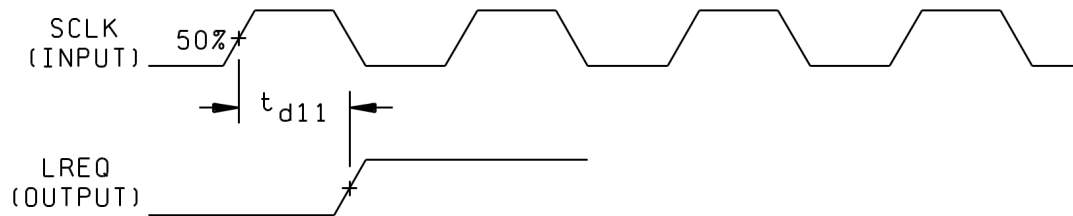


FIGURE 4. Timing waveforms - Continued.

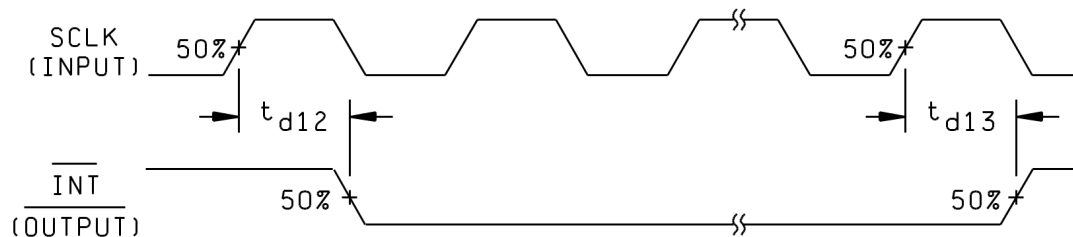
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PHY LAYER INTERFACE-TO-TSB12LV01B TRANSFER WAVEFORMS



TSB12LV01B LINK-REQUEST-TO-PHY LAYER INTERFACE WAVEFORMS



INTERRUPT WAVEFORM

FIGURE 4. Timing waveforms - Continued.

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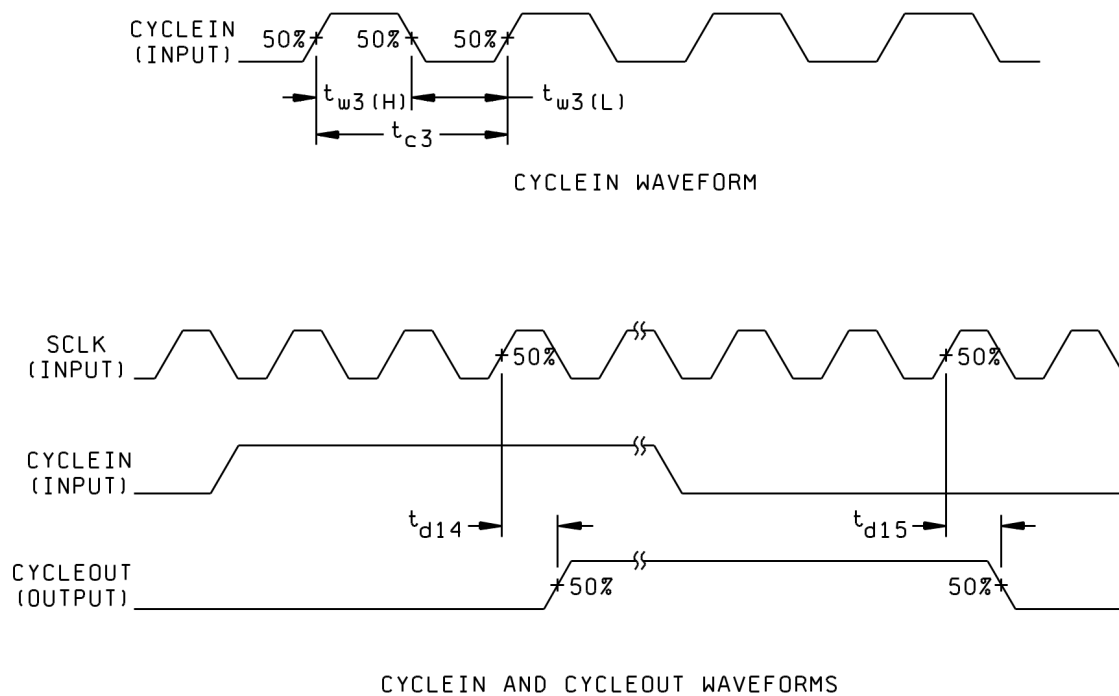


FIGURE 4. Timing waveforms - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03611-01XE	01295	TSB12LV01BIPZTEP	12LV01BIEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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