

	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED
	A	Make correction the title block. Replace footnote 1/ under Table I. Add notes and inch dimensions to figure 1. Drawing updated to reflect current requirements. - ro	08-04-28	R. HEBER
	B	Make changes to TM2-0 test modes 010 and 110 as specified in Table E figure 5. Update document paragraphs to current requirements. - ro	14-09-03	C. SAFFLE
	C	Make correction to the Table A output code table by deleting -ΔREF and replacing with +ΔREF in two places as specified under Figure 5. Update document paragraphs to current requirements. - ro	20-06-11	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
PAGE																				
REV	C	C	C																	
PAGE	18	19	20																	
REV STATUS OF PAGES			REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
			PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	PREPARED BY RICK OFFICER		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	
Original date of drawing YY-MM-DD 02-12-12	CHECKED BY TOM HESS		TITLE MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 14-BIT, 1, 3, 8 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON	
	APPROVED BY RAYMOND MONNIN			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03608	
	REV C		PAGE 1 OF 20	

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance analog-to-digital microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03608</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>	<u>Clock frequency</u>
01	THS1401-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	1 MHz
02	THS1403-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	3 MHz
03	THS1408-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	8 MHz

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	MS-026	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage (AVDD to AGND)	4 V
Supply voltage (DVDD to DGND)	4 V
Reference input voltage range (VBG)	-0.3 V to AVDD +0.3 V
Analog input voltage range	-0.3 V to AVDD +0.3 V
Digital input voltage range	-0.3 V to DVDD +0.3 V
Storage temperature range (TSTG)	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
Thermal resistance, junction-to-case (θ_{JC})	0.79°C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA})	28.8°C/W 2/

1.4 Recommended operating conditions. 3/

Supply voltage range (AVDD, DVDD)	3 V to 3.6 V
High level digital input voltage (V_{IH})	2 V minimum
Low level digital input voltage (V_{IL})	0.8 V maximum
Load capacitance (CL)	15 pF maximum
Clock frequency (fCLK) :	
Device type 01	0.1 to 1 MHz
Device type 02	0.1 to 3 MHz
Device type 03	0.1 to 8 MHz
Clock duty cycle	45% to 55%
Operating free-air temperature range (TA):	
Device types 01 and 02	-40°C to +125°C
Device type 03	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Informational purposes only, not production tested.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4.

3.5.5 Principles of operation. The principles of operation and test circuit shall be as shown in figure 5.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions AVDD = DVDD = 3.3 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Power supply section.							
Analog supply current	IDDA	AVDD = 3.6 V	-40°C ≤ TA ≤ +125°C	01,02		90	mA
			-55°C ≤ TA ≤ +125°C	03		90	
Digital supply current	IDDD	DVDD = 3.6 V	-40°C ≤ TA ≤ +125°C	01,02		10	mA
			-55°C ≤ TA ≤ +125°C	03		10	
Power		AVDD = DVDD = 3.6 V	-40°C ≤ TA ≤ +125°C	01,02		360	mW
			-55°C ≤ TA ≤ +125°C	03		360	
Power down current			-40°C ≤ TA ≤ +125°C	01,02	20 typical		μA
			-55°C ≤ TA ≤ +125°C	03	20 typical		
DC characteristics section.							
Resolution			-40°C ≤ TA ≤ +125°C	01,02	14 typical		Bits
			-55°C ≤ TA ≤ +125°C	03	14 typical		
Differential nonlinearity	DNL		-40°C ≤ TA ≤ +125°C	01,02		±1	LSB
			-55°C ≤ TA ≤ +125°C	03		±1	
Integral nonlinearity	INL	Best fit	-40°C ≤ TA ≤ +125°C	01		±2.5	LSB
				02		±3	
			-55°C ≤ TA ≤ +125°C	03		±7.5	
Offset error	OE	IN+, IN-, PGA = 0 dB	-40°C ≤ TA ≤ +125°C	01,02		0.3	%FSR
			-55°C ≤ TA ≤ +125°C	03		0.3	
Gain error	GE	PGA = 0 dB	-40°C ≤ TA ≤ +125°C	01,02		1.75	%FSR
			-55°C ≤ TA ≤ +125°C	03		1.75	

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions AVDD = DVDD = 3.3 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
AC characteristics section.							
Effective number of bits	ENOB		-40°C ≤ TA ≤ +125°C	01,02	11.2		Bits
			-55°C ≤ TA ≤ +125°C	03	11.2		
Total harmonic distortion	THD	fi = 100 kHz	-40°C ≤ TA ≤ +125°C	01,02	-81 typical		dB
			-55°C ≤ TA ≤ +125°C	03	-81 typical		
		fi = 1 MHz	-40°C ≤ TA ≤ +125°C	02	-78 typical		
			-55°C ≤ TA ≤ +125°C	03	-78 typical		
		fi = 4 MHz	-55°C ≤ TA ≤ +125°C	03	-77 typical		
Signal-to-noise ratio	SNR	fi = 100 kHz	-40°C ≤ TA ≤ +125°C	01,02	72 typical		dB
			-55°C ≤ TA ≤ +125°C	03	72 typical		
		fi = 1 MHz	-40°C ≤ TA ≤ +125°C	02	70		
			-55°C ≤ TA ≤ +125°C	03	70		
		fi = 4 MHz	-55°C ≤ TA ≤ +125°C	03	71 typical		
Signal-to-noise ratio + distortion	SINAD	fi = 100 kHz	-40°C ≤ TA ≤ +125°C	01,02	70 typical		dB
			-55°C ≤ TA ≤ +125°C	03	70 typical		
		fi = 1 MHz	-40°C ≤ TA ≤ +125°C	02	69		
			-55°C ≤ TA ≤ +125°C	03	69		
		fi = 4 MHz	-55°C ≤ TA ≤ +125°C	03	70 typical		
Spurious free dynamic range	SFDR	fi = 100 kHz	-40°C ≤ TA ≤ +125°C	01,02	80 typical		dB
			-55°C ≤ TA ≤ +125°C	03	80 typical		
		fi = 1 MHz	-40°C ≤ TA ≤ +125°C	02	71		
			-55°C ≤ TA ≤ +125°C	03	71		
		fi = 4 MHz	-40°C ≤ TA ≤ +125°C	03	80 typical		

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions AVDD = DVDD = 3.3 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
AC characteristics section – continued.							
Analog input bandwidth			-40°C ≤ TA ≤ +125°C	01,02	140 typical		MHz
			-55°C ≤ TA ≤ +125°C	03	140 typical		
Reference voltage section.							
Bandgap voltage, internal mode	VBG		-40°C ≤ TA ≤ +125°C	01,02	1.425	1.575	V
			-55°C ≤ TA ≤ +125°C	03	1.425	1.575	
Input impedance			-40°C ≤ TA ≤ +125°C	01,02	40 typical		kΩ
			-55°C ≤ TA ≤ +125°C	03	40 typical		
Positive reference voltage	REF+		-40°C ≤ TA ≤ +125°C	01,02	2.5 typical		V
			-55°C ≤ TA ≤ +125°C	03	2.5 typical		
Negative reference voltage	REF-		-40°C ≤ TA ≤ +125°C	01,02	0.5 typical		V
			-55°C ≤ TA ≤ +125°C	03	0.5 typical		
Reference difference, REF+ - REF-	ΔREF		-40°C ≤ TA ≤ +125°C	01,02	2 typical		V
			-55°C ≤ TA ≤ +125°C	03	2 typical		
Accuracy, internal reference			-40°C ≤ TA ≤ +125°C	01,02	5 typical		%
			-55°C ≤ TA ≤ +125°C	03	5 typical		
Temperature coefficient	TC		-40°C ≤ TA ≤ +125°C	01,02	40 typical		ppm/ °C
			-55°C ≤ TA ≤ +125°C	03	40 typical		
Voltage coefficient	VC		-40°C ≤ TA ≤ +125°C	01,02	200 typical		ppm/V
			-55°C ≤ TA ≤ +125°C	03	200 typical		

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions AVDD = DVDD = 3.3 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Analog inputs section.							
Positive analog input	IN+		-40°C ≤ TA ≤ +125°C	01,02	0	AVDD	V
			-55°C ≤ TA ≤ +125°C	03	0	AVDD	
Negative analog input	IN-		-40°C ≤ TA ≤ +125°C	01,02	0	AVDD	V
			-55°C ≤ TA ≤ +125°C	03	0	AVDD	
Analog input voltage difference		ΔAin = IN+ - IN-, Vref = REF+ - REF-	-40°C ≤ TA ≤ +125°C	01,02	-Vref	Vref	V
			-55°C ≤ TA ≤ +125°C	03	-Vref	Vref	
Input impedance			-40°C ≤ TA ≤ +125°C	01,02	25 typical		kΩ
			-55°C ≤ TA ≤ +125°C	03	25 typical		
PGA range			-40°C ≤ TA ≤ +125°C	01,02	0	7	dB
			-55°C ≤ TA ≤ +125°C	03	0	7	
PGA step size			-40°C ≤ TA ≤ +125°C	01,02	1 typical		dB
			-55°C ≤ TA ≤ +125°C	03	1 typical		
PGA gain error			-40°C ≤ TA ≤ +125°C	01,02		±0.25	dB
			-55°C ≤ TA ≤ +125°C	03		±0.25	
Digital inputs section.							
High level digital input	VIH		-40°C ≤ TA ≤ +125°C	01,02	2		V
			-55°C ≤ TA ≤ +125°C	03	2		
Low level digital input	VIL		-40°C ≤ TA ≤ +125°C	01,02		0.8	V
			-55°C ≤ TA ≤ +125°C	03		0.8	
Input capacitance	CIN		-40°C ≤ TA ≤ +125°C	01,02	5 typical		pF
			-55°C ≤ TA ≤ +125°C	03	5 typical		
Input current	IIN		-40°C ≤ TA ≤ +125°C	01,02		±1	μA
			-55°C ≤ TA ≤ +125°C	03		±1	

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 8

TABLE I. Electrical performance characteristics – Continued. 1/

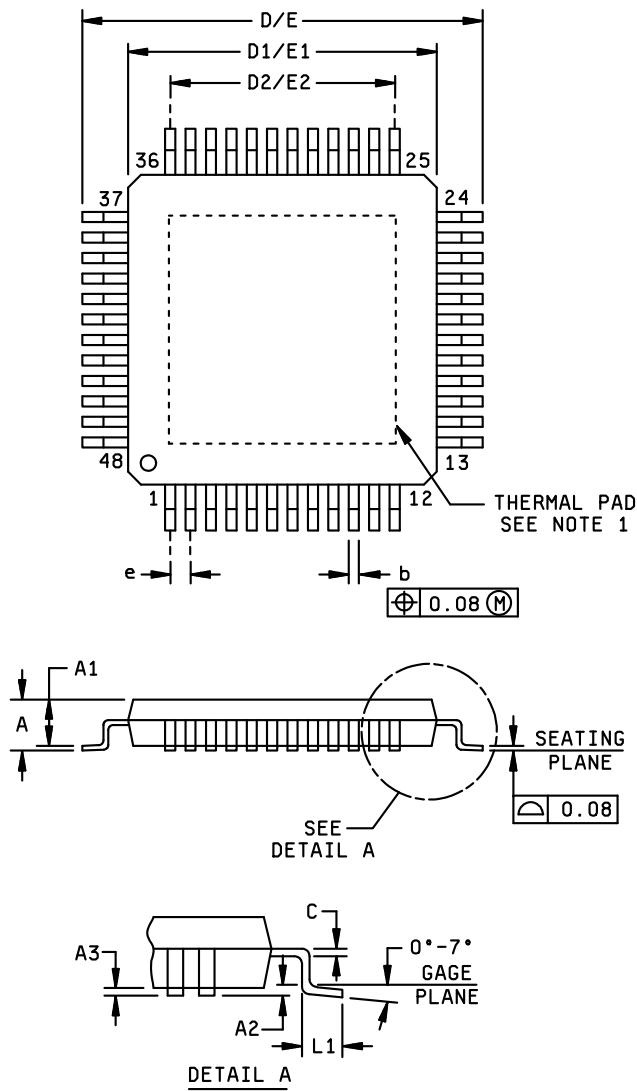
Test	Symbol	Conditions AVDD = DVDD = 3.3 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Digital outputs section.							
High level digital output	VOH	IOH = 50 μA	-40°C ≤ TA ≤ +125°C	01,02	2.6		V
			-55°C ≤ TA ≤ +125°C	03	2.6		
Low level digital output	VOL	IOL = 50 μA	-40°C ≤ TA ≤ +125°C	01,02		0.4	V
			-55°C ≤ TA ≤ +125°C	03		0.4	
Output current, high impedance	IOZ		-40°C ≤ TA ≤ +125°C	01,02		±10	μA
			-55°C ≤ TA ≤ +125°C	03		±10	
Clock timing (CS low) section.							
Clock frequency	fCLK		-40°C ≤ TA ≤ +125°C	01	0.1 <u>2/</u>	1	MHz
				02	0.1 <u>2/</u>	3	
			-55°C ≤ TA ≤ +125°C	03	0.1 <u>2/</u>	8	
Output delay time	td		-40°C ≤ TA ≤ +125°C	01,02		25	ns
			-55°C ≤ TA ≤ +125°C	03		25	
Latency			-40°C ≤ TA ≤ +125°C	01,02	9.5 typical		Cycles
			-55°C ≤ TA ≤ +125°C	03	9.5 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This parameter is not production tested.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 9

Case X

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 10

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.037	.041	0.95	1.05
A2	.009	---	0.25	---
A3	.001	.005	0.05	0.15
b	.006	.010	0.17	0.27
C	.005	---	0.13	---
D	.346	.362	8.80	9.20
D1	.267	.283	6.80	7.20
D2	.216	---	5.50	---
E	.346	.362	8.80	9.20
E1	.267	.283	6.80	7.20
E2	.216	---	5.50	---
e	.019 BSC		0.50 BSC	
L1	.017	.029	0.45	0.75

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. The package thermal performance may be enhanced by bonding the thermal pad to an thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outline – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 11

Device types	All		Device types	All
Case outline	X		Case outline	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	-IN		25	DGND
2	AVDD		26	DVDD
3	VBG		27	D2
4	CML		28	D1
5	+REF		29	D0
6	-REF		30	DVDD
7	AGND		31	DVDD
8	AGND		32	CLK
9	DGND		33	DGND
10	OV		34	DGND
11	D13		35	$\overline{\text{OE}}$
12	D12		36	$\overline{\text{WR}}$
13	D11		37	$\overline{\text{CS}}$
14	DVDD		38	NC
15	DGND		39	NC
16	D10		40	A1
17	D9		41	A0
18	D8		42	DVDD
19	D7		43	AVDD
20	DVDD		44	AGND
21	D6		45	AGND
22	D5		46	AGND
23	D4		47	AVDD
24	D3		48	+IN

NC = No connection

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 12

Terminal symbol	I/O	Description
A0; A1	I	Address input.
AGND		Analog ground.
AVDD		Analog power supply.
CLK	I	Clock input.
CML		Reference midpoint. This pin requires a 0.1 μ F capacitor to AGND.
$\overline{\text{CS}}$	I	Chip select input. Active low.
DGND		Digital ground.
DVDD		Digital power supply.
D0 – D13	I/O	Data inputs / outputs.
NC		No connection. Do not use. Reserved.
+IN	I	Positive differential analog input.
-IN	I	Negative differential analog input.
$\overline{\text{OE}}$	I	Output enable. Active low.
OV	O	Out of range output
+REF	O	Positive reference output. This pin requires a 0.1 μ F capacitor to AGND.
-REF	O	Negative reference output. This pin requires a 0.1 μ F capacitor to AGND.
VBG	I	Reference input. This pin requires a 1 μ F capacitor to AGND
$\overline{\text{WR}}$	I	Write signal. Active low.

FIGURE 2. Terminal connections – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 13

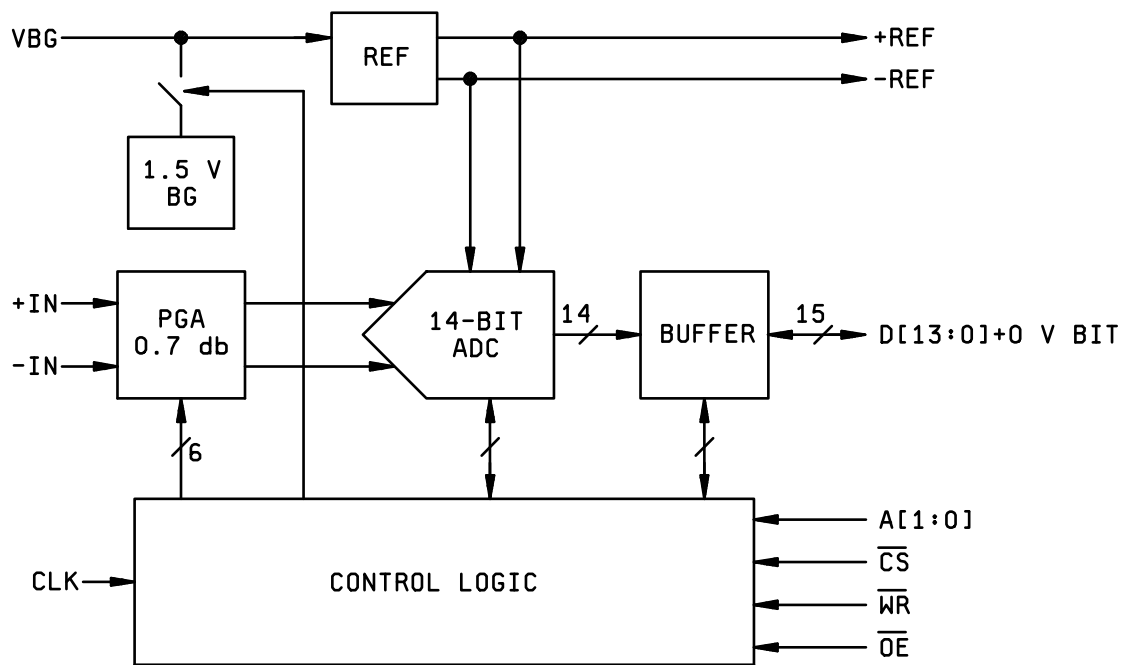
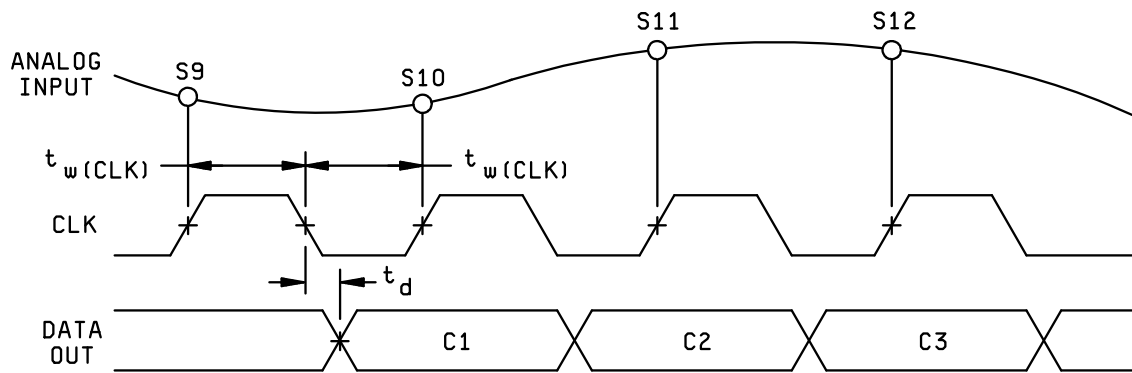


FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 14

Sample timing waveform

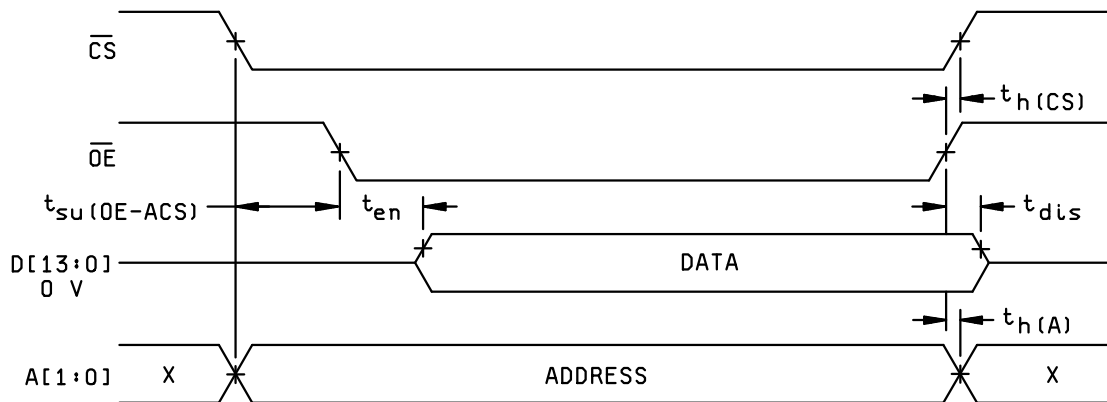


NOTE: The device core is based on a pipeline architecture with a dormancy of 9.5 samples. The conversion results appear on the digital output of 9.5 clock cycles after the input signal was sampled. The parallel interface of the device features 3-state buffers making it possible to directly connect it to a data bus. The output buffers are enabled by driving the OE input low. Besides the sample results, it is also possible to read the values of the control register, the PGA register, and the control register. Which register is read is determined by the address inputs A1, A0. The device results are available at address 0.

FIGURE 4. Timing diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 15

Read timing waveform



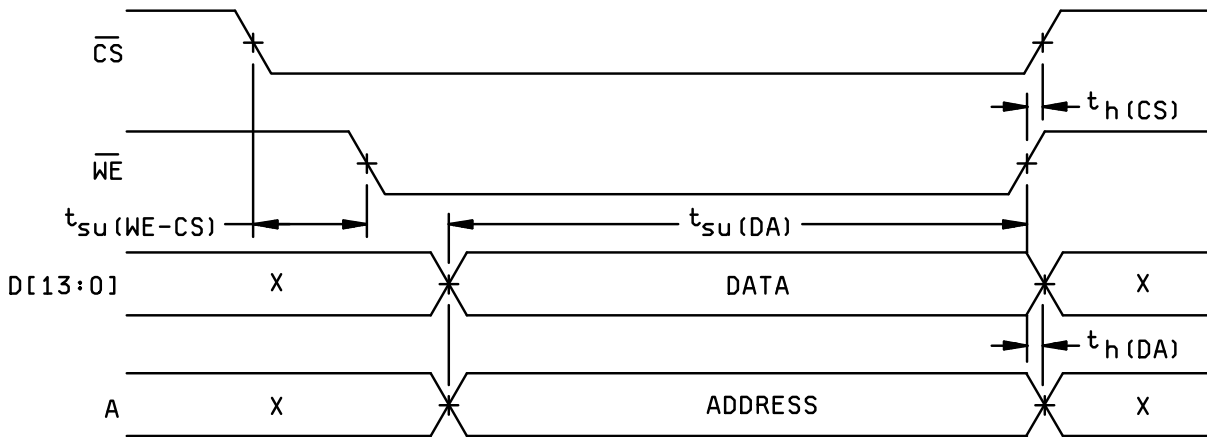
Test <u>1/</u>	Symbol	Limit		Unit
		Min	Max	
Load capacitance	C_L		15	pF
Address and chip select setup time	$t_{su}(\overline{OE}-ACS)$	4		ns
Output enable	t_{en}		15	ns
Output disable	t_{dis}	10 typical		ns
Address hold time	$t_h(A)$	1		ns
Chip select hold time	$t_h(CS)$	0		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 16

Write timing waveform



Test <u>1</u> /	Symbol	Limit		Unit
		Min	Max	
Load capacitance	CL		15	pF
Chip select setup time	$t_{su}(WE-CS)$	4		ns
Data and address setup time	$t_{su}(DA)$	29		ns
Data and address hold time	$t_h(DA)$	0		ns
Chip select hold time	$t_h(CS)$	0		ns
Wide pulse duration high	$t_{WH}(WE)$	15		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 17

Registers

The device contains several registers. The A register is selected by the values of bits A1 and A0:

A1	A0	Register
0	0	Conversion result
0	1	PGA
1	0	Offset
1	1	Control

TABLE A and B describe how to read the conversion results and how to configure the data converter. The default values (where applicable) show the state after a power-on reset.

TABLE A. Conversion result register, Address 0, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	MSB	---	---	---	---	---	---
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB

The output can be configured for two's complement or straight binary format (see D11 / control register).

The output code is given by:

2's complement:	Straight binary:
-8192 at $\Delta IN = -\Delta REF$	0 at $\Delta IN = -\Delta REF$
0 at $\Delta IN = 0$	8192 at $\Delta IN = 0$
8191 $\Delta IN = +\Delta REF - 1 \text{ LSB}$	16383 at $\Delta IN = +\Delta REF - 1 \text{ LSB}$
1 LSB = $2\Delta REF / 16384$	

TABLE B. PGA gain register, Address 1, Read / Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	X
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	G2	G1	G0
Default	0	0	0	0	0	0	0

The PGA gain is determined by writing to G2-0.

Gain (dB) = 1 dB x G2-0 maximum = 7 dB. The range of G2-0 is to 0 to 7.

FIGURE 5. Principles of operation.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 18

Registers – Continued.

TABLE C. Offset register, Address 2, Read/Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	MSB
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB
Default	0	0	0	0	0	0	0

NOTE: The offset correction range is from –128 to 127 LSB. This value is added to the conversion results from the device.

TABLE D. Control Register, Address 3, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES

TABLE E. Control Register, Address 3, Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0

PWD:	Power down	0 = normal operation	1 = power down
REF:	Reference select	0 = internal reference	1 = external reference
FOR:	Output format	0 = straight binary	1 = 2's complement
TM2-0:	Test mode	000 = normal operation	
		001 = both inputs = -REF	
		010 = +IN at VCM (voltage at CML pin), -IN at –REF	
		011 = +IN at +REF, -IN at –REF	
		100 = normal operation	
		101 = both inputs = +REF	
		110 = +IN at –REF, -IN at VCM (voltage at CML pin)	
		111 = +IN at –REF, -IN at +REF	
OF:	Offset correction	0 = enable	1 = disable
RES	Reserved	Must be set to 0	

FIGURE 5. Principles of operation – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 19

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/03608-01XE	01295	THS1401QE	THS1401QPHPEP
V62/03608-02XE	01295	THS1403QE	THS1403QPHPEP
V62/03608-03XE	01295	THS1408ME	THS1408MPHPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
		REV C	PAGE 20