

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate paragraphs to current requirements. - CFS	08-02-25	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	14-08-25	Thomas M. Hess
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	20-05-26	Muhammad A. Akbar
D	Update boilerplate paragraphs to current requirements. - DRH	26-07-02	Muhammad A. Akbar



Prepared in accordance with ASME Y14.24
The CAGE Code 16236 entity has been changed to DLA Weapons Support (Columbus).

Vendor item drawing

REV																						
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PMIC N/A	PREPARED BY Phu H. Nguyen		DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
Original date of drawing YY-MM-DD 03-01-21	CHECKED BY Phu H. Nguyen		TITLE MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/03616	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance floating-point digital signal processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/03616</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	320C32-50EP	Digital signal processor
02	320C32-60EP	Digital signal processor

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	144	JEDEC MS-022	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to +7.0 V <u>2/</u>
DC input voltage range (V_{IN})	-0.3 V to +7.0 V
DC output voltage range (V_O)	-0.3 V to +7.0 V
Continuous power dissipation (P_D)	1.95 W <u>3/</u>
Operating case temperature range (T_C)	-55°C to +125°C
Storage temperature range (T_{STG})	-55°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (DV_{DD}, V_{DDL})	+4.75 V to +5.25 V
High-level input voltage range (V_{IH}):	
CLKIN	+2.6 V to $V_{DD} + 0.3$ V <u>6/</u>
All other inputs	+2.0 V to $V_{DD} + 0.3$ V <u>6/</u>
Low-level input voltage range (V_{IL})	-0.3 V to 0.8 V <u>6/</u>
Maximum high-level output current (I_{OH})	-300 μ A
Maximum low-level output current (I_{OL})	+2 mA
Case operating temperature range (T_C)	-55°C to +125°C <u>7/</u>

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ All voltage values are with respect to V_{SS} .
- 3/ This value calculated for the C32-40. Actual operating power is less. This value was obtained under specially produced worst-case test conditions which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external bus at the maximum rate possible. See normal (I_{DD}) current specification in table I.
- 4/ All input and output voltage levels are TTL compatible.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 6/ Maximum V_{IH} and minimum V_{IL} are not production tested.
- 7/ T_C MAX at maximum rated operating conditions at any point on case. T_C MIN at initial (time zero) power-up.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagram. The block diagram shall be as specified on figure 3.

3.5.4 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as specified on figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	I _{OH} = -300 μA	5.0 V	25°C	All	3.0		V
			4.75 V	-55°C to +125°C		2.4		
Low level output voltage	V _{OL}	I _{OL} = 2 mA	5.0 V	25°C			0.3	V
			4.75 V	-55°C to +125°C			0.8	
High impedance state output current	I _{OZ}		5.25 V	-55°C to +125°C		-20	20	μA
Input current	I _I	V _I = 0 to V _{DD}	<u>2</u> /	-55°C to +125°C		-10	10	μA
Supply current	I _{DD}	f _X = 50 MHz	5.25 V	25°C			200	mA
				-55°C to +125°C			425	
		f _X = 60 MHz	5.25 V	25°C			225	
				-55°C to +125°C			475	
		Standby, IDLE2, CLKIN shut off	5.0 V	25°C			50	μA
Input capacitance	C _I	CLKIN	<u>2</u> /	-55°C to +125°C			25	pF
		All other inputs <u>3</u> /					15	
Output capacitance	C _O	<u>3</u> /	<u>2</u> /	-55°C to +125°C			20	

Timing for CLKIN [Q=t_{c(CI)}]

Fall time, CLKIN <u>3/</u> <u>4/</u>	t _{f(CI)}	See figure 4, 1	<u>2/</u>	-55°C to +125°C	1		5	ns
					2		4	
Pulse duration, CLKIN low <u>4/</u>	t _{w(CIL)}	See figure 4, 2 Q = min			1	7		ns
					2	6		
Pulse duration, CLKIN high <u>4/</u>	t _{w(CIH)}	See figure 4, 3 Q = min			1	8		ns
					2	6		
Rise time, CLKIN <u>3/</u> <u>4/</u>	t _{r(CI)}	See figure 4, 4			1		5	ns
					2		4	
Cycle time, CLKIN <u>4/</u>	t _{c(CI)}	See figure 4, 5			1	20	303	ns
					2	16.67	303	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Switching characteristics for H1 and H3 over recommended operating conditions (unless otherwise noted)								
Fall time, H1/H3	t _{r(H)}	See figure 4, 6	<u>2/</u>	-55°C to +125°C	1		3	ns
					2		3	
Pulse duration, H1/H3 low	t _{w(HL)}	See figure 4, 7			1	Q-5		ns
					2	Q-4		
Pulse duration, H1/H3 high	t _{w(HH)}	See figure 4, 8			1	Q-6		ns
					2	Q-5		
Rise time, H1/H3	t _{r(H)}	See figure 4, 9			1		3	ns
					2		3	
Delay time, H1/H3 low to H1/H3 high	t _{d(HL-HH)}	See figure 4, 9.1			1	0 <u>3/</u>	4	ns
					2	0 <u>3/</u>	4	
Cycle time, H1/H3	t _{c(H)}	See figure 4, 10			1	40	606	ns
					2	33.33	606	
Memory-read-cycle and memory-write-cycle timing (<u>STRBx</u>)								
Delay time, H1 low to <u>STRBx</u> low	t _{d(H1L-SL)}	See figure 4, 11	<u>2/</u>	-55°C to +125°C	1	0 <u>3/</u>	9	ns
					2	0 <u>3/</u>	7	
Delay time, H1 low to <u>STRBx</u> high	t _{d(H1L-SH)}	See figure 4, 12			1	0 <u>3/</u>	9	ns
					2	0 <u>3/</u>	7	
Delay time, H1 high to <u>R/ W</u> low (read)	t _{d(H1H-RWL)}	See figure 4, 13			1	0 <u>3/</u>	9	ns
					2	0 <u>3/</u>	8	
Delay time, H1 low to A valid	t _{d(H1L-A)}	See figure 4, 14			1	0 <u>3/</u>	9	ns
					2	0 <u>3/</u>	7	
Setup time, D valid before H1 low (read)	t _{su(D)R}	See figure 4, 15			1	10		ns
					2	10		
Hold time, D after H1 low (read)	t _{h(D)R}	See figure 4, 16			1	0		ns
					2	0		
Setup time, <u>RDY</u> before H1 low	t _{d(RDY)}	See figure 4, 17			1	19		ns
			2	17				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Hold time, $\overline{\text{RDY}}$ after H1 low	$t_{\text{h(RDY)}}$	See figure 4, 18	$\underline{2/}$	-55°C to +125°C	1	0		ns
					2	0		
Delay time, H1 high to R/ $\overline{\text{W}}$ high (write)	$t_{\text{d(H1H-RWH)}}$	See figure 4, 19			1		9	ns
					2		8	
Valid time, D after H1 low (write)	$t_{\text{v(D)W}}$	See figure 4, 20			1		14	ns
					2		12	
Hold time, D after H1 high (write) $\underline{4/}$	$t_{\text{h(D)W}}$	See figure 4, 21			1	0 $\underline{3/}$		ns
					2	0 $\underline{3/}$		
Delay time, H1 high to A valid on back-to-back write cycles	$t_{\text{d(H1H-A)}}$	See figure 4, 22			1		9	ns
					2		8	

Memory-read-cycle timing using $\overline{\text{IOSTRB}}$

Delay time, H3 low to $\overline{\text{IOSTRB}}$ low	$t_{\text{d}}(\text{H3L-IOSL})$	See figure 4, 11.1	$\underline{2/}$	-55°C to +125°C	1	0 $\underline{3/}$	9	ns
					2	0 $\underline{3/}$	8	
Delay time, H3 low to $\overline{\text{IOSTRB}}$ high	$t_{\text{d}}(\text{H3L-IOSH})$	See figure 4, 12.1			1	0 $\underline{3/}$	9	ns
					2	0 $\underline{3/}$	8	
Delay time, H1 low to $\overline{\text{R/W}}$ high	$t_{\text{d}}(\text{H1L-RWL})$	See figure 4, 13.1			1	0 $\underline{3/}$	9	ns
					2	0 $\underline{3/}$	8	
Delay time, H1 low to A valid	$t_{\text{d}}(\text{H1L-A})$	See figure 4, 14.1			1	0 $\underline{3/}$	9	ns
					2	0 $\underline{3/}$	8	
Setup time, D before H1 high	$t_{\text{su}}(\text{D})_{\text{R}}$	See figure 4, 15.1			1	10		ns
					2	9		
Hold time, D after H1 high	$t_{\text{h}}(\text{D})_{\text{R}}$	See figure 4, 16.1			1	0		ns
					2	0		
Setup time, $\overline{\text{RDY}}$ before H1 high	$t_{\text{su}}(\text{RDY})$	See figure 4, 17.1			1	8		ns
					2	7		
Hold time, $\overline{\text{RDY}}$ after H1 high	$t_{\text{h}}(\text{RDY})$	See figure 4, 18.1			1	0		ns
					2	0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Memory-write-cycle timing using $\overline{\text{IOSTRB}}$								
Delay time, H1 low to R/ $\overline{\text{W}}$ low	$t_{d(\text{H1L-RWH})}$	See figure 4, 23	<u>2/</u>	-55°C to +125°C	1	0 <u>3/</u>	9	ns
					2	0 <u>3/</u>	8	
Valid time, D after H1 high	$t_{v(\text{D})\text{W}}$	See figure 4, 24			1		14	ns
					2		12	
Hold time, D after H1 low	$t_{h(\text{D})\text{W}}$	See figure 4, 25			1	0		ns
					2	0		
Timing for XF0 and XF1 when executing LDFI or LDII								
Delay time, H3 high to XF0 low	$t_{d(\text{H3H-XF0L})}$	See figure 4, 38	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Setup time, XF1 before H1 low	$t_{su(\text{XF1})}$	See figure 4, 39			1	9		ns
					2	8		
Hold time, XF1 after H1 low	$t_{h(\text{XF1})}$	See figure 4, 40			1	0		ns
					2	0		
Timing for XF0 when executing STFI or STII <u>5/</u>								
Delay time, H3 high to XF0 high	$t_{d(\text{H3H-XF0H})}$	See figure 4, 41	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Timing for XF0 and XF1 when executing SIGI								
Delay time, H3 high to XF0 low	$t_{d(\text{H3H-XF0L})}$	See figure 4, 41.1	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Delay time, H3 high to XF0 high	$t_{d(\text{H3H-XF0H})}$	See figure 4, 42			1		12	ns
					2		11	
Setup time, XF1 before H1 low	$t_{su(\text{XF1})}$	See figure 4, 43			1	9		ns
					2	8		
Hold time, XF1 after H1 low	$t_{h(\text{XF1})}$	See figure 4, 44			1	0		ns
					2	0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for loading XF register when configured as an output pin								
Valid time, H3 high to XF valid	t _v (H3H-XF)	See figure 4, 45	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Timing of XF changing from output to input mode								
Hold time, XF after H3 high <u>3/</u>	t _h (H3H-XF01)	See figure 4, 46	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Setup time, XF before H1 low	t _{su} (XF)	See figure 4, 47			1	9		ns
					2	8		
Hold time, XF after H1 low	t _h (XF)	See figure 4, 48			1	0		ns
					2	0		
Timing of XF changing from input to output mode								
Delay time, H3 high to XF switching from input to output	t _d (H3H-XFIO)	See figure 4, 49	<u>2/</u>	-55°C to +125°C	1		17	ns
					2		15	
Timing for $\overline{\text{RESET}}$ [Q = t _c (CI)]								
Setup time, $\overline{\text{RESET}}$ before CLKIN low	t _{su} (RESET)	See figure 4, 50	<u>2/</u>	-55°C to +125°C	1	10	Q <u>3/</u>	ns
					2	7	Q <u>3/</u>	
Delay time, CLKIN high to H1 high	t _d (CLKINH- H1H)	See figure 4, 51			1	2	10	ns
					2	2	10	
Delay time, CLKIN high to H1 low	t _d (CLKINH- H1L)	See figure 4, 52			1	2	10	ns
					2	2	10	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after 10 H1 clock cycles	t _{su} (RESETH- H1L)	See figure 4, 53			1	7		ns
					2	6		
Delay time, CLKIN high to H3 low	t _d (CLKINH- H3L)	See figure 4, 54			1	2	10	ns
					2	2	10	
Delay time, CLKIN high to H3 high	t _d (CLKINH- H3H)	See figure 4, 55			1	2	10	ns
					2	2	10	
Disable time, H1 high to D in high-impedance state <u>3/</u>	t _{dis} (H1H-D)	See figure 4, 56			1		12	ns
					2		11	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{\text{RESET}}$ [Q = t _{c(CI)}] – Continued								
Disable time, H3 low to A in high-impedance state <u>3/</u>	t _{dis} (H3HL-A)	See figure 4, 57	<u>2/</u>	-55°C to +125°C	1		9	ns
					2		9	
Delay time, H3 high to control signals high <u>3/</u>	t _d (H3H-CONTROLH)	See figure 4, 58.1	<u>2/</u>	-55°C to +125°C	1		8	ns
					2		7	
Delay time, H1 high to R/ $\overline{\text{W}}$ high <u>3/</u>	t _d (H1H-RWH)	See figure 4, 58.2	<u>2/</u>	-55°C to +125°C	1		8	ns
					2		7	
Delay time, H1 high to $\overline{\text{IACK}}$ high <u>3/</u>	t _d (H1H-IACKH)	See figure 4, 59	<u>2/</u>	-55°C to +125°C	1		8	ns
					2		7	
Disable time, $\overline{\text{RESET}}$ low to asynchronously reset signals in high impedance <u>3/</u>	t _{dis} ($\overline{\text{RESETL}}$ -ASYNCH)	See figure 4, 60	<u>2/</u>	-55°C to +125°C	1		17	ns
					2		14	
Timing for $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ interrupt response [P = t _{c(H)}]								
Setup time, $\overline{\text{INT3}}$ - $\overline{\text{INT0}}$ before H1 low	t _{su} (INT)	See figure 4, 61	<u>2/</u>	-55°C to +125°C	1		10	ns
					2		8	
Pulse duration of interrupt to assure only one interrupt seen for level-triggered interrupts	t _w (INT)	See figure 4, 62.1	<u>2/</u>	-55°C to +125°C	1	P	2P <u>3/</u>	ns
					2	P	2P <u>3/</u>	
Pulse duration, of interrupt for edge-triggered interrupts <u>3/</u>	t _w (INT)	See figure 4, 62.2	<u>2/</u>	-55°C to +125°C	1	P		ns
					2	P		
Timing for $\overline{\text{IACK}}$ <u>6/ 7/</u>								
Delay time, H1 high to $\overline{\text{IACK}}$ low	t _d (H1H-IACKL)	See figure 4, 63	<u>2/</u>	-55°C to +125°C	1		7	ns
					2		6	
Delay time, H1 high to $\overline{\text{IACK}}$ high	t _d (H1H-IACKH)	See figure 4, 64	<u>2/</u>	-55°C to +125°C	1		7	ns
					2		6	

See footnotes at end of table.

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Test	Symbol	Conditions		V _{DD}	Temperature, T _C	Device type	Limits		Unit					
							Min	Max						
Serial port timing [P = t _{c(H)}]														
Delay time, H1 high to internal CLKX/R high/low	t _{d(H1-SCK)}	See figure 4, 65		<u>2/</u>	-55°C to +125°C	1		10	ns					
						2		8						
Cycle time, CLKX/R	t _{c(SCK)}	See figure 4, 66	CLKX/R ext			1	2.6P		ns					
			CLKX/R int			2	2.6P							
			Pulse duration, CLKX/R high/low			t _{w(SCK)}	See figure 4, 67	CLKX/R ext	1	2P	(2 ³²)P	ns		
								CLKX/R int	2	2P	(2 ³²)P			
Rise time, CLKX/R	t _{r(SCK)}	See figure 4, 68				CLKX/R ext	1	P+10		ns				
							2	P+10						
							Fall time, CLKX/R	t _{f(SCK)}	See figure 4, 69		1	[t _{c(SCK)} /2]-5	[t _{c(SCK)} /2]+5	ns
											2	[t _{c(SCK)} /2]-5	[t _{c(SCK)} /2]+5	
Delay time, CLKX to DX valid	t _{d(DX)}	See figure 4, 70	CLKX ext			1		6	ns					
			CLKX int			2		5						
			Setup time, DR before CLKR low			t _{su(DR)}	See figure 4, 71	CLKR ext	1		24	ns		
								CLKR int	2		20			
Hold time, DR from CLKR low	t _{h(DR)}	See figure 4, 72						CLKR ext	1		16	ns		
								CLKR int	2		15			
			Setup time, DR before CLKR low			t _{su(DR)}	See figure 4, 71	CLKR ext	1	9		ns		
								CLKR int	2	8				
Hold time, DR from CLKR low	t _{h(DR)}	See figure 4, 72						CLKR ext	1	17		ns		
								CLKR int	2	15				
			Hold time, DR from CLKR low			t _{h(DR)}	See figure 4, 72	CLKR ext	1	7		ns		
								CLKR int	2	6				
Setup time, DR before CLKR low	t _{su(DR)}	See figure 4, 71						CLKR ext	1	0		ns		
								CLKR int	2	0				

See footnotes at end of table.

DLA WEAPONS SUPPORT COLUMBUS, OHIO		SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
			REV D	PAGE 11

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit	
						Min	Max		
Serial port timing [P = t _{c(H)}] - Continued									
Delay time, CLKX to internal FSX high/low	t _{d(FSX)}	See figure 4, 73	CLKX ext	<u>2/</u>	-55°C to +125°C	1		22	ns
						2		20	
			CLKX int			1		15	ns
						2		14	
Setup time, FSR before CLKR low	t _{su(FSR)}	See figure 4, 74	CLKR ext			1	7		ns
						2	6		
			CLKR int			1	7		ns
						2	6		
Hold time, FSX/R input from CLKX/R low	t _{h(FS)}	See figure 4, 75	CLKX/R ext			1	7		ns
						2	6		
			CLKX/R int			1	0		ns
						2	0		
Setup time, external FSX before CLKX <u>3/</u>	t _{su(FSX)}	See figure 4, 76	CLKX ext			1	8-P	[t _{c(SCK)/2}]-10	ns
						2	8-P	[t _{c(SCK)/2}]-10	
			CLKX int			1	22-P	t _{c(SCK)/2}	ns
						2	22-P	t _{c(SCK)/2}	
Delay time, CLKX to first DX bit, FSX precedes CLKX high <u>3/</u>	t _{d(CH-DX)V}	See figure 4, 77	CLKX ext			1		24	ns
						2		20	
			CLKX int			1		14	ns
						2		12	
Delay time, FSX to first DX bit, CLKX precedes FSX <u>3/</u>	t _{d(FSX-DX)V}	See figure 4, 78				1		24	ns
						2		20	
Delay time, CLKX high to DX high impedance following last data bit <u>3/</u>	t _{d(DXZ)}	See figure 4, 79				1		14	ns
						2		12	

See footnotes at end of table.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV D	PAGE 12

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ [P = t _{c(H)}] <u>8/</u>								
Setup time, $\overline{\text{HOLD}}$ before H1 low	t _{su} (HOLD)	See figure 4, 80	<u>2/</u>	-55°C to +125°C	1	10		ns
					2	8		
Valid time, $\overline{\text{HOLDA}}$ after H1 low	t _v (HOLDA)	See figure 4, 81			1	0 <u>3/</u>	7	ns
					2	0 <u>3/</u>	6	
Pulse duration, $\overline{\text{HOLD}}$ low	t _w (HOLD)	See figure 4, 82			1	2P		ns
					2	2P		
Pulse duration, $\overline{\text{HOLDA}}$ low <u>3/</u>	t _w (HOLDA)	See figure 4, 83			1	P-5		ns
					2	P-5		
Delay time, H1 low to $\overline{\text{STRBx}}$ high for a $\overline{\text{HOLD}}$ <u>3/</u>	t _d (H1L- SH)H	See figure 4, 84			1	0	7	ns
					2	0	6	
Delay time, H1 high to $\overline{\text{IOSTRB}}$ high for a $\overline{\text{HOLD}}$ <u>3/</u>	t _d (H1H- IOS)H	See figure 4, 84.1			1	0	7	ns
					2	0	6	
Disable time, H1 low to $\overline{\text{STRBx}}$ or $\overline{\text{IOSTRB}}$ high impedance state <u>3/</u>	t _{dis} (H1L-S)	See figure 4, 85			1	0	8	ns
					2	0	7	
Enable time, H1 low to $\overline{\text{STRBx}}$ or $\overline{\text{IOSTRB}}$ active <u>3/</u>	t _{en} (H1L-S)	See figure 4, 86			1	0	7	ns
					2	0	6	
Disable time, H1 low to R/ $\overline{\text{W}}$ in the high- impedance state <u>3/</u>	t _{dis} (H1L- RW)	See figure 4, 87			1	0	8	ns
					2	0	7	
Enable time, H1 low to R/ $\overline{\text{W}}$ (active) <u>3/</u>	t _{en} (H1L- RW)	See figure 4, 88			1	0	7	ns
					2	0	6	
Disable time, H1 low to A high-impedance state <u>3/</u>	t _{dis} (H1L-A)	See figure 4, 89			1	0	8	ns
					2	0	7	
Enable time, H1 low to A valid <u>3/</u>	t _{en} (H1L-A)	See figure 4, 90			1	0	12	ns
					2	0	11	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions	V _{DD}	Temperature, T _C	Device type	Limits		Unit
						Min	Max	
Timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ [P = t _{c(H)}] – Continued <u>8/</u>								
Disable time, H1 high to D disabled in the high- impedance state <u>3/</u>	t _{dis(H1H-D)}	See figure 4, 91	<u>2/</u>	-55°C to +125°C	1	0	8	ns
					2	0	7	
Timing for peripheral pin configured as general-purpose I/O								
Setup time, general- purpose input before H1 low	t _{su(GPIOH1L)}	See figure 4, 92	<u>2/</u>	-55°C to +125°C	1	9		ns
					2	8		
Hold time, general- purpose input after H1 low	t _{h(GPIOH1L)}	See figure 4, 93	<u>2/</u>	-55°C to +125°C	1	0		ns
					2	0		
Delay time, general- purpose output after H1 high	t _{d(GPIOH1H)}	See figure 4, 94	<u>2/</u>	-55°C to +125°C	1		10	ns
					2		8	
Timing for peripheral pin changing from general-purpose output to input mode								
Hold time, after H1 high <u>3/</u>	t _{h(H1H)}	See figure 4, 95	<u>2/</u>	-55°C to +125°C	1		12	ns
					2		11	
Setup time, peripheral pin before H1 low	t _{su(GPIOH1L)}	See figure 4, 96	<u>2/</u>	-55°C to +125°C	1	9		ns
					2	8		
Hold time, peripheral pin after H1 low	t _{h(GPIOH1L)}	See figure 4, 97	<u>2/</u>	-55°C to +125°C	1	0		ns
					2	0		
Timing for peripheral pin changing from general-purpose input to output mode								
Delay time, H1 high to peripheral pin switching from input to output	t _{d(GPIOH1H)}	See figure 4, 98	<u>2/</u>	-55°C to +125°C	1		10	ns
					2		8	

See footnotes at end of table.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions		V _{DD}	Temperature, T _C	Device type	Limits		Unit
							Min	Max	
Timing for timer pin [P = t _{c(H)}]									
Setup time, TCLK external before H1 low <u>9/</u>	t _{su} (TCLKH1L)	See figure 4, 99		<u>2/</u>	-55°C to +125°C	1	8		ns
						2	6		
Hold time, TCLK external after H1low <u>9/</u>	t _h (TCLKH1L)	See figure 4, 100				1	0		ns
						2	0		
Delay time, H1 high to TCLK internal valid	t _d (TCLKH1H)	See figure 4, 101				1		9	ns
						2		8	
Cycle time, TCLK cycle time <u>10/</u>	t _c (TCLK)	See figure 4, 102	TCLK external <u>3/</u>			1	2.6P		ns
			2			2.6P			
			TCLK internal			1	2P	(2 ³²)P <u>3/</u>	ns
						2	2P	(2 ³²)P <u>3/</u>	
Pulse duration, TCLK high/low <u>10/</u>	t _w (TCLK)	See figure 4, 103	TCLK external <u>3/</u>			1	P+10		ns
			2			P+10			
			TCLK internal			1	[t _c (TCLK)/2]-5	[t _c (TCLK)/2]+5	ns
						2	[t _c (TCLK)/2]-5	[t _c (TCLK)/2]+5	
Timing for <u>SHZ</u> pin [Q = t _{c(Cl)}]									
Disable time, <u>SHZ</u> low to all O, I/O pins in the high- impedance state <u>3/</u>	t _{dis} (SHZ)	See figure 4, 104		<u>2/</u>	-55°C to +125°C	1	0	2Q	ns
						2	0	2Q	

See footnotes at end of table.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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TABLE I. Electrical performance characteristics - Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
- 3/ This value is not production tested.
- 4/ Minimum CLKIN high pulse duration at 3.3 MHz is 10ns.
- 5/ XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store is not driven until the store can execute.
- 6/ The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is extended if the bus cycle utilizes wait states.
- 7/ The $\overline{\text{IACK}}$ output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.
- 8/ $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur. The NOHOLD bit of the primary-bit-control register overwrites the $\overline{\text{HOLD}}$ signal.
- 9/ This timing parameter is applicable for a synchronous input clock.
- 10/ This timing parameter is applicable for an asynchronous input clock.

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Case X

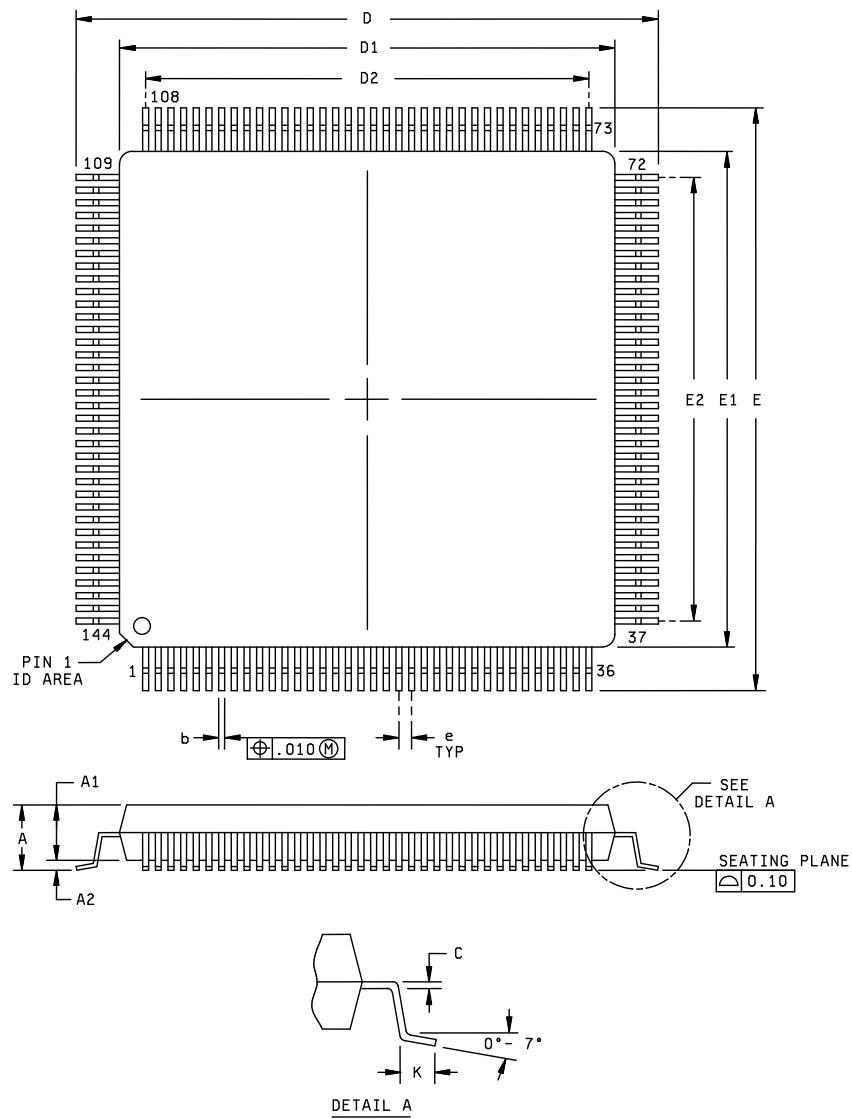


FIGURE 1. Case outlines.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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Case X

	Millimeters	
Dimension	Min	Max
A		4.10
A1	3.20	3.60
A2	0.25	
b	0.22	0.38
C	0.16	
D/E	30.95	31.45
D1/E1	27.80	28.20
D2/E2	22.75	
e	0.65	
K	0.73	1.03

FIGURE 1. Case outlines - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DR0	30	A17	59	DV _{DD}	88	IV _{SS}	117	RDY
2	DV _{DD}	31	A16	60	D31	89	D11	118	IV _{SS}
3	FSR0	32	A15	61	D30	90	DV _{DD}	119	I _{OSTRB}
4	CLKR0	33	A14	62	D29	91	D10	120	STRB0_B3 /A ₋₁
5	CLKX0	34	A13	63	D28	92	CV _{SS}	121	STRB0_B2 /A ₋₂
6	FSX0	35	CV _{SS}	64	D27	93	DV _{SS}	122	STRB0_B1
7	DX0	36	DV _{SS}	65	D26	94	V _{SSL}	123	STRB0_B0
8	IV _{SS}	37	NC	66	IV _{SS}	95	V _{SSL}	124	V _{DDL}
9	SHZ	38	A12	67	D25	96	D9	125	V _{DDL}
10	TCLK0	39	DV _{DD}	68	DV _{DD}	97	D8	126	STRB1_B3 /A ₋₁
11	TCLK1	40	A11	69	D24	98	D7	127	V _{SSL}
12	DV _{DD}	41	A10	70	D23	99	D6	128	STRB1_B2 /A ₋₂
13	EMU3	42	A9	71	D22	100	D5	129	DV _{DD}
14	EMU2	43	A8	72	NC	101	D4	130	STRB1_B1
15	V _{DDL}	44	A7	73	CV _{SS}	102	DV _{DD}	131	STRB1_B0
16	V _{DDL}	45	A6	74	DV _{SS}	103	D3	132	R/W
17	EMU1	46	DV _{DD}	75	D21	104	D2	133	PRGW
18	EMU2	47	A5	76	D20	105	D1	134	RESET
19	V _{SSL}	48	A4	77	D19	106	D0	135	CV _{SS}
20	MCBL/MP	49	A3	78	D18	107	H1	136	DV _{SS}
21	CV _{SS}	50	V _{DDL}	79	DV _{DD}	108	H3	137	XF0
22	DV _{SS}	51	V _{DDL}	80	D17	109	NC	138	XF1
23	A23	52	A2	81	D16	110	V _{SUBS}	139	IACK
24	A22	53	CV _{SS}	82	D15	111	CV _{SS}	140	INT0
25	A21	54	DV _{SS}	83	D14	112	DV _{SS}	141	INT1
26	A20	55	A1	84	D13	113	CLKIN	142	INT2
27	A19	56	V _{SSL}	85	V _{DDL}	114	HOLD _A	143	INT3
28	A18	57	V _{SSL}	86	V _{DDL}	115	HOLD	144	NC
29	DV _{DD}	58	A0	87	D12	116	DV _{DD}		

FIGURE 2. Terminal connections.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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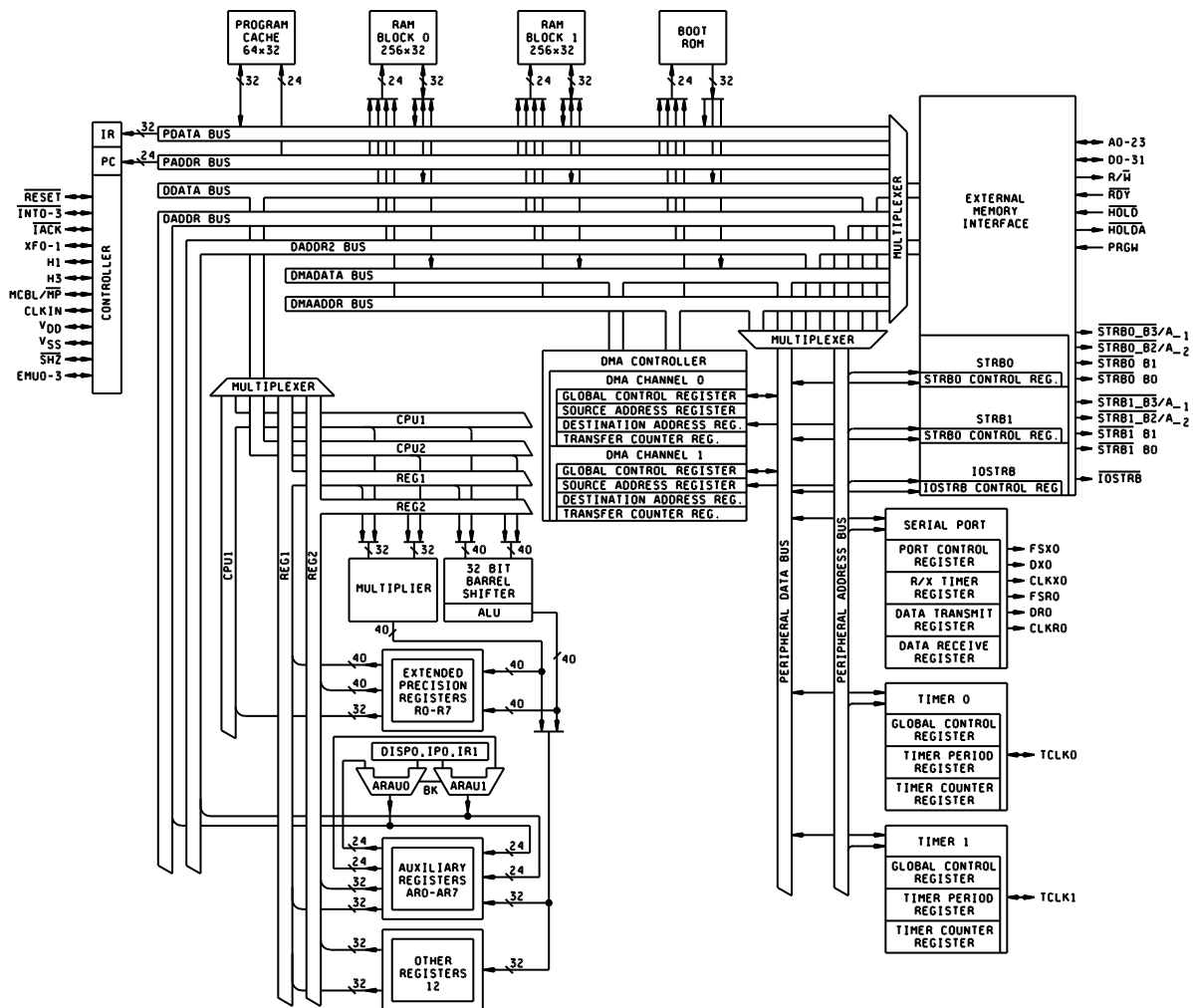


FIGURE 3. Block diagram.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV D	PAGE 20

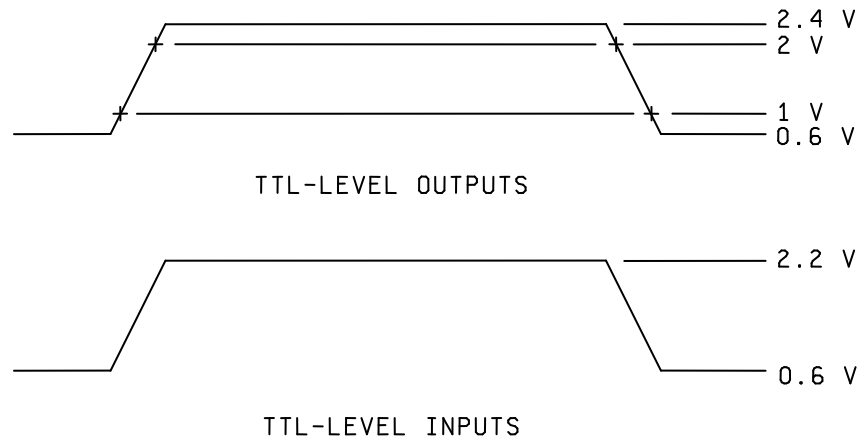


FIGURE 4. Load circuit and timing waveforms.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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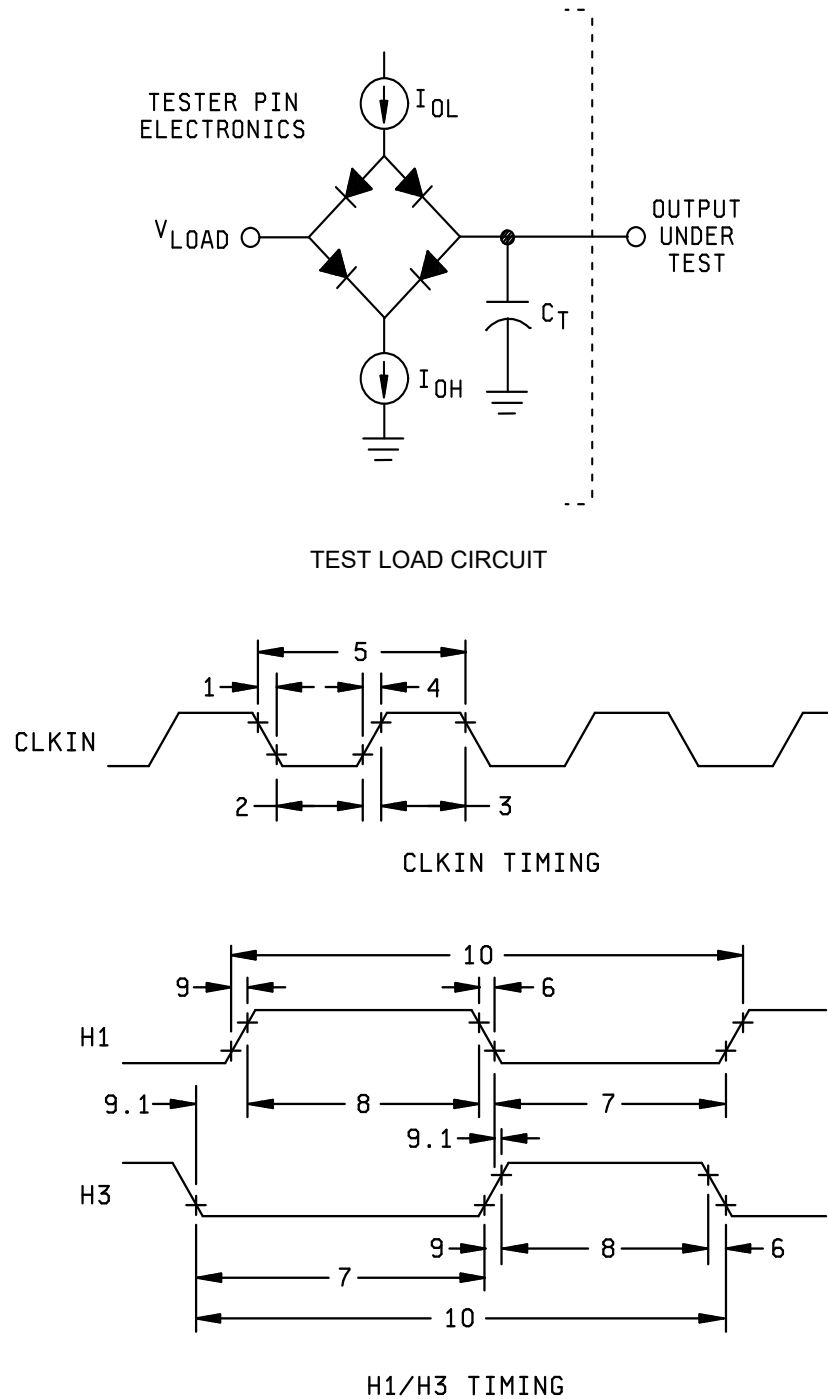
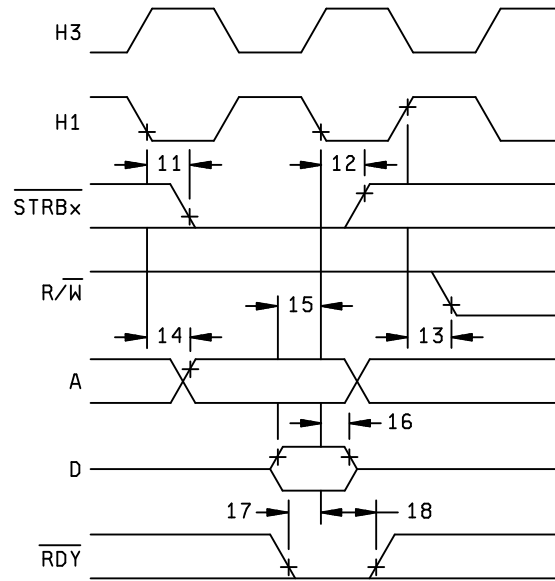
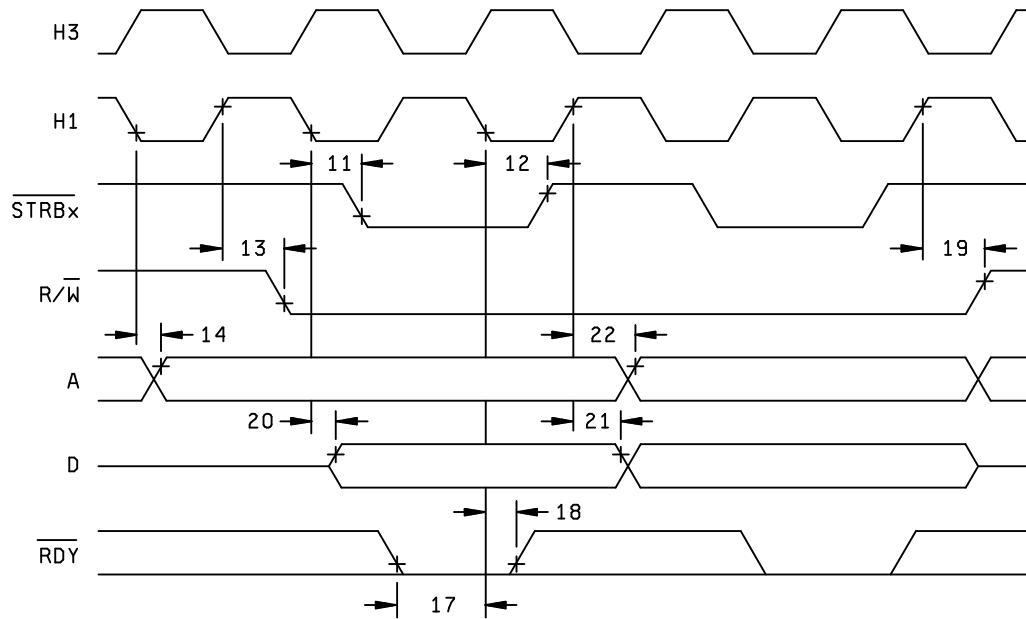


FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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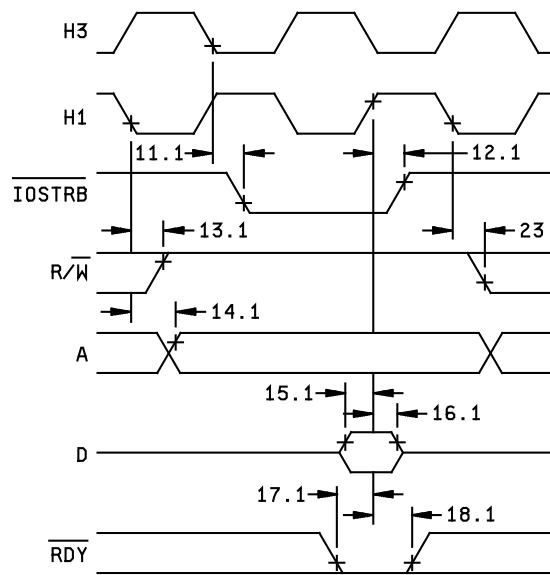
MEMORY-READ-CYCLE TIMING



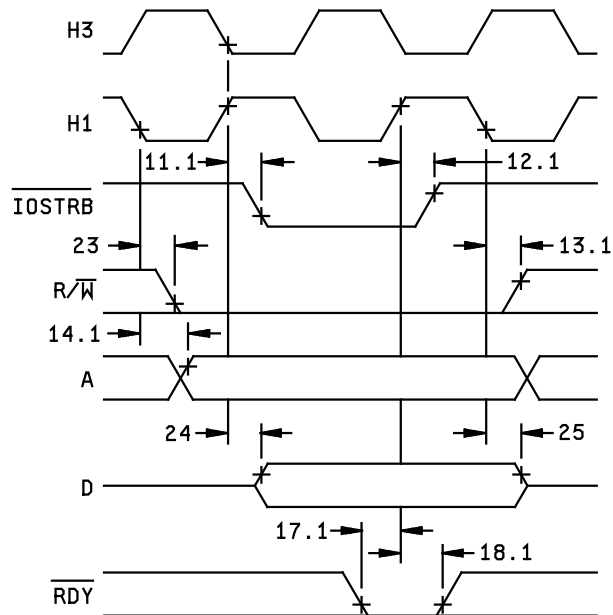
MEMORY-WRITE-CYCLE TIMING

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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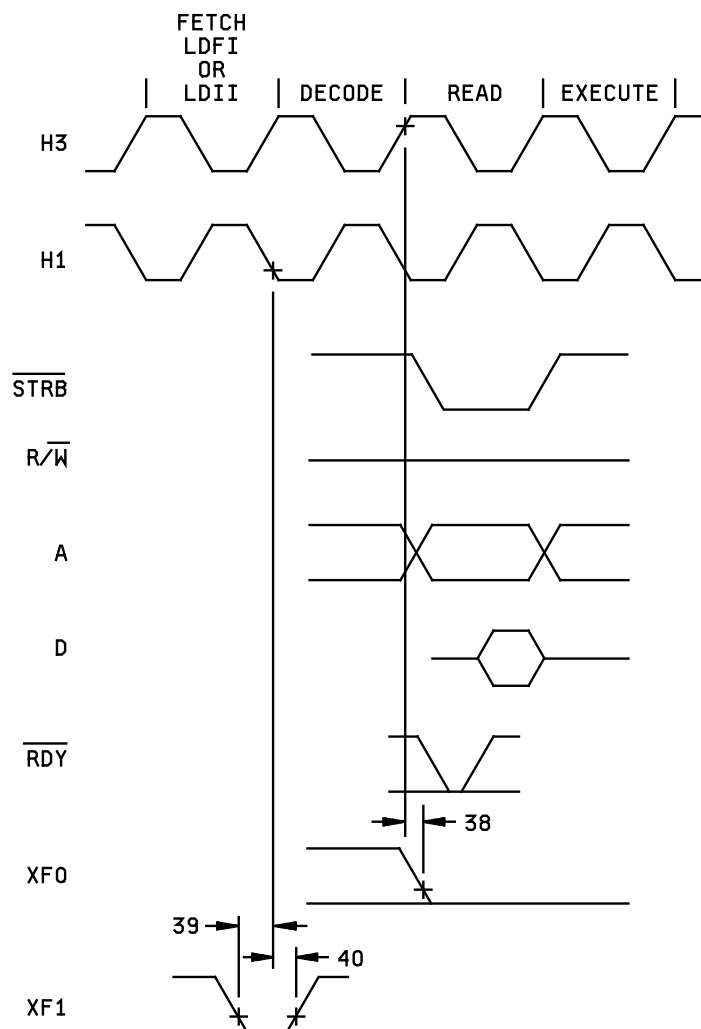
MEMORY-READ-CYCLE TIMING USING IOSTRB



MEMORY-WRITE-CYCLE TIMING USING IOSTRB

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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XF0 AND XF1 WHEN EXECUTING LDFI OR LDII

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV D	PAGE 25

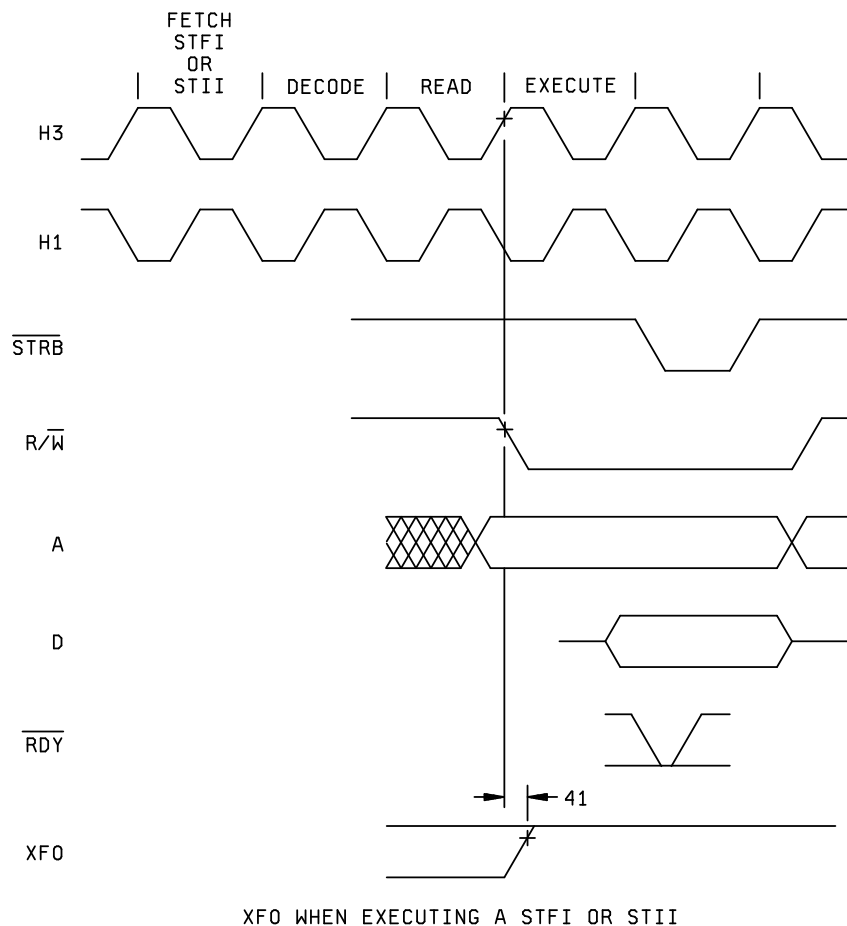
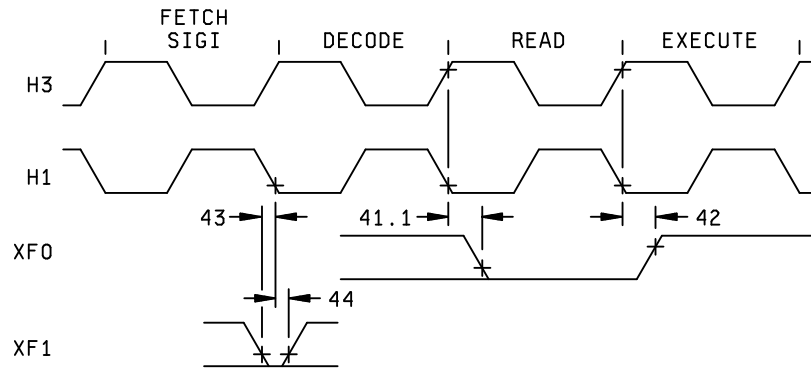
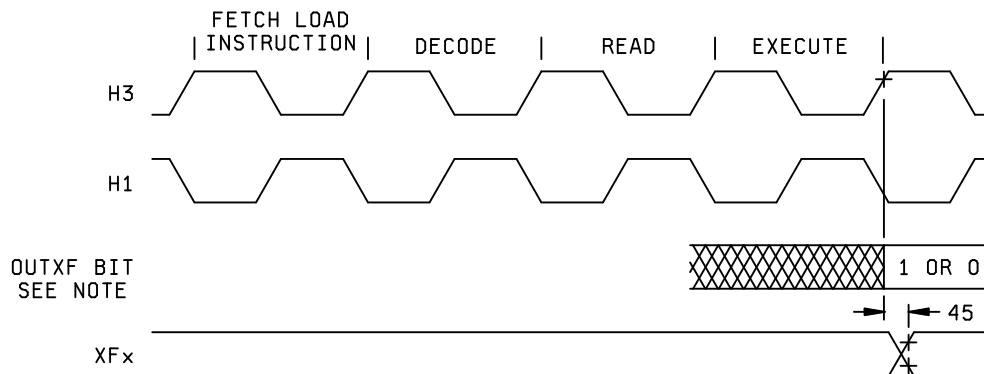


FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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XFO AND XF1 WHEN EXECUTING SIGI

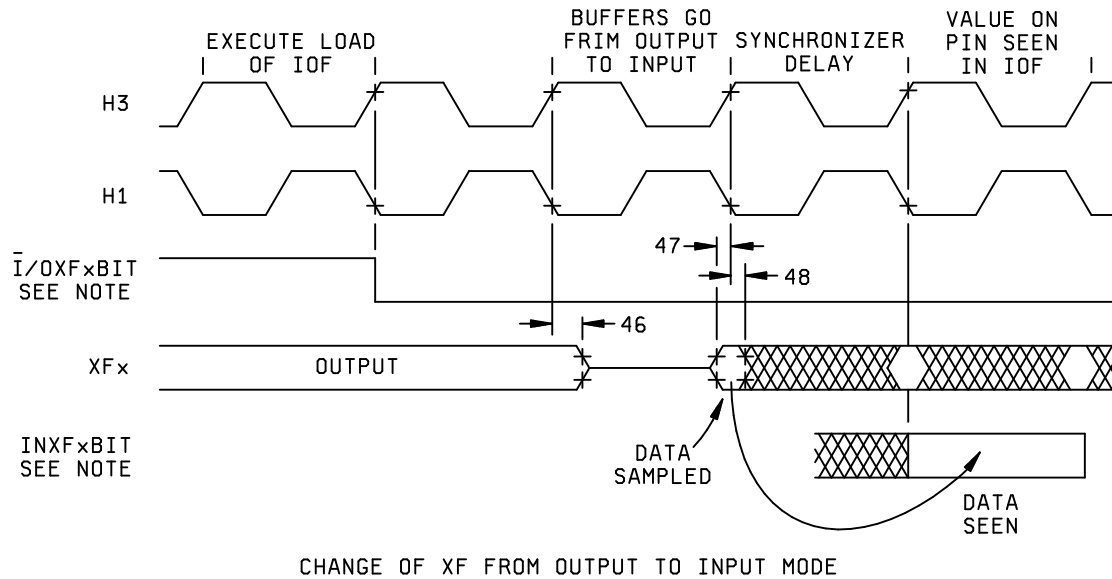


LOADING XF REGISTER WHEN CONFIGURED AS AN OUTPUT PIN

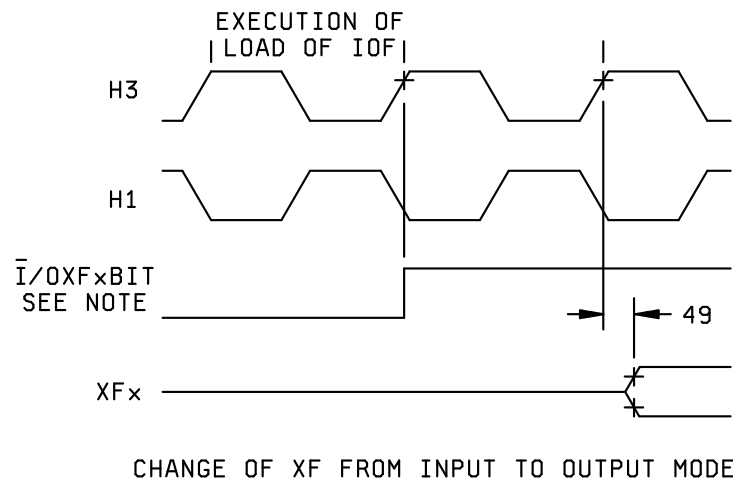
NOTE: OUTXFx represents either bit 2 or bit 6 of the IOF register.

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV D	PAGE 27



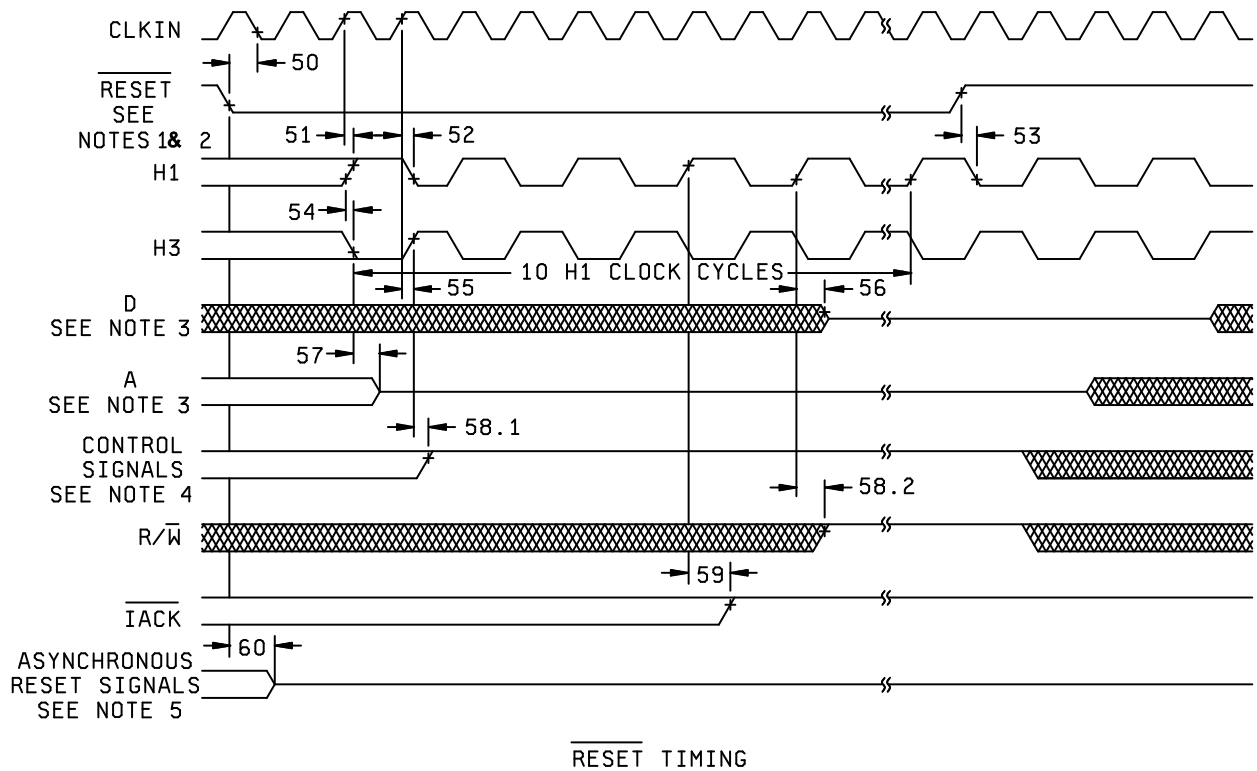
NOTE: $\bar{I}/OXFxBIT$ represents either bit 1 or bit 5 of the IOF register, and INXFxBIT represents either bit 3 or bit 7 of the IOF register.



NOTE: $\bar{I}/OXFxBIT$ represents either bit 1 or bit 5 of the IOF register.

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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NOTES:

1. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
2. The $\overline{\text{R/W}}$ output is placed in the high-impedance state during reset. It can be pulled high with a resistive pullup of 18-20 k Ω to prevent spurious writes.
3. In microprocessor mode ($\text{MCBL}/\overline{\text{MP}} = 0$), reset vector is fetched twice with seven software wait states each. In microcomputer mode ($\text{MCBL}/\overline{\text{MP}} = 1$), the reset vector is fetched two times, with no software wait states.
4. Control signals include $\overline{\text{STRBx}}$ and $\overline{\text{IOSTRB}}$.
5. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLKx.

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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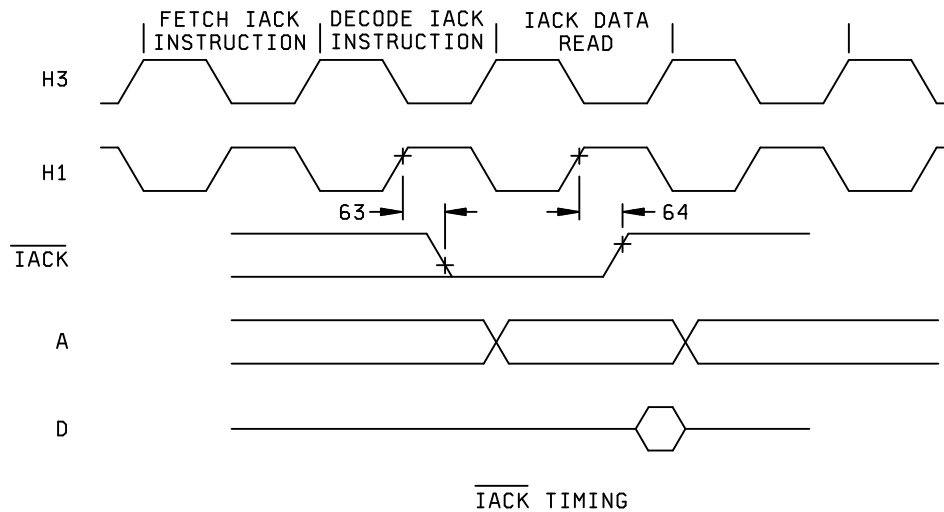
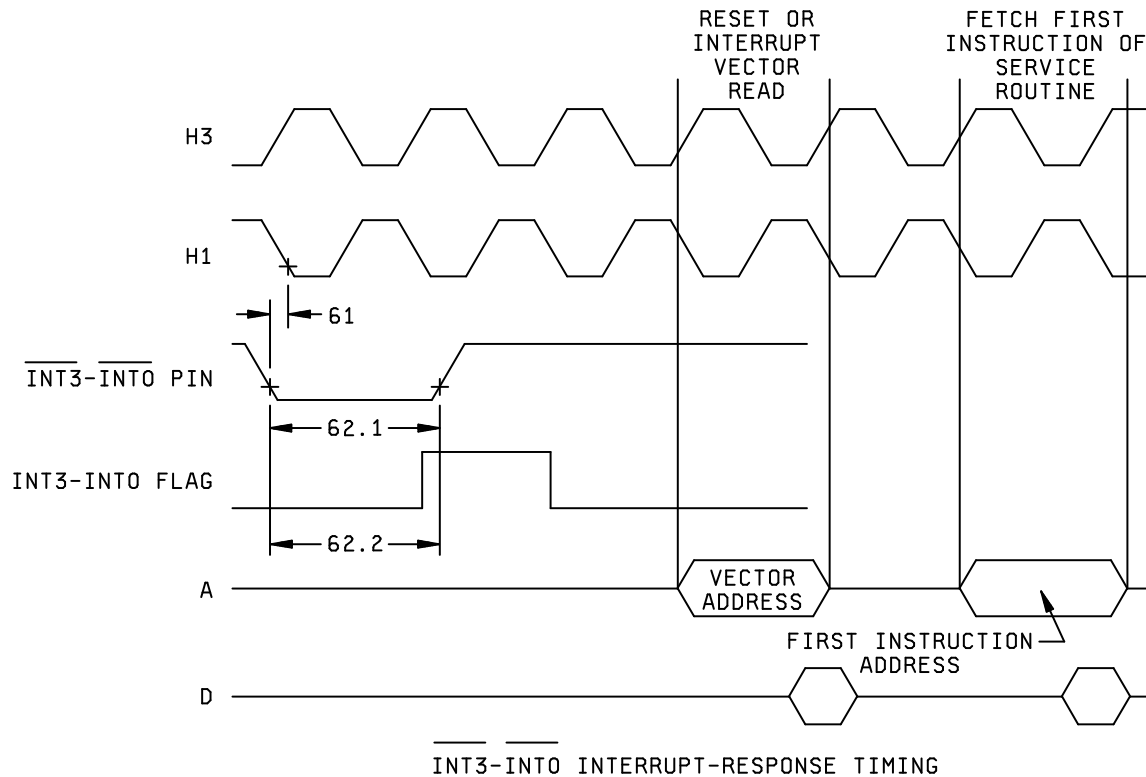
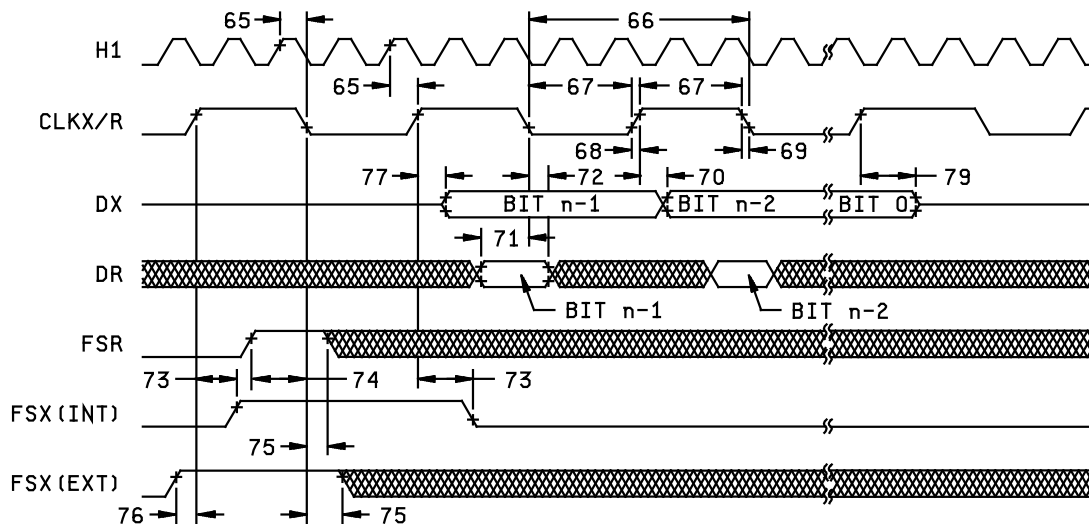


FIGURE 4. Load circuit and timing waveforms - Continued.

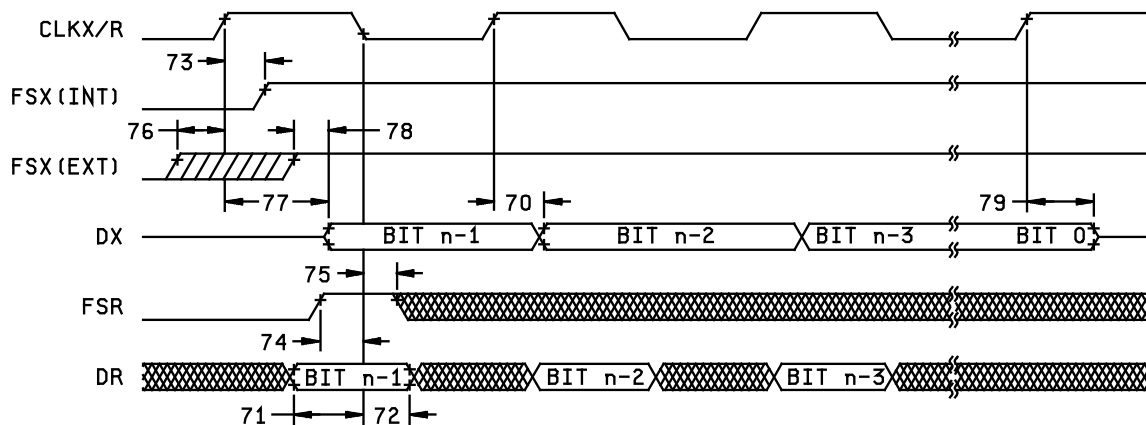
DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
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FIXED DATA-RATE-MODE TIMING

NOTES:

1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend upon the length of the serial-port word, where $n = 8, 16, 24,$ or 32 bits, respectively.



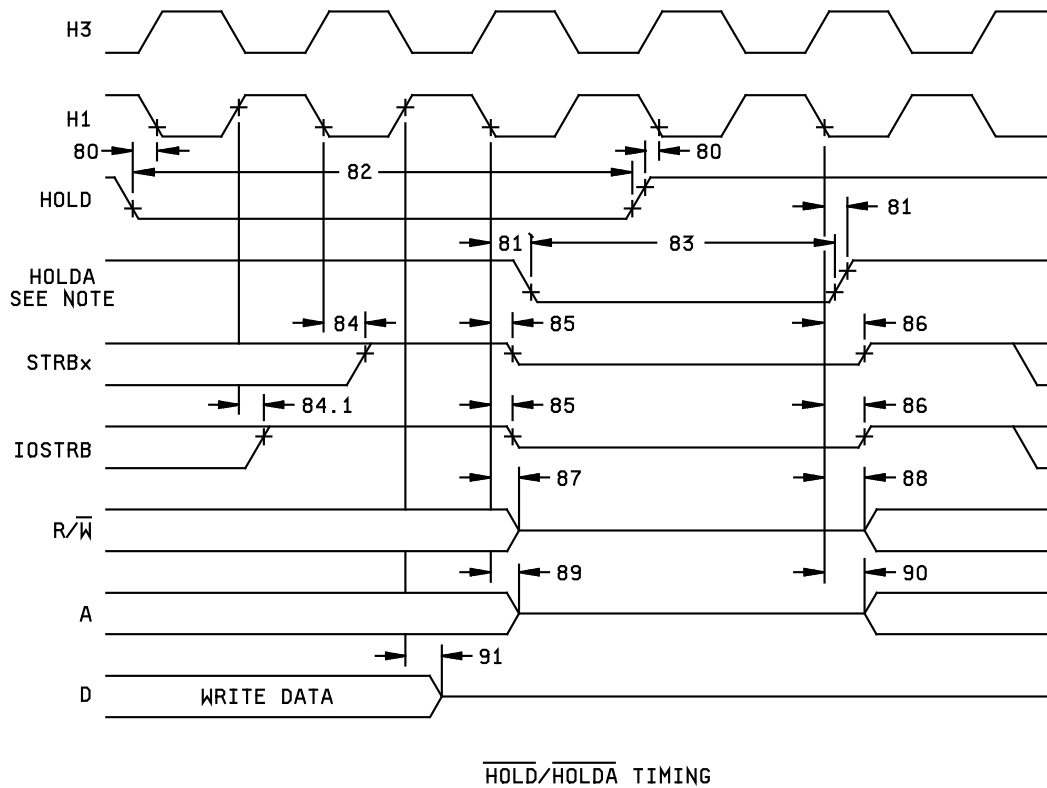
VARIABLE DATA-RATE-MODE TIMING

NOTES:

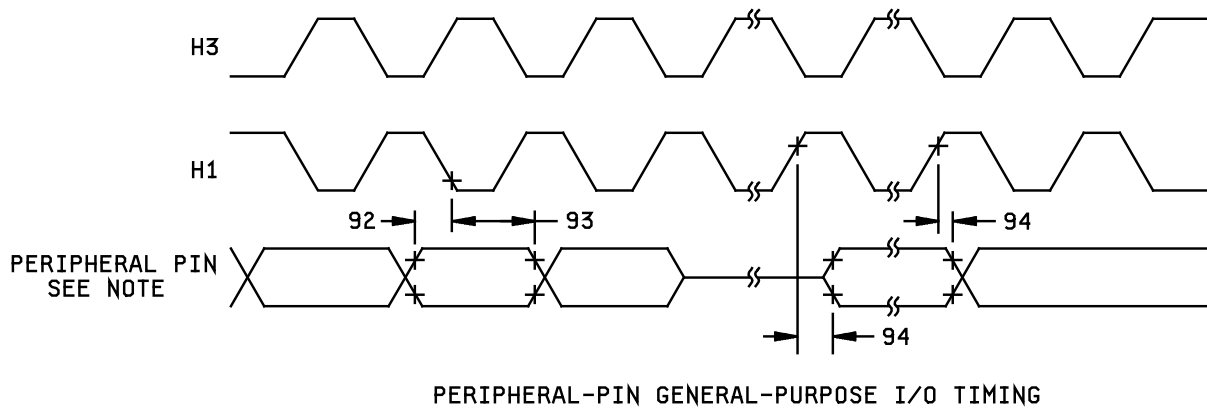
1. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
2. Timing diagrams depend upon the length of the serial-port word, where $n = 8, 16, 24,$ or 32 bits, respectively.
3. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

FIGURE 4. Load circuit and timing waveforms - Continued.

DLA WEAPONS SUPPORT COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03616
		REV D	PAGE 31



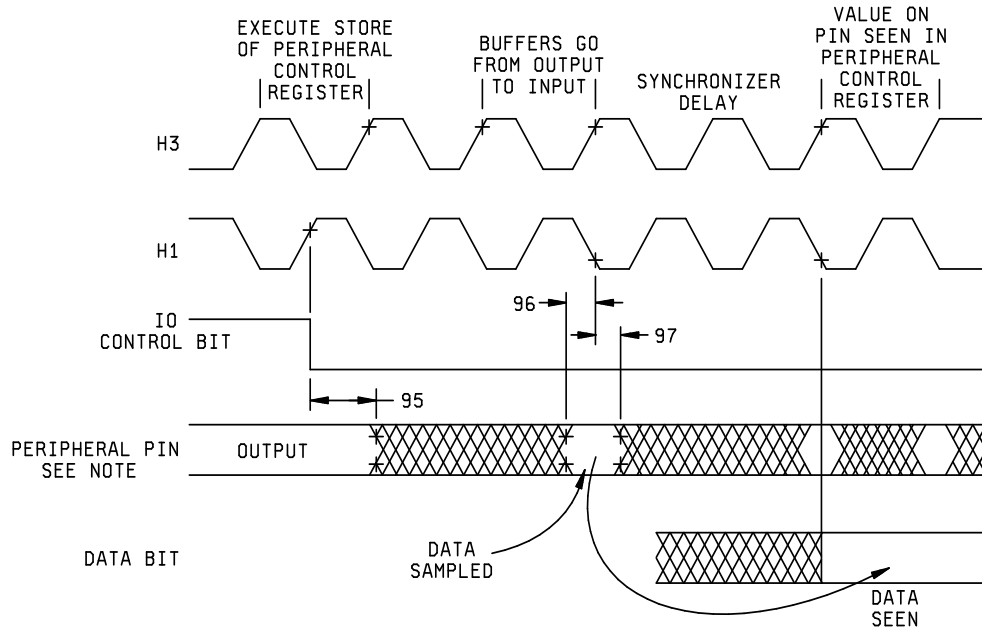
NOTE: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.



NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

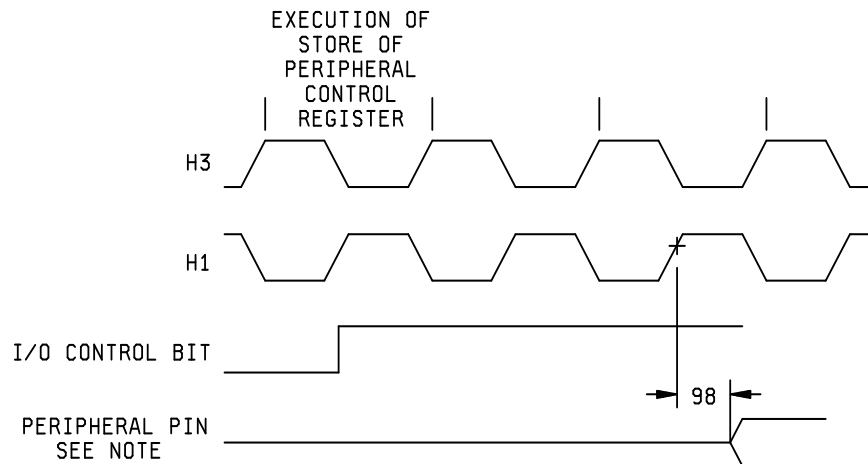
FIGURE 4. Load circuit and timing waveforms - Continued.

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CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE OUTPUT TO INPUT-MODE TIMING

NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

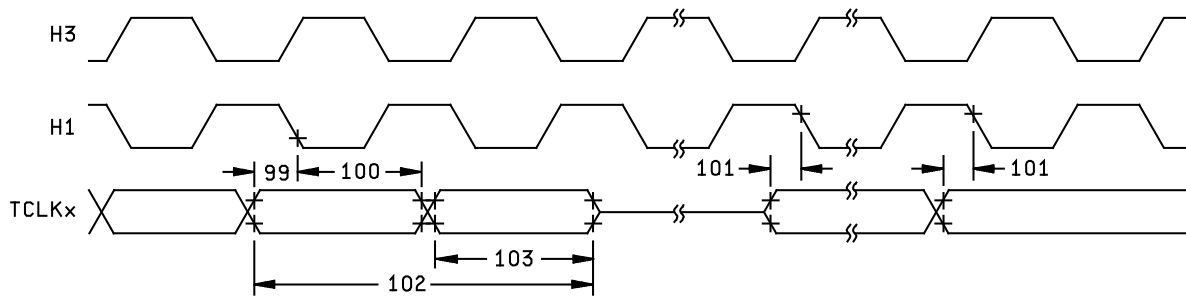


CHANGE OF PERIPHERAL PIN FROM GENERAL-PURPOSE INPUT TO OUTPUT-MODE TIMING

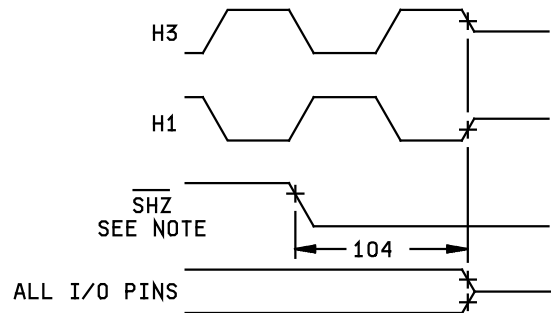
NOTE: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLKx. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

FIGURE 4. Load circuit and timing waveforms - Continued.

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TIMING FOR TIMER PIN



SHZ PIN TIMING

NOTE: Enabling $\overline{\text{SHZ}}$ destroys the device register and memory contents. Assert $\overline{\text{SHZ}} = 1$ and reset the device to restore it to a known condition.

FIGURE 4. Load circuit and timing waveforms - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Weapons Support (Columbus) maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top-Side Marking
V62/03616-01XE	01295	SM320C32PCMM50EP	SM320C32-50EP
V62/03616-02XE	01295	SM320C32PCMM60EP	SM320C32-60EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
12500 TI Blvd.
Dallas, TX 75243

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