REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R016-99. - drw	99-01-11	Raymond Monnin
B	Add requirements for QD certification. Incorporate revision A N.O.R. Editorial changes throughout. - drw	02-03-28	Raymond Monnin
C	Update drawing to meet current MIL-PRF-38535 requirements. - cgh	25-01-22	Laura Leeper Branham

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A

STANDARD MICROCIRCUIT DRAWING
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
93-11-22

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, 12-BIT, D/A CONVERTER, HIGH SPEED, MONOLITHIC SILICON

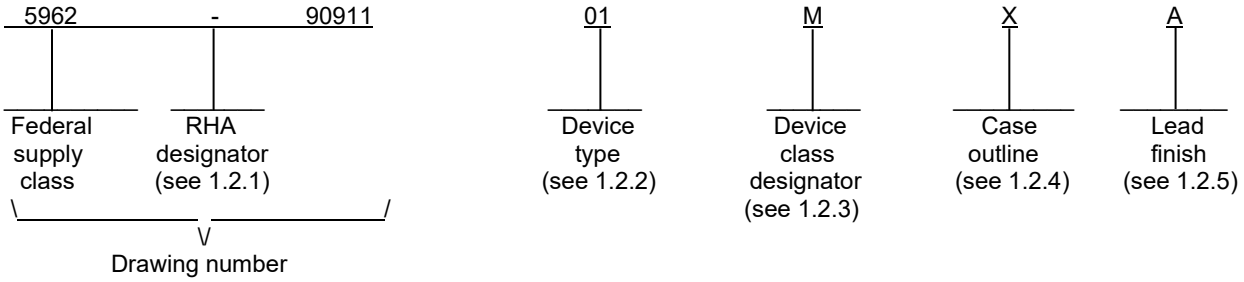
AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **67268**	**5962-90911**
		SHEET	1 OF 11	

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Differential nonlinearity
01	AD9712BS	12-bit, 100 MSPS, ECL-compatible D/A converter	±2.0 LSB
02	AD9712BT	12-bit, 100 MSPS, ECL-compatible D/A converter	±1.5 LSB
03	AD9713BS	12-bit, 80 MSPS, TTL-compatible D/A converter	±2.0 LSB
04	AD9713BT	12-bit, 80 MSPS, TTL-compatible D/A converter	±1.5 LSB

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Positive supply voltage ($+V_S$) ..... +6 V dc
Negative supply voltage ($-V_S$) ..... -7 V dc
Analog-to-digital ground voltage differential ..... 0.5 V dc
Digital input voltages (D_1 – D_{12}, LATCH ENABLE):
  Device types 01 and 02 ..... [0 to ($-V_S$)] V dc
  Device types 03 and 04 ..... [-0.5 to ($+V_S$)] V dc
Internal reference output current ..... 500 µA
Control amplifier input voltage range ..... 0 V dc to -4.0 V dc
Control amplifier output current ..... ±2.5 mA
Reference input voltage (V_{REF}) ..... [-3.7 to ($-V_S$)] V dc
Analog output current ..... 30 mA
Junction temperature (T_J) ..... +175°C
Storage temperature range (case) ..... -65°C to +150°C
Lead temperature (soldering 10 sec) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case outline X ..... 10°C/W
  Case outline 3 ..... 13°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case outline X ..... 32°C/W
  Case outline 3 ..... 41°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A) ..... -55°C to +125°C
Positive supply voltage range ..... V_S ±5%
Power dissipation (P_D):
  Devices types 01 of 02 ..... 728 mW (typical)
  Devices types 03 and 04 ..... 784 mW (typical)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, absolute maximum ratings are given at T_A = +25°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 56 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential nonlinearity	DNL		4	01, 03		±1.5	LSB
			5, 6			±2.0	
			4	02, 04		±1.0	
			5, 6			±1.5	
Integral nonlinearity	INL		4	01, 03		±1.75	LSB
			5, 6			±2.0	
			4	02, 04		±1.25	
			5, 6			±1.75	
Zero-scale offset error	I_Z		1	All		2.5	µA
			2, 3			5.0	
Full-scale offset error	A_{EFS}		1	All		5	%
			2, 3			8.0	
Internal reference voltage	V_{IR}		1	All	-1.11	-1.25	V
			2, 3		-1.09	-1.27	
Internal reference output current	I_{IR}	2/	1	All	-50	500	µA
Output compliance range	V_{OC}	2/	1	All	-1.2	2	V
Output resistance	R_O	2/	1	All	2.0	3.0	kΩ
Output update rate 3/		2/	9	01, 02	100		MSPS
				03, 04	80		
Digital logic “1” input voltage	V_{IH}		1, 2, 3	01, 02	-1.0		V
				03, 04	2.0		
Digital logic “0” input voltage	V_{IL}		1, 2, 3	01, 02		-1.5	V
				03, 04		0.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital logic "1" input current	I_{IH}		1, 2, 3	All		20	µA
Digital logic "0" input current	I_{IL}		1, 2, 3	01, 02		10	µA
				03, 04		600	
Input setup time 4/	t_S	2/	9	All	0.5		ns
Input hold time 5/	t_H	2/	9	All	1.8		ns
Latch pulse width (LOW) (transparent)	t_{LPW}	2/	9	All	2.5		ns
$+V_S$ supply current	$+I_S$		1	03, 04		12	mA
			2, 3			14	
$-V_S$ supply current	$-I_S$		1	01, 02		178	mA
			2, 3			183	
			1	03, 04		184	
			2, 3			188	
Power supply rejection ratio 6/	PSRR		4	All		125	µA/V

1/ $+V_S$ = +5 V; $-V_S$ = -5.2 V; reference voltage = -1.2 V; R_{SET} = 7.5 kΩ; V_{OUT} = 0 V (virtual ground), unless otherwise specified.

2/ Specification is guaranteed, but not tested.

3/ Data registered into DAC accurately at this rate; does not imply settling to 12-bit accuracy.

4/ Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.

5/ Data must remain stable for specified time prior to rising edge of LATCH ENABLE signal.

6/ Measured at ±5% of $+V_S$ (device types 03 and 04) and $-V_S$ (all device types) using external reference.

Device type	All
Case outline	X, 3
Terminal number	Terminal symbol
1	D_2
2	D_3
3	D_4
4	D_5
5	D_6
6	D_7
7	D_8
8	D_9
9	D_{10}
10	D_{11}
11	D_{12} (LSB)
12	DIGITAL $-V_S$
13	ANALOG RETURN
14	I_{OUT}
15	ANALOG $-V_S$
16	$\overline{I_{OUT}}$
17	REFERENCE IN
18	CONTROL AMP OUT
19	CONTROL AMP IN
20	REFERENCE OUT
21	DIGITAL $-V_S$
22	REFERENCE GROUND
23	DIGITAL $+V_S$
24	R_{SET}
25	ANALOG $-V_S$
26	LATCH ENABLE
27	DIGITAL GROUND
28	D_1 (MSB)

FIGURE 1. Terminal connections.

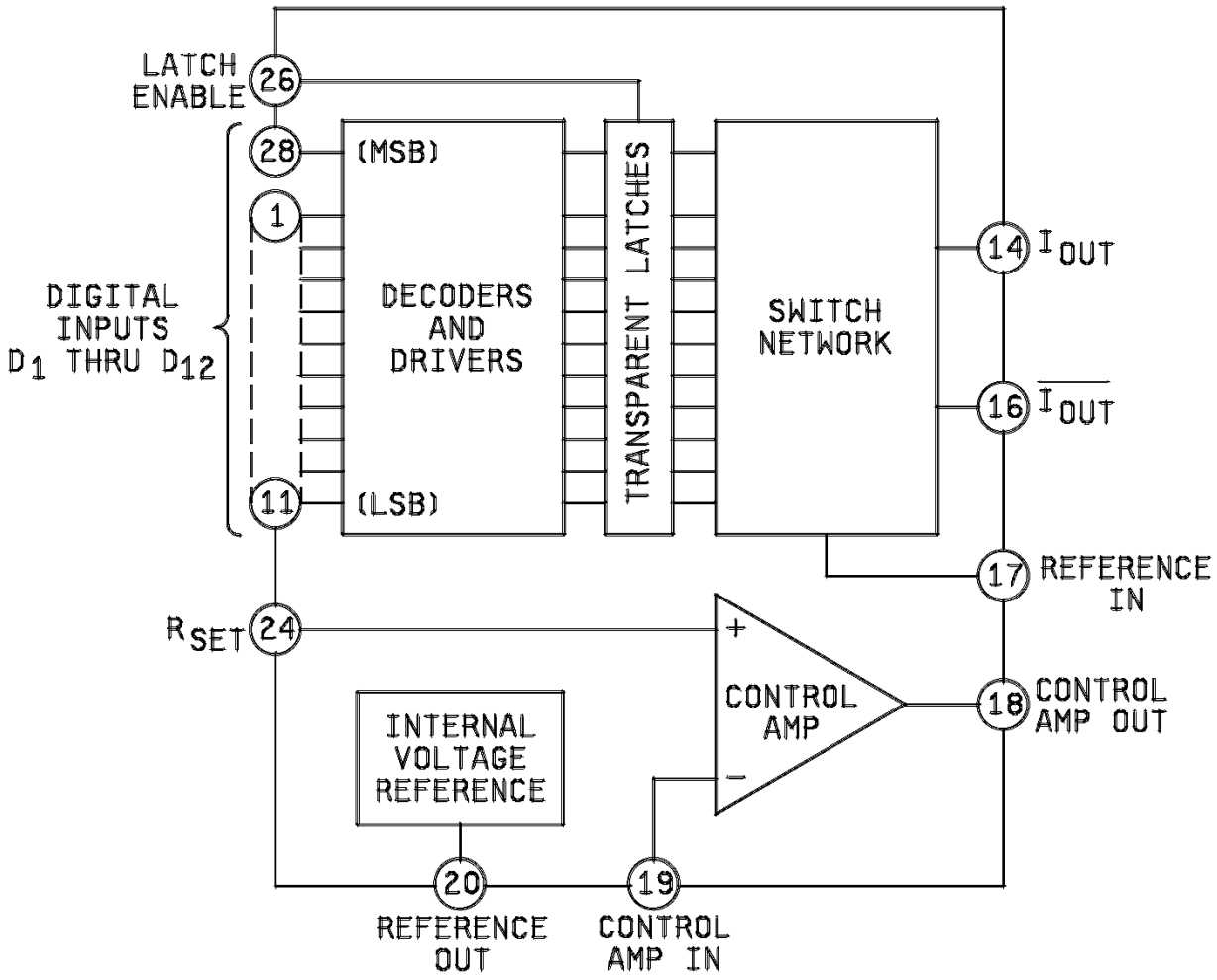


FIGURE 2. Functional block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3 1/	1, 2, 3 1/	1, 2, 3 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9	1, 2, 3, 4, 5, 6, 9	1, 2, 3, 4, 5, 6, 9
Group C end-point electrical parameters (see 4.4)	1	1	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-01-22

Approved sources of supply for SMD 5962-90911 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9091101M3A	3/	AD9712BSE/883B
5962-9091101MXA	3/	AD9712BSQ/883B
5962-9091102M3A	3/	AD9712BTE/883B
5962-9091102MXA	3/	AD9712BTQ/883B
5962-9091103M3A	3/	AD9713BSE/883B
5962-9091103MXA	3/	AD9713BSQ/883B
5962-9091104M3A	3/	AD9713BTE/883B
5962-9091104MXA	3/	AD9713BTQ/883B
	3/	AS9713BC28/883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr Suite 105 Austin, TX 78754 4566

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.