

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
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THE CAGE CODE 67268 ENTITY HAS BEEN CHANGED TO DLA WEAPONS SUPPORT (COLUMBUS).

Revision Status of Sheets

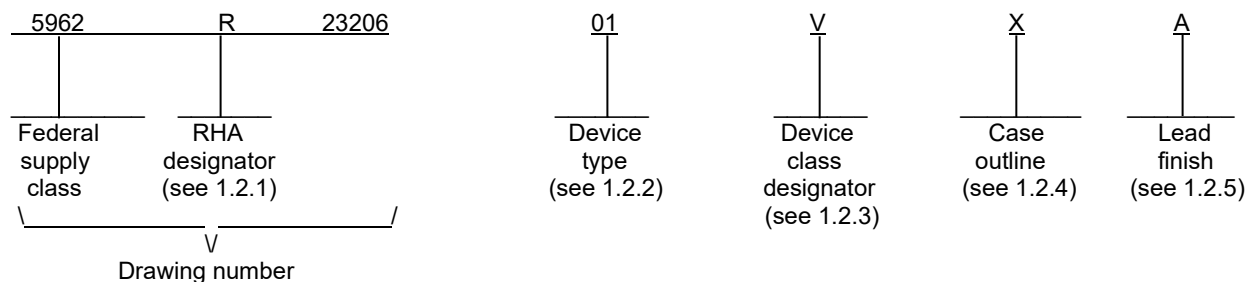
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PMIC N/A				
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY CHRISTOPHER HANCOCK	DLA WEAPONS SUPPORT COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY CHRISTOPHER HANCOCK			
	APPROVED BY JAMES R. ESCHMEYER	MICROCIRCUIT, LINEAR, BiCMOS, RADIATION HARDENED, SYNCHRONOUS BUCK CONTROLLER WITH INTEGRATED GATE DRIVERS, 4.75 V TO 13.2 V INPUT, 0.6 V TO 5.25 V OUTPUT, 100 kHz TO 2 MHz, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 26-08-07			
AMSC N/A	REVISION LEVEL	SIZE A	CAGE CODE 67268	5962-23206
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	RIC70847	Radiation hardened, Synchronous buck controller with integrated gate drivers

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	24	Flat pack package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Input voltage (V _{IN})	-0.3 V to 17.1 V
VDRV to PGND	-0.3 V to 6.5 V
BOOT to SW	-0.3 V to 6.5 V
SW to PGND	-1.3 V to 17.1 V
GH to SW	-0.3 V to [V _{DRV} + 0.3] V
GL to PGND	-0.3 V to [V _{DRV} + 0.3] V
EN (V _{EN})	-0.3 V to 17.1 V
SYNCl, ISNS-, ISNS+, PG (IN)	-0.3 V to 6.5 V
SLP, RT, SYNCO, OCP, LLR, COMP, VREF, SS, FB (LGC)	-0.3 V to 3.6 V
FB RET to AGND (GND _A)	-0.3 V to 0.3 V
PGND to AGND (GND _P)	-0.9 V to 0.9 V
Operating junction temperature range:	-55°C to +150°C
Storage temperature range	-65°C to +165°C
Lead temperature (soldering, 10 seconds):	
1.6 mm (0.063 inch) from case	+300°C
Thermal resistance, junction to case (θ _{JC})	1.7°C/W
Thermal resistance, junction to ambient (θ _{JA})	27°C/W
Electrostatic discharge (ESD):	
Human body model (HBM) (class 3A)	4 kV 2/
Charged device model (CDM)	1 kV 3/

1.4 Recommended operating conditions. 4/

VIN bias voltage (V _{IN})	4.75 V to 13.2 V 5/
External voltage on VDRV pin (V _{DRV})	4.6 V to 5.25 V
Output voltage (V _{OUT})	0.6 V to 5.25 V
Switching frequency (f _{SW}) (RT or SYNCl)	100 kHz to 2 MHz 6/
Operating temperature range (T _A)	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Per MIL-STD-883, TM 3015.
- 3/ Per ANSI/ESDA/JEDEC JS-002.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 5/ When voltage on VIN is less than 5.25 V, internal LDO is in dropout which may cause VDRV voltage to drop too low under some operating conditions. When operating with low voltage input it is recommended to short VDRV to VIN pin.
- 6/ At higher frequency, minimum on time requirements will limit duty cycle and minimum supported output voltage.

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1.5 Radiation features.

Maximum total ionizing dose (TID) available:

Dose rate = 50 - 300 rad(Si)/s (see 4.4.4.1) 100 krad(Si) 7/
 Low dose rate $\leq$ 10 mrad(Si)/s (see 4.4.4.1) 100 krad(Si) 7/

Heavy ion single event phenomenon (SEP) test:

No Single event latch-up (SEL) occurs at effective LET (see 4.4.4.2) $\leq 81.8 \text{ MeV-cm}^2/\text{mg}$ 8/
 No Single event burnout (SEB) occurs at effective LET (see 4.4.4.2) $\leq 81.8 \text{ MeV-cm}^2/\text{mg}$ 8/
 No Single event gate rupture (SEGR) occurs at effective LET (see 4.4.4.2) $\leq 81.8 \text{ MeV-cm}^2/\text{mg}$ 8/

Neutron/Displacement irradiation damaged test (1-MeV equivalent) (see 4.4.4.3) $1 \times 10^{13} \text{ neutrons/cm}^2$ 9/

- 7/ The manufacturer supplying device type 01 has performed total ionizing dose (TID) characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and parts exhibited no enhanced dose rate sensitivity (ELDRS) susceptibility to TID level 150 krad(Si). However, the radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D, and postirradiation electrical parametric limits fall within the specification limit for parts marked to RHA designated level R to a maximum total dose of 100 krad(Si). For more information on TID test and results, please contact device type 01 manufacturer CAGE 69210.
- 8/ Heavy-ion testing was performed at TAMU Cyclotron Radiation Effects Facility. Gold (Au), Xe, Ag, and Kr ion beams were used at a flux of $10^5 \text{ ions/cm}^2\text{-s}$, a fluence level of 10^7 ions/cm^2 , and a temperature of 125°C . Destructive testing (SEL, SEB, SEGR) was performed on 9 samples using Au, with no events observed; specifically, no single event latch-up (SEL) was observed at effective LET of $81.8 \text{ MeV-cm}^2/\text{mg}$, and no SEB/SEGR was observed at effective LET of $81.8 \text{ MeV-cm}^2/\text{mg}$. SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEE/SEP test and results, please contact device type 01 manufacturer CAGE 69210.
- 9/ Neutron/Displacement damaged (NDD) dosimetry test was performed in the Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to $1 \times 10^{13} \text{ neutrons/cm}^2$ (1-MeV equivalent). A sample size of twelve units were exposed to radiation testing per MIL-STD-883, method 1017 for Neutron Irradiation. For more information on NDD test and results, please contact device type 01 manufacturer CAGE 69210.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 – Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 – Test Method Standard Microcircuits.

MIL-STD-1835 – Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 – List of Standard Microcircuit Drawings.

MIL-HDBK-780 – Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) INTERNATIONAL

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org/>.)

JEDEC Solid State Technology Association

JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)

(Copies of these documents are available online at <https://www.jedec.org/>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Weapons Support (Columbus)-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
BIAS INPUT POWER.							
VIN operating current unloaded (500 kHz switching frequency)	I _{INQNL}	EN = 5 V, RT = 28.6 kΩ, GL and GH = no load <u>4/</u>	1, 2, 3	01	5	9	mA
VIN standby current	I _{INSD}	EN = 0 V <u>4/</u>	1, 2, 3	01	2	7	mA
Input overvoltage shutdown rising	V _{INOV+}	<u>4/</u>	1, 2, 3	01	15.5	17.1	V
Input overvoltage shutdown falling	V _{INOV-}	<u>4/</u>	1, 2, 3	01	15.2	17.1	V
Input OVP hysteresis	V _{INOVH}	<u>3/</u>	1, 2, 3	01	0.4 typical		mV
VIN UVLO rising threshold	V _{INUV+}	<u>4/</u>	1, 2, 3	01	4.2	4.6	V
VIN UVLO falling threshold	V _{INUV-}	<u>4/</u>	1, 2, 3	01	4.1	4.5	V
VIN UVLO hysteresis	V _{INUVH}	<u>3/</u>	1, 2, 3	01	100 typical		mV
LINEAR DROPOUT REGULATOR (LDO).							
VDRV voltage from LDO	V _{DRV}	VIN = 9 V <u>4/</u>	1, 2, 3	01	4.7	5.3	V
Dropout voltage (VIN - VDRV)	V _{DRVD}	VIN = 4.5 V <u>4/</u>	1, 2, 3	01	5	20	mV
Current limit from VDRV pin	I _{DRV}	EN = 0 V, VIN = 4.75 V <u>4/</u>	1, 2, 3	01	130	280	mA
		EN = 0V, VIN = 13.2 V <u>4/</u>	1, 2, 3	01	170	310	mA
VDRV UVLO rising threshold	V _{DRVUV+}	<u>4/</u>	1, 2, 3	01	3.25	3.85	V
VDRV UVLO falling threshold	V _{DRVUV-}	<u>4/</u>	1, 2, 3	01	3.0	3.65	V
VDRV UVLO hysteresis	V _{DRVUVH}	<u>3/</u>	1, 2, 3	01	130 typical		mV
DRIVER.							
GH high output drive	V _{OHGH}	I _{GH} = 20 mA, BOOT = 5 V <u>4/</u>	1, 2, 3	01	4.95	---	V
GL high output drive	V _{OHGL}	I _{GL} = 20 mA, VDRV = 5 V <u>4/</u>	1, 2, 3	01	4.95	---	V
GH low output drive	V _{OLGH}	I _{GH} = 20 mA, BOOT = 5 V <u>4/</u>	1, 2, 3	01	---	0.05	V
GL low output drive	V _{OLGL}	I _{GL} = 20 mA, VDRV = 5 V <u>4/</u>	1, 2, 3	01	---	0.05	V
GH turn on resistance	R _{GHH}	I _{GL} = 20 mA <u>4/</u>	4, 5, 6	01	0.9	1.9	Ω
GH turn off resistance	R _{GHL}	I _{GL} = 20 mA <u>4/</u>	4, 5, 6	01	0.6	1.5	Ω
GL turn on resistance	R _{GLH}	I _{GL} = 20 mA <u>4/</u>	4, 5, 6	01	0.7	1.6	Ω
GL turn off resistance	R _{GLL}	I _{GL} = 20 mA <u>4/</u>	4, 5, 6	01	0.7	1.6	Ω
See footnotes at end of table.							
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TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DRIVER – continued.							
GH turn on peak current	I _{GHH}	<u>3/</u>	1, 2, 3	01	2 typical		A
GH turn off peak current	I _{GH} L	<u>3/</u>	1, 2, 3	01	2 typical		A
GL turn on peak current	I _{GLH}	<u>3/</u>	1, 2, 3	01	2 typical		A
GL turn off peak current	I _{GL} L	<u>3/</u>	1, 2, 3	01	2 typical		A
Minimum on time GH	t _{minonGH}	<u>4/</u>	9, 10, 11	01	---	27	ns
Minimum on time GL	t _{minonGL}		9, 10, 11	01	---	30	ns
Dead time	t _{dt}	<u>3/</u>	9, 10, 11	01	---	15	ns
OSCILLATOR.							
Internal oscillator frequency	f _{RT}	RT = 28.6 kΩ <u>4/</u>	4, 5, 6	01	450	550	kHz
		RT = 13.7 kΩ <u>4/</u>			900	1100	
SYNCl input threshold (rising edge)	V _{SYNCl}	<u>4/</u>	1, 2, 3	01	0.8	1.0	V
SYNCl input minimum on and off pulse width	t _{SYNClON}	<u>3/</u>	9, 10, 11	01	---	100	ns
SYNCl input current	I _{SYNCl}	V _{SYNCl} = 0 V or 5 V <u>4/</u>	1, 2, 3	01	-70	60	μA
SYNCO voltage, logic high	V _{SYNCOH}	<u>4/</u>	1, 2, 3	01	2.7	3.1	V
SYNCO voltage, logic low	V _{SYNCOL}	<u>4/</u>	1, 2, 3	01	---	0.1	V
SYNCO phase delay (GH to SYNCO)	P _{SYNCO}	180° phase shift <u>3/</u>	4, 5, 6	01	[0.5 / f _{RT}] typical		° (degrees)
FEEDBACK AND ERROR AMPLIFIER.							
Reference voltage (V _{REF}) + EA offset voltage (V _{OSEA})	V _{FB}		1, 2, 3	01	594	606	mV
Reference voltage	V _{REF}	<u>4/</u>	1, 2, 3	01	594	606	mV
FB input leakage current	I _{FB}	V _{FB} = 600 mV, LLR = open	1, 2, 3	01	-1	1	μA
FB pin overvoltage protection	V _{FBOVP}	<u>4/</u>	1, 2, 3	01	0.64	0.69	V
FB pin undervoltage protection	V _{FBUVP}	<u>4/</u>	1, 2, 3	01	0.51	0.57	V

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
FEEDBACK AND ERROR AMPLIFIER – continued.							
Feedback pin undervoltage propagation delay	t _{VFBUP}	<u>4/</u>	9, 10, 11	01	0.3	0.7	μs
EA DC gain	A _{EA}	<u>3/</u>	4, 5, 6	01	126 typical		dB
EA transconductance	g _{mEA}	<u>4/</u>	9, 10, 11	01	0.6	1.6	mS
EA offset voltage	V _{OSEA}	<u>4/</u>	1, 2, 3	01	-6	6	mV
EA gain bandwidth product	G _{BWEA}	<u>3/</u>	4, 5, 6	01	155 typical		MHz
SOFT START.							
Soft start current source	I _{SS}	<u>4/</u>	1, 2, 3	01	7.5	12.5	μA
CURRENT SENSE.							
Current sense amplifier DC gain	A _{ISNS}	(ISNS+) – (ISNS-) = ±5 mV <u>4/</u>	4, 5, 6	01	9.5	10.5	V/V
Current sense amplifier transconductance	g _{mISNS}	Measured on OCP pin <u>4/</u>	1, 2, 3	01	280	380	μS
Current sense amplifier gain bandwidth product	G _{BWISNS}	<u>3/</u>	4, 5, 6	01	30 typical		MHz
Leakage current, ISNS+ and ISNS-	I _{ISNS}	(ISNS+) = 0.6 V, (ISNS-) = 0.6 V <u>4/</u>	1, 2, 3	01	---	20	μA
		(ISNS+) = 3.6 V, (ISNS-) = 3.6 V <u>4/</u>					
Overcurrent threshold	V _{OCP}	<u>4/</u>	1, 2, 3	01	1.195	1.235	V
Negative overcurrent threshold	V _{NOCP}	Preirradiation <u>4/</u>	1, 2, 3	01	-40	-13	mV
		Postirradiation	1, 2, 3	01	-40	-10	mV
Overcurrent threshold propagation delay	t _{OCP}	(ISNS+) to (ISNS-) = 20 mV <u>4/</u>	9, 10, 11	01	0.2	0.5	μs
LOAD LINE REGULATION.							
Load line regulation current source from feedback pin, no load	I _{LLRIN}	R _{LLR} = 7.15 kΩ, (ISNS+) – (ISNS-) = 0 mV	1, 2, 3	01	-0.01	0.01	μA
Load line regulation current source from feedback pin, full load	I _{LLRL}	R _{LLR} = 7.15 kΩ, (ISNS+) to (ISNS-) = 20 mV <u>4/</u>	1, 2, 3	01	-1.7	-0.5	μA
Load line regulation current source maximum	I _{LLRM}	<u>3/</u>	1, 2, 3	01	10 typical		μA
LLR bandwidth	BW _{LLR}	<u>3/</u>	4, 5, 6	01	250 typical		kHz
See footnotes at end of table.							
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TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions $\frac{1}{2}$ / -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ENABLE.							
EN rising threshold	V _{EN+}	<u>4</u> /	1, 2, 3	01	0.86	0.98	V
EN falling threshold	V _{EN-}	<u>4</u> /	1, 2, 3	01	0.69	0.85	V
EN pin hysteresis	V _{ENHYS}	<u>3</u> /	1, 2, 3	01	200 typical		mV
EN pin leakage current	I _{EN}	EN = 0 V and 5 V <u>4</u> /	1, 2, 3	01	-100	100	nA
POWER GOOD.							
V _{FB} high limit for PG	V _{PGOV}	<u>4</u> /	1, 2, 3	01	630	700	mV
V _{FB} high limit hysteresis	V _{PGOVH}	<u>3</u> /	1, 2, 3	01	21 typical		mV
V _{FB} low limit for PG	V _{PGUV}	<u>4</u> /	1, 2, 3	01	510	570	mV
V _{FB} low limit hysteresis	V _{PGUVH}	<u>3</u> /	1, 2, 3	01	31 typical		mV
PG low output	V _{PGL}	I _{PGOUT} = 2 mA <u>4</u> /	1, 2, 3	01	0.1	0.4	V
PG active source current limit	I _{PG}	<u>3</u> /	1, 2, 3	01	---	4	mA
PG high leakage current	I _{PGLK}		1, 2, 3	01	---	100	nA
OVER TEMPERATURE.							
Overtemperature shutdown	T _{SD}	<u>3</u> /	---	01	155	---	°C
Overtemperature hysteresis	T _{HYS}	<u>3</u> /	---	01	25 typical		°C

- 1/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are characterized up to “R” level. Preirradiation and postirradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 2/ Unless otherwise specified, V_{IN} = 4.75 V to 13.2 V, and T_A = T_J. Logic pins (EN, SLP, RT, SYNCO, SYNCI, ISNS-, ISNS+, OCP, LLR, PG, COMP, VREF, SS, FB) are with respect to AGND = FB RET, power pins (VIN, VDRV, GL) are with respect to PGND and bootstrap pins (BOOT, GH) are with respect to SW.
- 3/ Not subject to production test and guaranteed by design and characterization.
- 4/ Burn-in deltas are performed on this electrical characteristic. Refer to table IIA and table IIB for additional information.

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TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T _C)	V _{IN}	Effective linear energy transfer (LET)
01	No SEL	125°C	16.7 V	≤ 81.8 MeV-cm ² /mg
	No SEB	25°C	16.7 V	≤ 81.8 MeV-cm ² /mg
	No SEGR	25°C	16.7 V	≤ 81.8 MeV-cm ² /mg

1/ For single event phenomena (SEP) test conditions, see 4.6 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ Heavy-ion testing was performed at TAMU Cyclotron Radiation Effects Facility. Gold (Au), Xe, Ag, and Kr ion beams were used at a flux of 10⁵ ions/cm²-s, a fluence level of 10⁷ ions/cm², and a temperature of 125°C. Destructive testing (SEL, SEB, SEGR) was performed on 9 samples using Au, with no events observed; specifically, no single event latch-up (SEL) was observed at effective LET of 81.8 MeV-cm²/mg, and no SEB/SEGR was observed at effective LET of 81.8 MeV-cm²/mg. SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEE/SEP test and results, please contact device type 01 manufacturer CAGE 69210.

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Case outline X

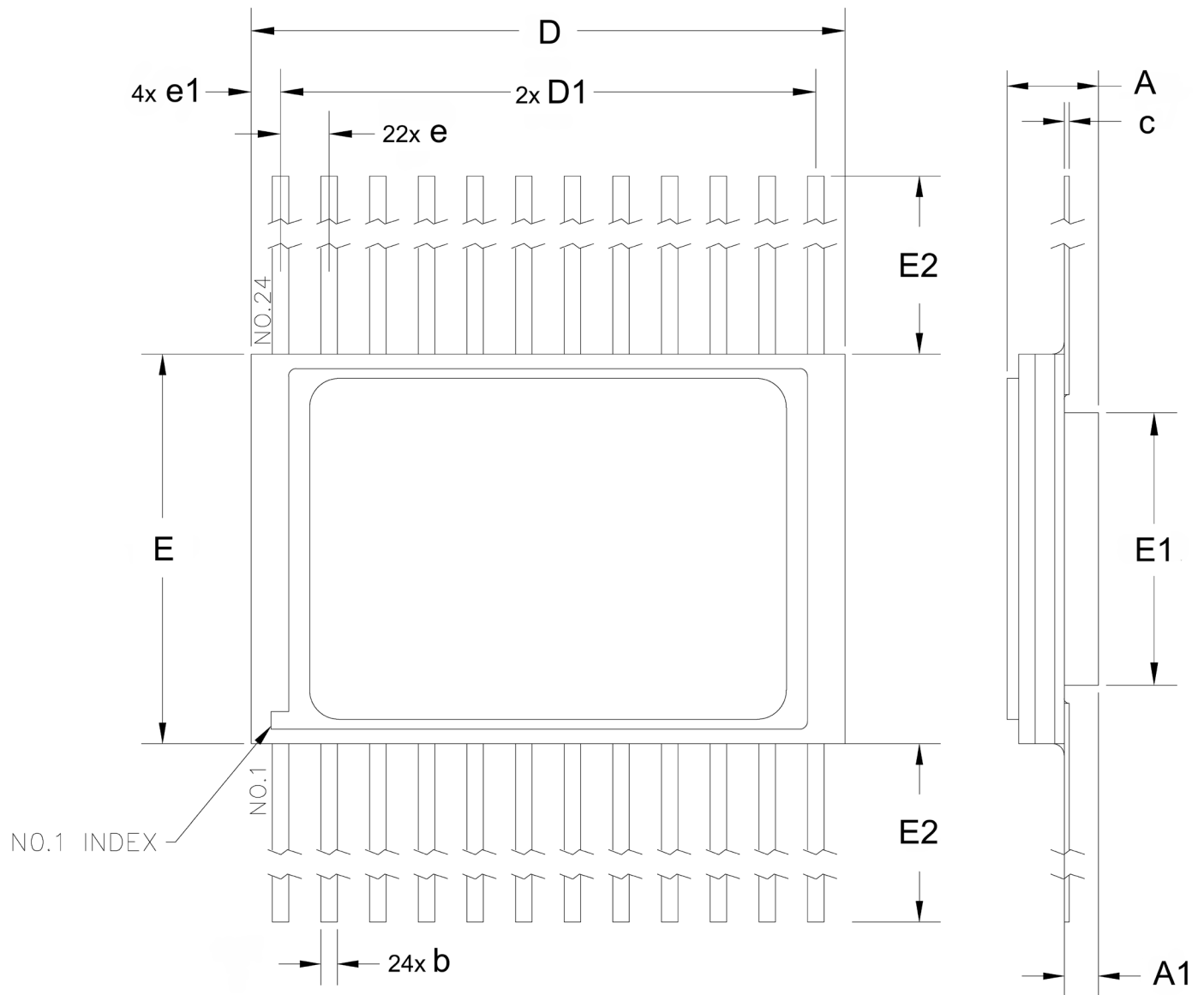


FIGURE 1. Case outline.

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Case outline X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	0.118	---	3.0
A1 REF	0.035 REF		0.89 REF	
b	0.014	0.020	0.36	0.51
c	0.004	0.006	0.1	0.15
D	0.602	0.618	15.29	15.7
D1	0.545	0.555	13.84	14.1
E	0.392	0.408	9.96	10.36
E1	0.274	0.286	6.96	7.26
E2	0.250	0.370	6.35	9.4
e	0.047	0.053	1.19	1.35
e1 REF	0.030 REF		0.76 REF	
N	24			

NOTES:

1. Controlling dimensions are inches; millimeter dimensions are given for reference only.
2. Dimensioning and tolerancing per ASME Y14.5M.
3. Lead thickness dimension does not include solder thickness.
4. Symbol N is the maximum number of leads.

FIGURE 1. Case outline - continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	SYNCl	Input for external clock. Clock on this pin will determine switching frequency if higher than frequency set on RT.
2	RT	Switching frequency selection. Connect a resistor from this pin to FB RET to set the switching frequency when in standalone operation.
3	SYNCO	Output of external clock for synchronization.
4	ISNS+	Positive input pin for inductor current sensing
5	ISNS-	Negative input pin for inductor current sensing
6	AGND	Analog ground. Logic signals are referenced to this pin. This terminal is connected to the lid.
7	FB RET	Feedback return ground. Feedback signals are referenced to this pin.
8	VREF	Output of internal 600 mV reference voltage. A ceramic capacitor is recommended between this pin and FB RET.
9	FB	Feedback pin for output voltage sensing
10	COMP	Output of internal transconductance error amplifier. Connect compensation network from this pin to AGND.
11	SLP	Slope compensation pin. Connect a resistor from this pin to FB RET to set slope compensation ramp.
12	SS	Soft start pin. A capacitor connected from this pin to FB RET sets the soft start ramp time.

FIGURE 2. Terminal connections.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
13	LLR	Load line regulation. To enable load line regulation, connect a resistor from this pin to AGND. For no load line regulation, leave the pin unconnected.
14	OCP	Over current protection. Connect a resistor from this pin to FB RET to set overcurrent, short circuit and negative current protection threshold. This pin can additionally be used as an output for the sensed inductor current (ISNS+ to ISNS-).
15	VIN	Input for internal LDO. A ceramic capacitor is recommended between this pin and PGND.
16	GH	High side field effect transistor (FET) gate driver output.
17	SW	Switch node. Connect the high side FET source, low side FET drain and output inductor to this pin.
18	BOOT	Bootstrap supply for the high side FET gate driver. A ceramic capacitor is required between this pin and SW.
19	GL	Low side FET gate driver output
20, 22	PGND	Power ground. Connect to the source of the low side FET and negative terminal of input and output capacitors.
21	VDRV	Output of 5 V internal LDO. A ceramic capacitor is required between VDRV and PGND
23	PG	Open drain power good signal. pulled low when fault triggers, EN is pulled low or output voltage is outside regulation window
24	EN	Enable. Forcing low disables PWM on GH and GL and holds both driver outputs low.

FIGURE 2. Terminal connections – continued.

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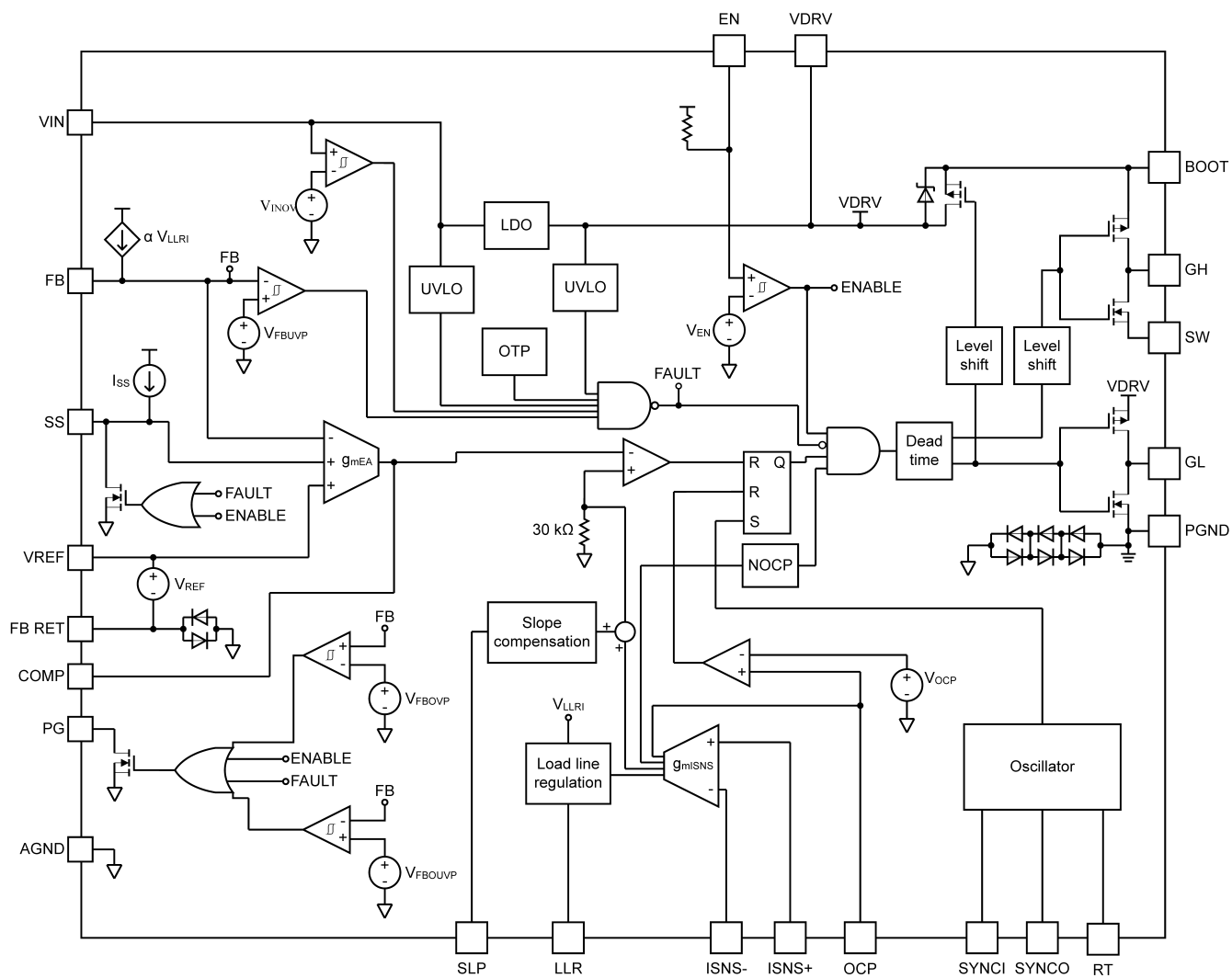


FIGURE 3. Block diagram.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4, 9 <u>1/</u>	1, 4, 9 <u>1/</u> <u>2/</u>
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>	1Δ, 2, 3, 4Δ, 5, 6, 9Δ, 10, 11 <u>1/</u> <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 4, 9	1Δ, 4Δ, 9Δ <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9

1/ PDA applies to subgroup 1.

2/ Δ indicates delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous electrical parameters.

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TABLE IIB. Burn-in and operating life test delta parameters ($T_A = +25^\circ\text{C}$). 1/ 2/ 3/

Parameters	Symbol	Min	Max	Units
VIN standby current	I_{NSD}	-0.7	0.7	mA
Dropout voltage ($V_{\text{IN}} - V_{\text{DRV}}$)	V_{DRVD}	-5	5	mV
Minimum on time GH	t_{minonGH}	-5	5	ns
SYNCO voltage, logic low	$V_{\text{SYNCO L}}$	-10	10	mV
EA offset voltage	V_{OSEA}	-0.7	0.7	mV
Leakage current, ISNS+ and ISNS- ($I_{\text{SNS+}}$, $I_{\text{SNS-}} = 0.6 \text{ V}$)	I_{SNS}	-0.25	0.25	μA
Negative overcurrent threshold (Preirradiation)	V_{NOCP}	-8	8	mV
Overcurrent threshold propagation delay	t_{OCP}	-0.08	0.08	μs
Load line regulation current source from feedback pin, full load	I_{LLRL}	-1	1	μA
Additional burn-in delta parameters <u>4/</u>	---	-10	10	%

1/ 240 hour burn-in and group C end point electrical parameters. Deltas are performed at $T_A = +25^\circ\text{C}$.

2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in electrical limit.

3/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall correspond to the test defined in table IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

4/ This delta limit shall apply to each characteristic that is specified in table IA to have delta testing performed and which is also not individually listed in table IIB under the 'Parameters' column.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and D, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring an RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the preirradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the SEP characteristics. ASTM standard F1192 or JESD57 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 ions/cm²-s and 10^5 ions/cm²-s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ for single event burnout (SEB) testing and SEGR testing, and at the maximum rated operating temperature $\pm 10^{\circ}\text{C}$ for single event latch-up.
- f. Bias conditions shall be defined by the manufacturer for latch-up measurements.
- g. A minimum of four devices shall be tested for each SEP test mode. Destructive tests (SEL, SEB, SEGR) shall require zero failures.

4.4.4.3 Neutron/Displacement damaged dosimetry testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ after an exposure of 1×10^{12} neutrons/cm² (1-MeV equivalent minimum).

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Weapons Support (Columbus) when a system application requires configuration control and which SMD's are applicable to that system. DLA Weapons Support (Columbus) will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Weapons Support (Columbus)-VA via email: VACChief@dla.mil

6.4 Comments. Comments on this drawing should be directed to DLA Weapons Support (Columbus)-VA, 3990 E. Broad Street, Columbus, Ohio 43218-3990, or via email: VASChief@dla.mil

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Weapons Support (Columbus)-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions of SEP.
- b. Occurrence of latch-up (SEL).
- c. Occurrence of burnout (SEB).
- d. Occurrence of transient (SET).
- e. Occurrence of gate rupture (SEGR).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 26-08-07

Approved sources of supply for SMD 5962-23206 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Weapons Support (Columbus)-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Weapons Support (Columbus) maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R2320601VXA	69210	RIC70847F

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

69210

Vendor name
and address

IR HiRel Products, Inc
205 Crawford St,
Leominster, MA 01453

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.