

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
			

Revision Status of Sheets

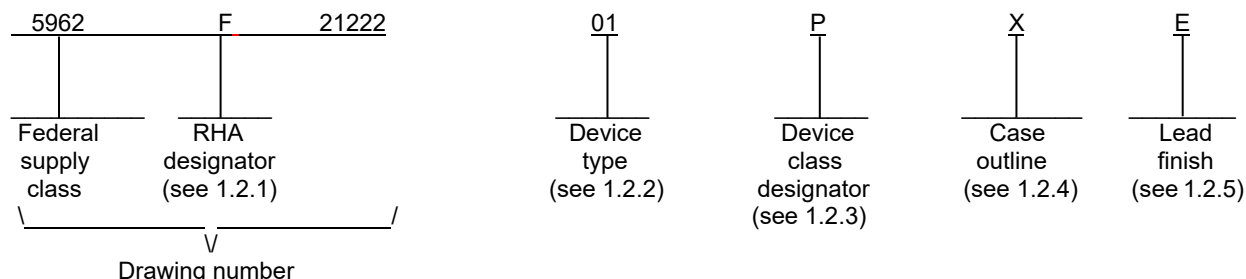
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SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A				
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY Ron E. Pompey	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY Christopher Hancock			
	APPROVED BY Laura Leeper Branham	MICROCIRCUIT, MEMORY, DIGITAL, CMOS RADIATION HARDENED, 512Mb NOR FLASH NON-VOLATILE MEMORY, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 25-03-06			
AMSC N/A	REVISION LEVEL	SIZE A	CAGE CODE 67268	5962-21222
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q), space application (device class V or Y), and plastic encapsulated microcircuits (PEM) (device class N) for military, terrestrial and avionics application and device class P for space application. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device classes N and P, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, P, Q, Y, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit Function
01	CYRS17B512-133AZMB	Plastic QSPI with ECC, 2.97-3.63 Volt, Radiation Hardened NOR Flash
02	CYRS17B512-133UZMB	Ceramic QSPI with ECC, 2.97-3.63 Volt, Radiation Hardened NOR Flash

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N or P	Certification and qualification to MIL-PRF-38535 for PEM performance environments.
Y	Certification and qualification to MIL-PRF-38535. Non hermetic flip chip technology on a ceramic or organic substrate.
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Plastic Thin Quad Flat Pack
Y	See figure 2	68	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, P, Q, Y, and V.

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/ 2/

V _{DD} MAX, V _{DDIO} MAX	-0.5 V to +4.1 V
Input voltage with respect to ground (V _{SS})	-0.5 V to V _{DD} + 0.5 V <u>2/</u>
Electrostatic discharge:	
HBM.....	> 2000 V <u>3/</u>
CDM.....	> 500 V <u>4/</u>
Output short circuit current	100 mA <u>5/</u>
Storage temperature plastic packages.....	-65°C to +150°C
Ambient temperature with power applied.....	-65°C to +125°C
Thermal resistance (junction to case) (Theta JC) Device Type 01.....	2.739°C/W
Thermal resistance (junction to case) (Theta JC) Device Type 02.....	12.66°C/W
Maximum Junction Temperature (T _j) Device Type 01.....	126°C
Maximum Junction Temperature (T _j) Device Type 02.....	130°C
Endurance / Data retention:	
Program / Erase Cycles:	
10K at ≤ 85°C	10 years <u>6/</u>
1K (50% duty cycle) at ≤ 125°C.....	10 years <u>6/</u>
Read cycle endurance.....	1 x 10 ¹² cycles <u>7/</u>

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V _{DD})	2.97 V dc to 3.63 V dc
Supply voltage range (V _{DDIO})	1.63 V dc to 3.63 V dc
Supply voltage reference (GND)	0.0 V dc
High level input voltage range (V _{IH})	0.7 x V _{DDIO} V to V _{DDIO} + 0.3 V
Low level input voltage range (V _{IL})	-0.3 V dc to 0.3 x V _{DDIO} V dc
Case operating temperature range (T _C)	-55°C to +125°C
Glass Transition Temperature Mold Compound (T _g)	125°C nominal <u>8/</u>

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum or minimum levels may degrade performance and affect reliability.
- 2/ All voltages are referenced to GND and maximum applied voltage shall not exceed +4.1 V.
- 3/ Human body model (HBM) tested per ANSI/ESDA/JEDEC JS-001 or method 3015 of MIL-STD-883.
- 4/ Charged device model (CDM) tested per ANSI/ESDA/JEDEC JS-002.
- 5/ No more than one output may be shorted to ground at a time. The duration of the short circuit should not be greater than one second.
- 6/ Endurance assumes a 50% write 1's and 50% write 0's.
- 7/ Read cycle endurance 1 x 10¹² cycles are tested under 10 program erase cycles, operating range voltage and temperature.
- 8/ Glass transition temperature (T_g) of Mold compound measured spec T_g value is 125°C.

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1.5 Radiation features.

Maximum total ionizing dose available (effective dose rate = 2.78 rads(Si)/s)..... 300 krad(Si) 7/

Heavy ion Single event phenomenon (SEP):

No SEL occurs at effective LET (see 4.4.4.4) at 125°C $\leq 80 \text{ MeV-cm}^2/\text{mg}$ 8/

No SEU occurs at on-set LET (see 4.4.4.4)..... $\leq 65 \text{ MeV-cm}^2/\text{mg}$ 8/

Single event functional interrupt (SEFI) error rate at in-situ LET 2.5 MeV-cm²/mg = 2.77×10^{-5} error /dev-day 8/

No dose rate induced upset – static $\leq 7 \times 10^{10} \text{ rad(Si)/sec}$ 9/

No Dose rate induced functional upset – R/W $\leq 1.1 \times 10^8 \text{ rad(Si)/sec}$ 9/

Dose rate survivability (RS)..... $\leq 5.72 \times 10^{10} \text{ rad(Si)/sec}$ 9/

No displacement damage was observed during neutron irradiation (1 MeV equivalent)... $5 \times 10^{14} \text{ neutrons/cm}^2$ 10/

7/ Manufacturer supplying device has been tested total ionizing dose (TID) test in accordance with method 1019 of MIL-STD-883, condition A to a maximum TID level of 350 krad(Si). However, devices marked to standard 300 krad(Si) of RHA TID level F. Manufacturer also perform room temperature anneal and 168 hours 100°C accelerated anneal test and effective dose rate after extended room temperature anneal = 2.78 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment. For details of the TID test report, please contact the manufacturer.

8/ Heavy ion single event effects (SEE) test was performed at the Texas A & M K500 Cyclotron facility. For single event latch-up (SEL) Xe ion beam was used and observed no rail to trail latch up occurred at an effective LET = 80 MeV-cm²/mg. However, high current events were observed at LET value 60.5 at 85°C and above. For single event functional interrupt (SEFI) error rate = 2.77×10^{-5} errors/dev-day to consider SEU error rate per CREME96 Geosynchronous orbit. For details of the SEE test report contact the device manufacturer.

9/ Flash X-Ray (FXR) radiation testing was performed at the AFRL Febetron 705 facility in Albuquerque, NM. No dose rate induced Latch up were observed at the dose rate = $7 \times 10^{10} \text{ rad(Si)/sec}$. Dose rate survivability test also performed at the AFRL Febetron 705 facility and no latch up occurs at high dose rate $5.72 \times 10^{10} \text{ rad(Si)/sec}$. For more information on FXR test contact the device manufacturer.

10/ Neutron/Displacement damaged dosimetry (NDD) test was performed in Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to $5 \times 10^{14} \text{ n/cm}^2$ (1-MeV equivalent). For more information on NDD tests contact the device manufacturer.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are the issues of the documents cited in the solicitation.

ANSI/ESDA/JEDEC JOINT STANDARD

ANSI/ESDA/JEDEC JS-001 - For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) – Component Level.

ANSI/ESDA/JEDEC JS-002 - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

(Copies of these documents are available online at <https://www.esda.org/>.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org/>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, P, Q, Y, and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block or logic diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The read and write cycle timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Functional tests. Various functional tests used to test this device are contained in appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes N, P, Q, Y, and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Organic or polymeric materials in device type 01. For device type 01, plastic packages inherently use organic or polymeric materials (adhesives, mold compounds, underfill, organic substrates, etc.).

3.2.8 Internal lead wire and die bond pad materials in device type 01. For device type 01, plastic packages internal lead wire metals are dissimilar from the die bond pad metallization metals. Internal lead wire metal is Gold (Au) and the die bond pad metallization metal is Aluminum (Al).

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, P, Q, Y, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, P, Q, Y, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, P, Q, Y, and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, P, Q, Y, and V in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V _{IL}		1, 2, 3	All	-0.3	0.3 x V _{DDIO}	V
Input high voltage	V _{IH}		1, 2, 3	All	0.7 x V _{DDIO}	V _{DDIO} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 0.1 mA, V _{DD} = V _{DD} min	1, 2, 3	All		0.4	V
Output high voltage	V _{OH}	I _{OH} = -0.1 mA	1, 2, 3	All	V _{DDIO} - 0.5		V
Input leakage current (except RESET#)	I _{LI}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH}	1, 2, 3	All	-10	+10	μA
Input leakage current (RESET# only)	I _{LI}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH}	1, 2, 3	All	-900	+200	μA
Output leakage current	I _{LO}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{SS} , CS# = V _{IH}	1, 2, 3	All	-10	+10	μA
Active QIO/QPI Read Current (READ) <u>1/</u>	I _{CC1}	QIO/QPI @ 133 MHz No output load	1, 2, 3	All		120	mA
Active Page Program Current	I _{CC2}	CS# = V _{DD}	1, 2, 3	All		120	mA
Active Non-Volatile Register Write Current (WRAR, WRR)	I _{CC3}	CS# = V _{DD}	1, 2, 3	All		120	mA
Active Sector/Block/Chip Erase Current	I _{CC4}	CS# = V _{DD}	1, 2, 3	All		120	mA
Active Page / Chip Scrub Current	I _{CC5}	CR1[7] = 0 (Flash); CS# = V _{DD}	1, 2, 3	All		120	mA
		CR1[7] = 1 (SRAM); CS# = V _{DD}	1, 2, 3	All		50	mA
Standby Current QPI Mode	I _{SB}	RESET#, CS# = V _{DD} ; SI, SCK = V _{DD} or V _{SS}	1, 2, 3	All		12	mA
Power On Reset Current (In-rush) <u>4/</u>	I _{POR}	RESET#, CS# = V _{DD} ; SI, SCK = V _{DD} or V _{SS}	1, 2, 3	All		100	mA
Input Capacitance (applies to SCK, CS#, RESET#)	C _{IN}	1 MHz, See 4.4.1e	4	All		8	pF
Output Capacitance (applies to All I/O)	C _{OUT}	1 MHz, See 4.4.1e	4	All		8	pF
Functional tests		See 4.4.1c	7, 8A, and 8B	All			

RESET# PARAMETERS

RESET# setup	t _{RS}		9, 10, 11	All	50		ns
RESET# hold (w.r.t CS#)	t _{RH} (t _{RPH})		9, 10, 11	All	1.5		ms
RESET# pulse width	t _{RP}		9, 10, 11	All	200		ns
Internal device reset	t _{RESET}		9, 10, 11	All	300		μs

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC CHARACTERISTICS							
SCK clock frequency for READ and 4READ instructions	F _{SCK, R}	See Figure 4	9, 10, 11	All	DC	33	MHz
SCK clock frequency for the following quad commands: FAST_READ, 4FAST_READ, QOR, 4QOR, QIOR, 4QIOR	F _{SCK, C}		9, 10, 11	All	DC	133	MHz
SCK Clock Period	P _{SCK}		9, 10, 11	All	1 / F _{SCK}		
Clock High Time	t _{WH} , t _{CH}		9, 10, 11	All	50% P _{SCK} ± 5%		ns
Clock Low Time	t _{WL} , t _{CL}		9, 10, 11	All	50% P _{SCK} ± 5%		ns
Clock Rise Time (slew rate) <u>2</u> /	t _{CRT} , t _{CLCH}		9, 10, 11	All	1.5		V/ns
Clock Fall Time (slew rate) <u>2</u> /	t _{CFT} , t _{CHCL}		9, 10, 11	All	1.5		V/ns
CS# HIGH Time (Any Read Instructions)	t _{CS}		9, 10, 11	All	40		ns
CS# HIGH Time (All other Non-Read instructions)			9, 10, 11	All	50		ns
CS# Active Setup Time (relative to SCK)	t _{CSS}		9, 10, 11	All	4.5		ns
CS# Active Hold Time (relative to SCK)	t _{CSH}		9, 10, 11	All	5.5		ns
Data in Setup Time	t _{SU}		9, 10, 11	All	2.0		ns
Data in Hold Time	t _{HD}		9, 10, 11	All	4.0		ns
Clock Low to Output Valid (30 pF Loading, V _{DDIO} = 3.3 V)	t _{v1}		9, 10, 11	All		8.5	ns
Clock Low to Output Valid (15 pF Loading, V _{DDIO} = 3.3 V)			9, 10, 11	All		6.5	ns
Clock Low to Output Valid (30 pF Loading, V _{DDIO} = 1.8 V)	t _{v2}		9, 10, 11	All		10	ns
Clock Low to Output Valid (15 pF Loading, V _{DDIO} = 1.8 V)			9, 10, 11	All		8	ns
See footnotes at end of table.							
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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC CHARACTERISTICS – CONTINUED							
Output Hold Time	t _{HO}	See Figure 4	9, 10, 11	All	1		ns
Output Disable Time 4/	t _{DIS}		9, 10, 11	All		12	ns
Output Disable Time (Reset & Quad enabled) 4/	t _{DIS2}		9, 10, 11	All		20	ns
WP# Setup Time 3/	t _{WPS}		9, 10, 11	All	20		ns
WP# Hold Time 3/	t _{WPH}		9, 10, 11	All	50		ns
PROGRAM AND ERASE PERFORMANCE							
Non-volatile Register Write Time	t _W		9, 10, 11	All		32	ms
Page Programming (2048 Bytes)	t _{PP}		9, 10, 11	All		32	ms
Sector Erase Time (1 MByte)	t _{SE}		9, 10, 11	All		22	ms
Block Erase Time (8 MBytes)	t _{BE}		9, 10, 11	All		176	ms
Chip Erase Time (64 MBytes)	t _{CE}		9, 10, 11	All		1.41	s
Page Scrub Time (2048 Bytes)	t _{PSR}		9, 10, 11	All		32	ms
Chip Scrub Time (64 MBytes) (CR1[7] = 0) Flash	t _{CSR1}		9, 10, 11	All		1048	s
Chip Scrub Time (CR1[7] = 1) SRAM	t _{CSR2}		9, 10, 11	All		1	ms
PROGRAM OR ERASE SUSPEND AC PARAMETERS							
Suspend Latency	t _{SL}		9, 10, 11	All		40	μs
Resume to next Suspend	t _{RNS}		9, 10, 11	All	100		μs
1/ Outputs unconnected during read data return. Output switching current is not included. 2/ t_{CRT}, t_{CLCH} Clock Rise and fall slew rate for Fast clock (133 MHz) min is 1.5 V/ns and for Slow Clock (40 MHz) min is 1.0 V/ns. 3/ Only applicable as a constraint for WRR or WRAR instruction when SRP0 is set to a '1'. 4/ Guaranteed by design.							
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Table IB. SEP test limits. 1/ 2/

Device type	Single Event Upset 3/ $V_{DD} = 1.63$		Single Event Latch-up (SEL) test Bias $V_{DD} = V_{DDIO} = 3.6$ V
	SEFI/SEU error rate at in-situ LET 5/	SEU/SEFI error rate	Effective LET No SEL occurs 4/
All	2.5 MeV/(mg/cm ²)	2.77×10^{-5} errors/dev-day	80 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Test temperature $T_A = +25^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

4/ Worst case test temperature $T_A = +125^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

5/ Heavy ion single event effects (SEE) test was performed at the Texas A&M K500 Cyclotron facility. For single event latch-up (SEL) Xe ion beam was used and observed no rail to trail latch up occurred at an effective LET = 80 MeV-cm²/mg. However, high current events were observed at LET value 60.5 at 85°C and above. For single event functional interrupt (SEFI) error rate = 2.77×10^{-5} errors/dev-day to consider SEU error rate per CREME96 Geosynchronous orbit. For details SEE test report contact the device manufacturer.

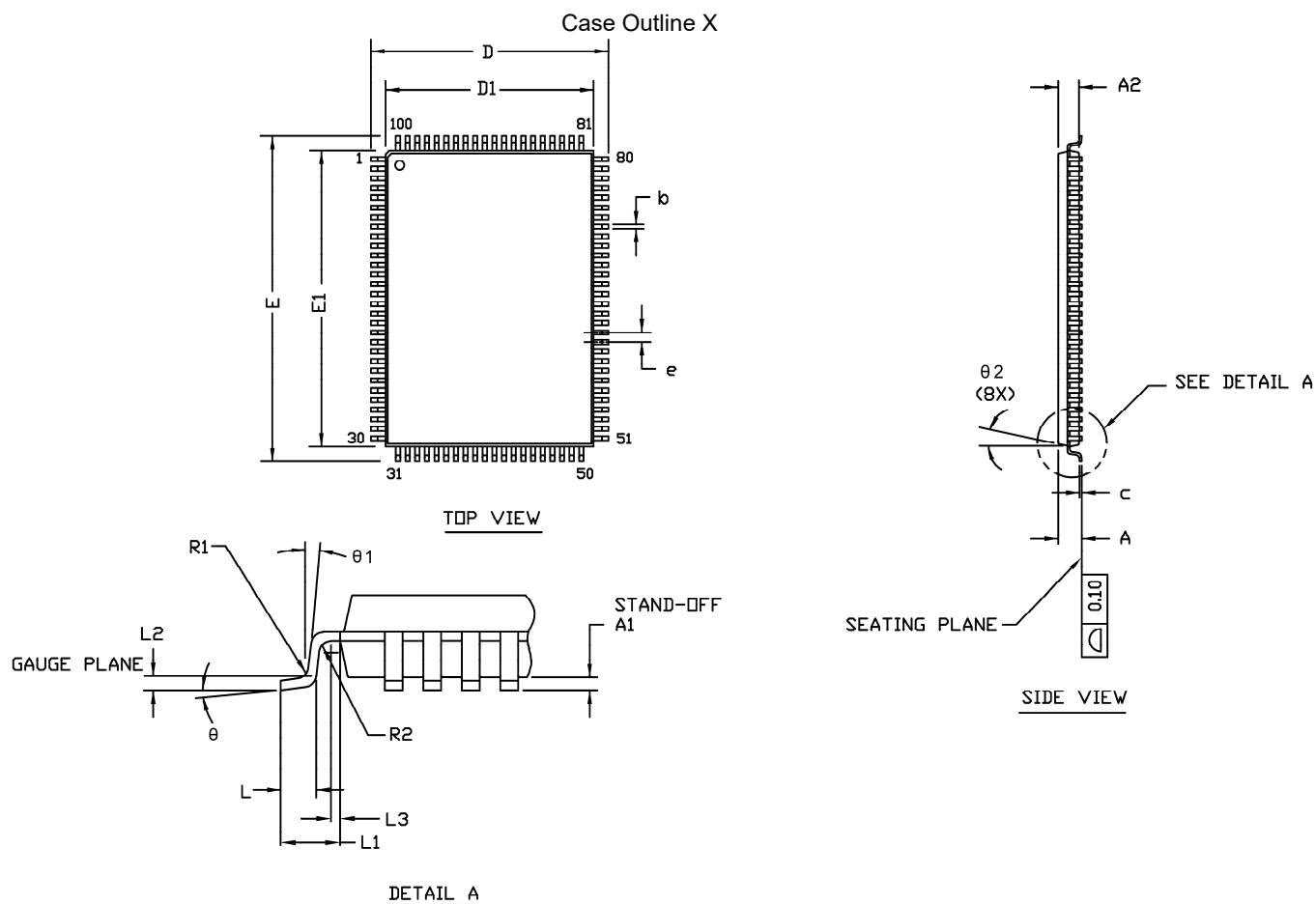
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SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.06
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
c		0.20		0.008
D	15.80	16.20	0.622	0.638
D1	13.90	14.10	0.547	0.555
E	21.80	22.20	0.858	0.874
E1	19.90	20.10	0.783	0.791
e	0.65 TYP		0.026 TYP	

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.25 BSC		0.010 BSC	
L3	0.20		0.008	
R1	0.08	0.20	0.003	0.008
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	0.276°
θ1	0°		0°	
θ2	11°	13°	0.433°	0.472°
N	100			

NOTE

1. Controlling dimensions are millimeters, inch dimensions are given for reference only.
2. Body length dimension does not include mold protrusion/end flash. Mold protrusion/end flash shall not exceed 0.0098 IN. (0.25 MM) per side. Body length dimensions are max plastic body size including mold mismatch.
3. JEDEC Specification No. REF: MS-026

FIGURE 1. Case outline.

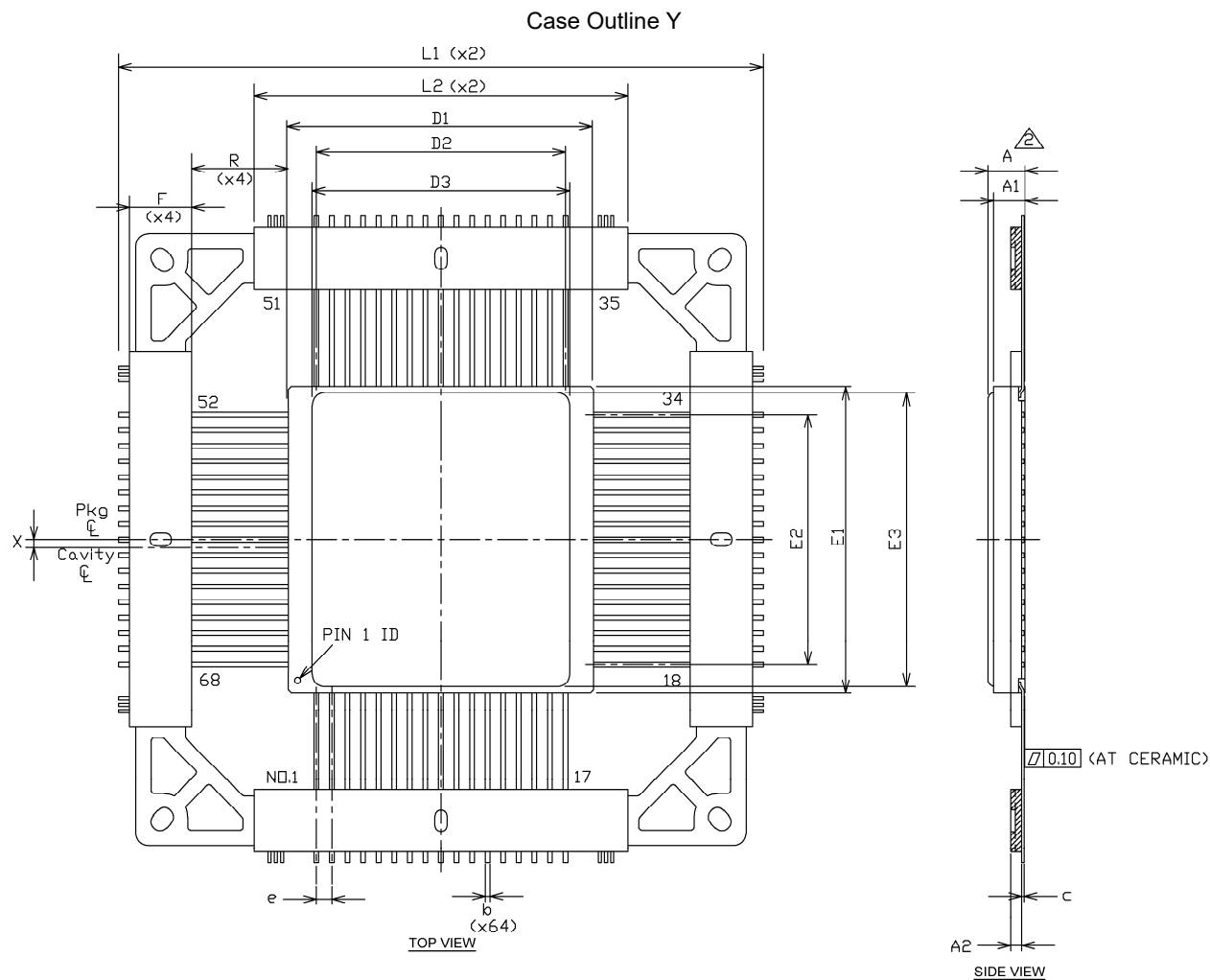
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SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		3.28		0.129
A1	2.54 BSC		0.100 BSC	
A2	0.76	1.02	0.030	0.040
b	0.33	0.43	0.013	0.017
c	0.15	0.25	0.006	0.010
D1/E1	24.66	25.12	0.970	0.989
D2/E2	20.19	20.45	0.795	0.805
D3	21.01 BSC		0.827 BSC	

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E3	23.88 BSC		0.940 BSC	
e	1.14	1.40	0.045	0.055
F	4.44	5.72	0.175	0.225
L1	52.33	52.83	2.060	2.080
L2	30.10	30.86	1.185	1.215
R	7.875 BSC		0.310 BSC	
X	0.635 BSC		0.025 BSC	
N	68			

NOTE

1. Controlling dimensions are millimeters, inch dimensions are given for reference only.
2. Reference NTK DWG Number: IFK68F4-2963A-ND

FIGURE 1. Case outline – continued.

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CASE OUTLINE X									
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V _{DDIO}	21	V _{SS}	41	NC	61	NC	81	NC
2	NC	22	V _{SS}	42	NC	62	NC	82	NC
3	NC	23	V _{DD}	43	NC	63	V _{SS}	83	NC
4	NC	24	INT#	44	NC	64	DNU	84	NC
5	NC	25	DNU	45	NC	65	DNU	85	NC
6	DNU	26	NC	46	NC	66	DNU	86	NC
7	RESET#	27	NC	47	NC	67	NC	87	NC
8	CS#	28	NC	48	NC	68	NC	88	NC
9	V _{SS}	29	NC	49	NC	69	NC	89	NC
10	V _{DD}	30	V _{DDIO}	50	NC	70	NC	90	NC
11	V _{SS}	31	V _{SS}	51	NC	71	NC	91	NC
12	SI/IO0	32	DNU	52	NC	72	V _{SS}	92	NC
13	SO/IO1	33	DNU	53	NC	73	V _{DD}	93	NC
14	V _{DDIO}	34	DNU	54	NC	74	NC	94	NC
15	V _{SS}	35	V _{SS}	55	NC	75	NC	95	V _{DD}
16	SCK	36	V _{DD}	56	NC	76	NC	96	V _{SS}
17	V _{SS}	37	NC	57	NC	77	NC	97	DNU
18	V _{DDIO}	38	NC	58	NC	78	NC	98	DNU
19	WP# / IO2	39	NC	59	V _{DD}	79	NC	99	DNU
20	IO3	40	NC	60	V _{SS}	80	NC	100	V _{SS}

NOTES:

1. NC pins are no connect and are not connected on the die.
2. DNU pins are connected and may not be biased.
3. The RESET# input has an internal pull-up and may be left unconnected if hardware reset is not in use.

CASE OUTLINE Y							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	18	V _{DD}	35	NC	52	V _{DD}
2	DNU	19	NC	36	NC	53	DNU
3	DNU	20	NC	37	NC	54	RESET#
4	NC	21	NC	38	NC	55	CS#
5	V _{DD}	22	NC	39	NC	56	NC
6	V _{SS}	23	NC	40	NC	57	V _{DDIO}
7	NC	24	NC	41	NC	58	SI/IO0
8	V _{DD}	25	NC	42	NC	59	SO/IO1
9	V _{SS}	26	NC	43	V _{SS}	60	V _{SS}
10	NC	27	NC	44	V _{DD}	61	SCK
11	NC	28	V _{DDIO}	45	NC	62	WP# / IO2
12	NC	29	V _{SS}	46	DNU	63	IO3
13	NC	30	NC	47	DNU	64	V _{DDIO}
14	NC	31	NC	48	DNU	65	INT#
15	NC	32	V _{DD}	49	NC	66	DNU
16	NC	33	V _{DDIO}	50	NC	67	V _{DD}
17	NC	34	V _{SS}	51	NC	68	V _{SS}

NOTES:

1. NC pins are no connect and are not connected on the die.
2. DNU pins are connected and may not be biased.
3. The RESET# input has an internal pull-up and may be left unconnected if hardware reset is not in use.

FIGURE 2. Terminal connections.

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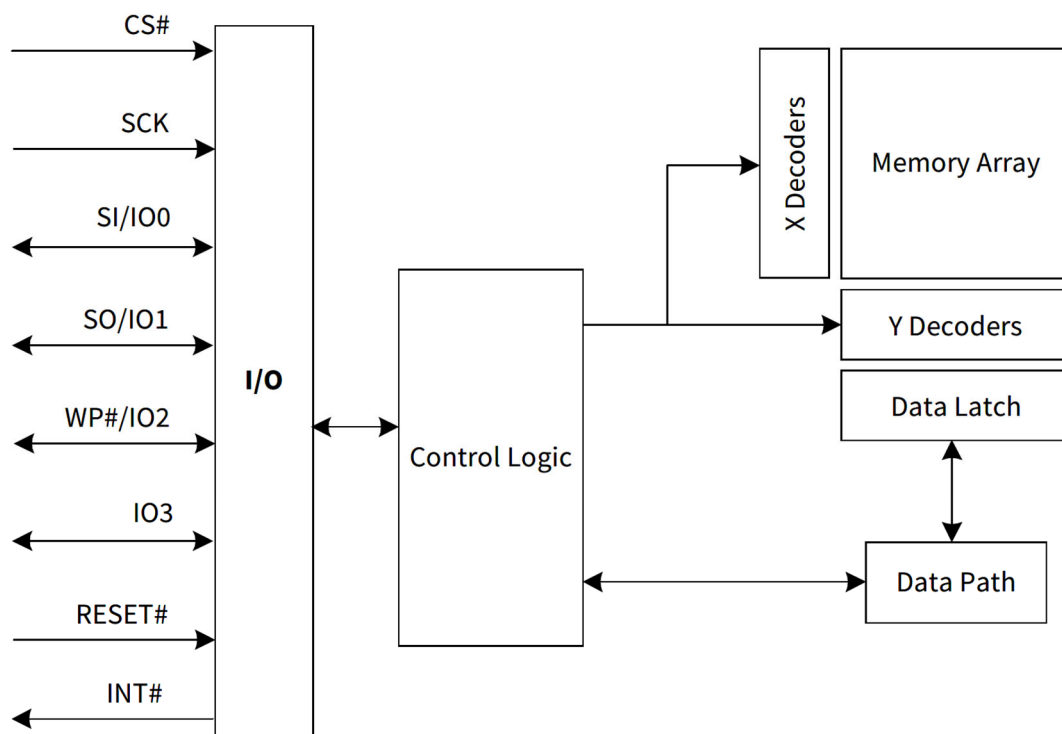


FIGURE 3. Block diagram.

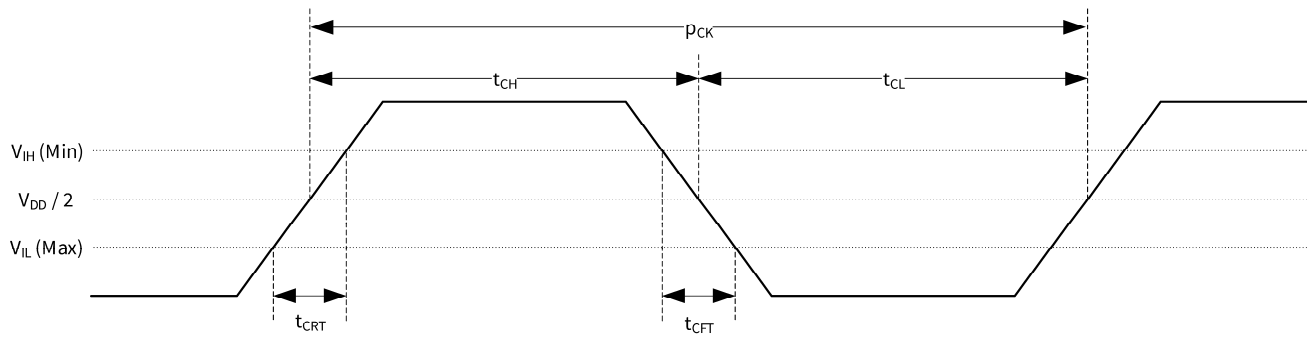
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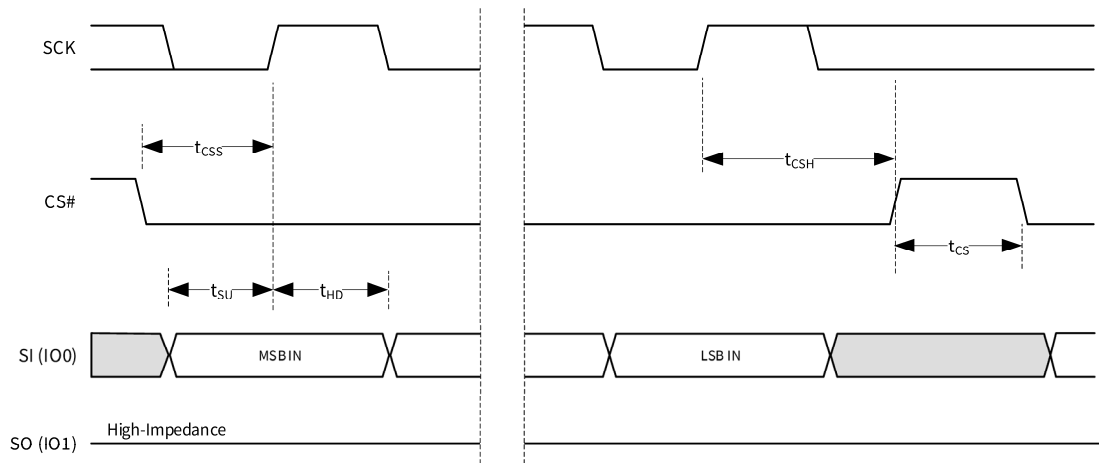
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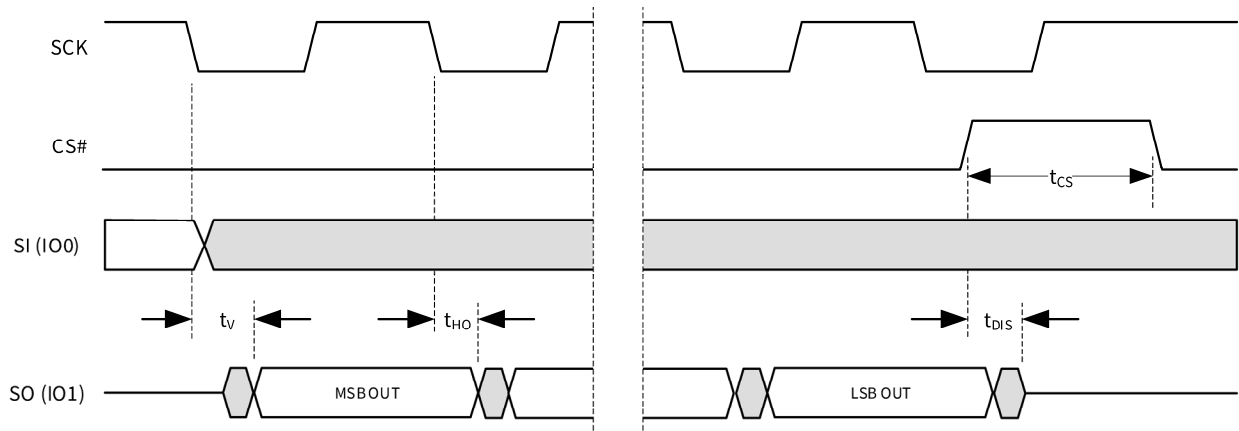
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Clock Timing



SPI single bit input timing



SPI single bit output timing

FIGURE 4. Timing waveforms.

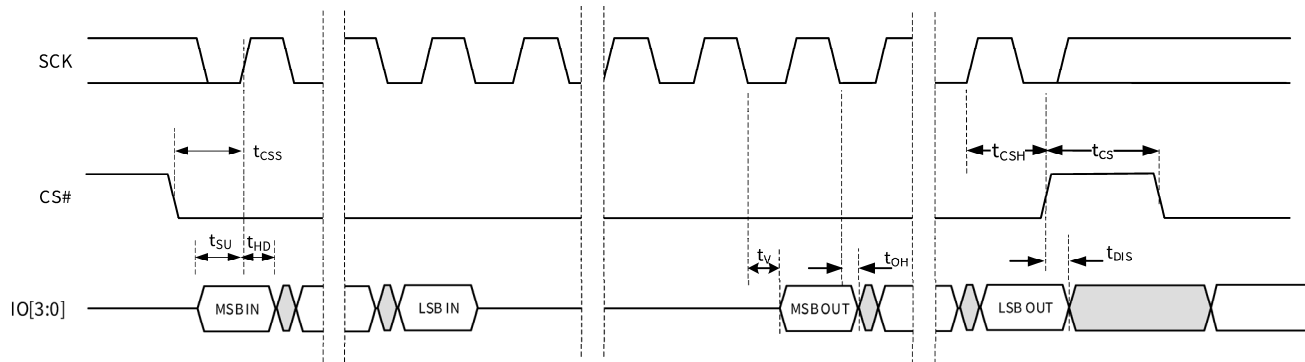
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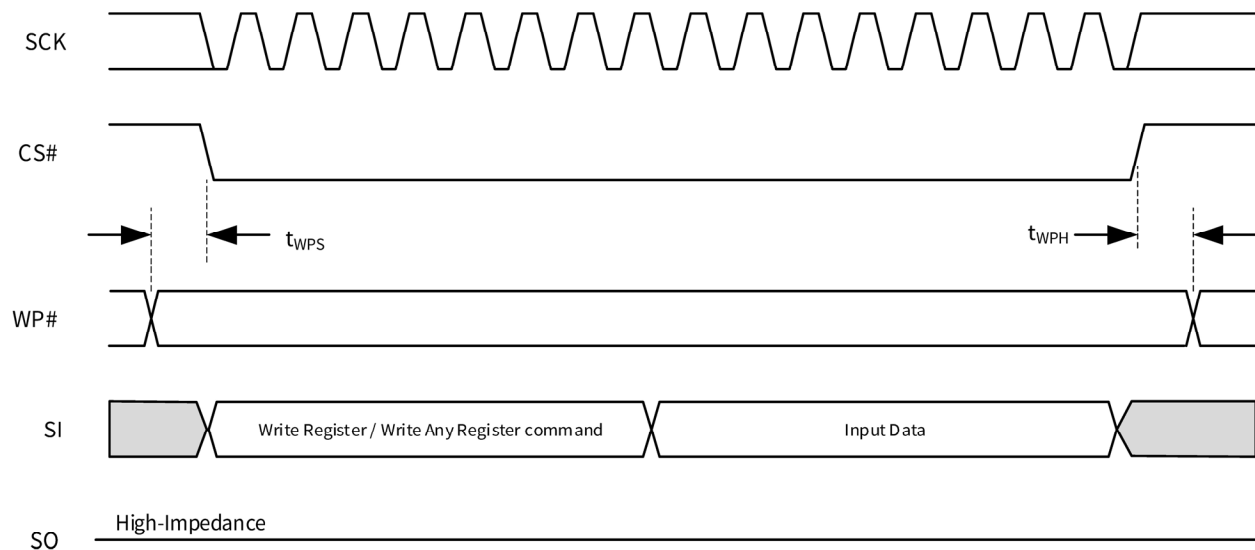
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Quad / QPI timing



WP# input timing

FIGURE 4. Timing waveforms – continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes N, P, Q, Y, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, P, Q, Y, and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, P, Q, Y, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, P, Q, Y, and V. Qualification inspection for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes N, P, Q, Y, and V subgroups 7, 8A and 8B shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, P, Q, Y, and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. In addition, special test structures may be used for latch-up characterization in place of using product. If test structures are used, testing shall be on five wafers. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)				
	Device class N	Device class P	Device class Q	Device class V	Device class Y
Interim electrical parameters (see 4.2)		1*, 7*, 9	Not Required	1*, 7*, 9	
Static burn-in (method 1015)		Required	Not Required	Required	
Same as line 1		1*, 7*, 9 Δ	Not Required	1*, 7*, 9 Δ	
Dynamic burn-in (method 1015)		Required	Required	Required	
Final electrical parameters (see 4.2)		1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ	
Group A test requirements (see 4.4)		1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	
Group C endpoint electrical parameters (see 4.4)		1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	
Group D endpoint electrical parameters (see 4.4)		1, 7, 9	1, 7, 9	1, 7, 9	
Group E endpoint electrical parameters (see 4.4)		1, 7, 9	1, 7, 9	1, 7, 9	

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroups 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limits	Units
I _{CC}	± 10% of the measured value	mA
I _{SB}	± 340	μA
I _{LI} , I _{LO}	± 1	μA
V _{OH}	± 10% of the measured value	mV
V _{OL}	± 3	mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall correspond to the test defined in table IA (electrical performance characteristics). The drift values shall not be limits shall correspond to the test defined in table IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes N, P, Q, Y, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. Preconditioning shall be performed on non-hermetic device classes N, P, and Y surface mount devices as specified in the manufacturer's QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes N, P, Q, Y, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A (effective dose rate 2.78 rad/s), as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} + 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on classes P and V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$. The latch-up test temperature shall be at 115°C .
- f. Bias conditions shall be V_{DD} maximum = 2.0 V dc for the upset measurements and V_{DD} max = 3.6 V dc for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

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4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ after an exposure of 5×10^{14} neutrons/cm².

4.5 Delta measurements for device classes P and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, P, Q, Y, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, P, Q, Y, and V. Sources of supply for device classes N, P, Q, Y, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Occurrence of latch-up (SEL).

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APPENDIX A
Appendix A forms a part of SMD 5962-21222
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 1.4 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.

- Step 1. Increment address from minimum to maximum writing each address with solid data pattern (xFF).
- Step 2. Increment address from minimum to maximum while performing 2a and 2b.
 - Step 2a. Read and verify an address.
 - Step 2b. Write the address with complement data.
- Step 3. Increment address from minimum to maximum while performing 3a, 3b, 3c, 3d.
 - Step 3a. Read and verify an address.
 - Step 3b. Write the address with complement data.
 - Step 3c. Read and verify the address.
 - Step 3d. Write the address with complement data.

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APPENDIX A – Continued.
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FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solid.

- Step 1. Write x55 data pattern to all addresses from minimum to maximum.
- Step 2. Read and verify x55 data pattern at all addresses.
- Step 3. Write xAA data pattern to all addresses from minimum to maximum.
- Step 4. Read and verify xAA data pattern at all addresses.
- Step 5. Write xFF data pattern to all addresses from minimum to maximum.
- Step 6. Read and verify xFF data pattern at all addresses.
- Step 7. Write x00 data pattern to all addresses from minimum to maximum.
- Step 8. Read and verify x00 data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verification.

Each test performed independently.

Write Protect Functional test: Write data with Software Write Protect set for given array block, read data and confirm no data change.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 25-03-06

Approved sources of supply for SMD 5962-21222 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962F2122201PXE	65786	CYRS17B512-133AZMB
5962F2122202VYC	65786	CYRS17B512-133UZMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.