

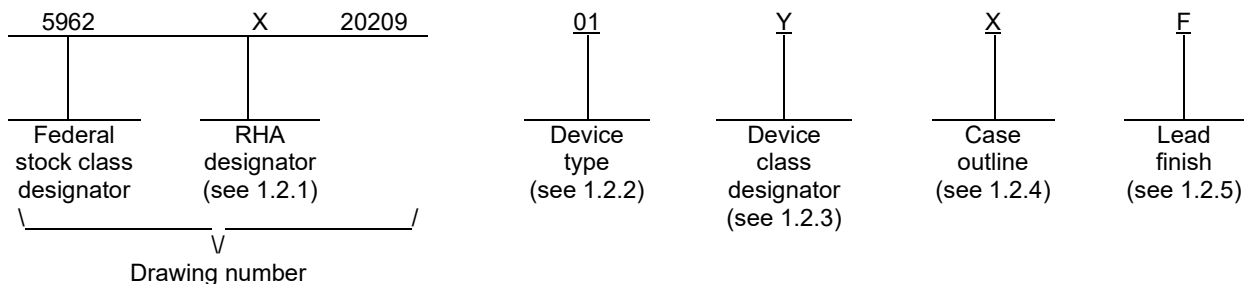
REVISIONS																				
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED				
																				
REV																				
SHEET	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69					
REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV																
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY Phu H. Nguyen							DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime									
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Phu H. Nguyen																
				APPROVED BY Muhammad A. Akbar							MICROCIRCUIT, DIGITAL, CERAMIC, NON-HERMATIC FLIP CHIP (CLASS Y DEVICE), POWER QUICC III INTEGRATED PROCESSOR, MONOLITHIC SILICON									
				DRAWING APPROVAL DATE 21-03-09																
				REVISION LEVEL							SIZE A	CAGE CODE 67268	5962-20209							
												SHEET 1 OF 69								

1. SCOPE

1.1 Scope. This drawing documents product assurance class level consisting of high reliability space application device class Y ceramic non-hermetic flip chip device. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class Y:



1.2.1 RHA designator. Device class Y RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	8548E	1200/400 MHz	Power QUICC III Integrated Processor
02	8548E	1333/533 MHz	Power QUICC III Integrated Processor
03	8548	1200/400 MHz	Power QUICC III Integrated Processor
04	8548	1333/533 MHz	Power QUICC III Integrated Processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below.

Device class	Device requirements documentation
Y	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 or as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	783	Flip Chip – Ceramic Ball Grid Array (FC-CBGA) <u>1/</u>
Y	See figure 2	783	Flip Chip – Ceramic Column Grid Array (FC-CCGA) <u>2/</u>

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class Y.

1/ Terminal lead finish F is tin lead alloy. Package case outline X solder balls material is Sn= 63% and Pb=37%.

2/ Terminal lead finish F is tin lead alloy with copper spiral column. Package case outline Y solder columns material is Sn= 15%, Pb=85% and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

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1.3 Absolute maximum ratings. 3/

Core supply voltage, (V_{DD})	-0.3 V to 1.21 V
PLL supply voltage, (AV_{DD})	-0.3 V to 1.21 V
Core power supply for SerDes transceivers, (SV_{DD})	-0.3 V to 1.21 V
Pad power supply for SerDes transceivers, (XV_{DD})	-0.3 V to 1.21 V
DDR and DDR2 DRAM I/O voltage, (GV_{DD})	-0.3 V to 2.75 V and -0.3 V to 1.98 V <u>4/</u>
Three-speed Ethernet I/O voltage:	
LV_{DD} (for eTSEC1 and eTSEC2)	-0.3 V to 3.63 V and -0.3 V to 2.75 V <u>5/</u>
TV_{DD} (for eTSEC3 and eTSEC4)	-0.3 V to 3.63 V and -0.3 V to 2.75 V <u>5/</u>
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage, (OV_{DD})	
	-0.3 V to 3.63 V <u>5/</u>
Local bus I/O voltage, (BV_{DD})	-0.3 V to 3.63 V and -0.3 V to 2.75 V <u>5/</u>
Input voltage	
DDR/DDR2 DRAM signals, (MV_{IN})	-0.3 V to ($GV_{DD} + 0.3$) V <u>6/</u>
DDR/DDR2 DRAM reference, (MV_{REF})	-0.3 V to ($GV_{DD}/2 + 0.3$) V
Three-speed Ethernet I/O signals:	
(LV_{IN})	-0.3 V to ($LV_{DD} + 0.3$) V <u>6/</u>
(TV_{IN})	-0.3 V to ($TV_{DD} + 0.3$) V <u>6/</u>
Local bus signals, (BV_{IN})	-0.3 V to ($BV_{DD} + 0.3$) V
DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals, (OV_{IN})	
	-0.3 V to ($OV_{DD} + 0.3$) V <u>6/</u>
PCI/PCI-X, (OV_{IN})	-0.3 V to ($OV_{DD} + 0.3$) V <u>6/</u>
Storage temperature range, (T_{STG})	-55°C to 150°C

3/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4/ The -0.3 to 2.75 V range is for DDR and -0.3 to 1.98 V range is for DDR2.

5/ The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See manufacturer data sheet on “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications” for details on the recommended operating conditions per protocol.

6/ (M, L, O) V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in FIGURE 4.

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1.4 Recommended operating conditions.

Core supply voltage, (V_{DD})	1.1 V $\pm$ 55 mV	
PLL supply voltage, (AV_{DD})	1.1 V $\pm$ 55 mV	<u>7/</u>
Core power supply for SerDes transceivers, (SV_{DD})	1.1 V $\pm$ 55 mV	
Pad power supply for SerDes transceivers, (XV_{DD})	1.1 V $\pm$ 55 mV	
DDR and DDR2 DRAM I/O voltage, (GV_{DD})	2.5 V $\pm$ 125 mV and 1.8 V $\pm$ 90 mV	
Three-speed Ethernet I/O voltage:		
(LV_{DD})	3.3 V $\pm$ 165 mV and 2.5 V $\pm$ 125 mV	<u>10/</u>
(TV_{DD})	3.3 V $\pm$ 165 mV and 2.5 V $\pm$ 125 mV	<u>10/</u>
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage, (OV_{DD})		
	3.3 V $\pm$ 165 mV	<u>9/</u>
Local bus I/O voltage, (BV_{DD})	3.3 V $\pm$ 165 mV and 2.5 V $\pm$ 125 mV	
Input voltage:		
DDR and DDR2 DRAM signals, (MV_{IN})	GND to GV_{DD}	<u>8/</u>
DDR and DDR2 DRAM reference, (MV_{REF})	GND to $GV_{DD}/2$	<u>8/</u>
Three-speed Ethernet signals,		
(LV_{IN})	GND to LV_{DD}	<u>10/</u>
(TV_{IN})	GND to TV_{DD}	
Local bus signals, (BV_{IN})	GND to BV_{DD}	
PCI, DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals, (OV_{IN})		
	GND to OV_{DD}	<u>9/</u>
Operating temperature range (T_J , T_C)	$T_C = -55^{\circ}\text{C}$ to $T_J = 125^{\circ}\text{C}$	
Thermal characteristics.		

Characteristic	JEDEC Board	Value		Unit
		Case X	Case Y	
Die Junction-to-Ambient (Natural Convection), $R_{\theta JA}$ <u>11/ 12/</u>	Single-layer board (1s)	17	17.3	$^{\circ}\text{C/W}$
Die Junction-to-Ambient (Natural Convection), $R_{\theta JA}$ <u>11/ 12/</u>	Four-layer board (2s2p)	12	12.3	
Die Junction-to-Ambient (200 ft/min), $R_{\theta JA}$ <u>11/ 12/</u>	Single-layer board (1s)	11	11.3	
Die Junction-to-Ambient (200 ft/min), $R_{\theta JA}$ <u>11/ 12/</u>	Four-layer board (2s2p)	8	8.3	
Die Junction-to-Board, $R_{\theta JB}$ <u>13/</u>	N/A	3	3.3	
Die Junction-to-Case, $R_{\theta JC}$ <u>14/</u>	N/A	0.8	0.8	

- 7/ This voltage is the input to the filter discussed in manufacturer data sheet on "PLL Power Supply Filtering" and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
- 8/ Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power on reset and power-down sequences.
- 9/ Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power on reset and power-down sequences.
- 10/ Caution: L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 11/ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 12/ Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 13/ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 14/ Thermal resistance between the die and the case top surface as determined by thermal simulation.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD51-6	–	Integrated Circuit Thermal Test Method Environmental Conditions
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board
JESD57	–	Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation
J-STD-020	–	Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices
JEP163	–	Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits
JESD22-B117	–	Solder ball shear test method
JESD471	–	Symbol and Label for Electrostatic Sensitivity Devices.
JESD625	–	Requirements for Handling Electrostatic Discharge Sensitive (ESDs) Devices

(Copies of these documents are available online at <https://www.jedec.org>)

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org>).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class Y.

3.2.1 Case outline X. The case outline X shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Case outline Y. The case outline Y shall be in accordance with 1.2.4 herein and figure 2.

3.2.3 Block diagram. The Block Diagram shall be as specified on figure 3.

3.2.4 Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}$. The Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}$ shall be as specified on figure 4.

3.2.5 Timing Diagram for t_{DDKMHM} . The Timing Diagram for t_{DDKMHM} shall be as specified on figure 5.

3.2.6 DDR SDRAM Output Timing Diagram. The DDR SDRAM Output Timing Diagram shall be as specified on figure 6.

3.2.7 DDR AC Test Load. The DDR AC Test Load shall be as specified on figure 7.

3.2.8 FIFO Transmit AC Timing Diagram. The FIFO Transmit AC Timing Diagram shall be as specified on figure 8.

3.2.9 FIFO Receive AC Timing Diagram. The FIFO Receive AC Timing Diagram shall be as specified on figure 9.

3.2.10 GMII Transmit AC Timing Diagram. The GMII Transmit AC Timing Diagram shall be as specified on figure 10.

3.2.11 GMII Receive AC Timing Diagram. The GMII Receive AC Timing Diagram shall be as specified on figure 11.

3.2.12 MII Transmit AC Timing Diagram. The MII Transmit AC Timing Diagram shall be as specified on figure 12.

3.2.13 eTSEC AC Test Load. The eTSEC AC Test Load shall be as specified on figure 13.

3.2.14 MII Receive AC Timing Diagram. The MII Receive AC Timing Diagram shall be as specified on figure 14.

3.2.15 TBI Transmit AC Timing Diagram. The TBI Transmit AC Timing Diagram shall be as specified on figure 15.

3.2.16 TBI Receive AC Timing Diagram. The TBI Receive AC Timing Diagram shall be as specified on figure 16.

3.2.17 TBI Single-Clock Mode Receive AC Timing Diagram. The TBI Single-Clock Mode Receive AC Timing Diagram shall be as specified on figure 17.

3.2.18 RGMII and RTBI AC Timing and Multiplexing Diagrams. The RGMII and RTBI AC Timing and Multiplexing Diagrams shall be as specified on figure 18.

3.2.19 RMII Transmit AC Timing Diagram. The RMII Transmit AC Timing Diagram shall be as specified on figure 19.

3.2.20 eTSEC AC Test Load. The eTSEC AC Test Load shall be as specified on figure 20.

3.2.21 RMII Receive AC Timing Diagram. The RMII Receive AC Timing Diagram shall be as specified on figure 21.

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- 3.2.22 MII Management Interface Timing Diagram. The MII Management Interface Timing Diagram shall be as specified on figure 22.
- 3.2.23 Local Bus AC Test Load. The Local Bus AC Test Load shall be as specified on figure 23.
- 3.2.24 Local Bus Signals, (PLL Enabled). The Local Bus Signals, (PLL Enabled) shall be as specified on figure 24.
- 3.2.25 Local Bus Signals (PLL Bypass Mode). The Local Bus Signals (PLL Bypass Mode) shall be as specified on figure 25.
- 3.2.26 Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled). The Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled) shall be as specified on figure 26.
- 3.2.27 Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode). The Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode) shall be as specified on figure 27.
- 3.2.28 Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled). The Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled) shall be as specified on figure 28.
- 3.2.29 Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode). The Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode) shall be as specified on figure 29.
- 3.2.30 AC Test Load for the JTAG Interface. The AC Test Load for the JTAG Interface shall be as specified on figure 30.
- 3.2.31 JTAG Clock Input Timing Diagram. The JTAG Clock Input Timing Diagram shall be as specified on figure 31.
- 3.2.32 TRST Timing Diagram. The TRST Timing Diagram shall be as specified on figure 32.
- 3.2.33 Boundary-scan Timing Diagram. The Boundary-scan Timing Diagram shall be as specified on figure 33.
- 3.2.34 I²C AC Test Load. The I²C AC Test Load shall be as specified on figure 34.
- 3.2.35 I²C Bus AC Timing Diagram. The I²C Bus AC Timing Diagram shall be as specified on figure 35.
- 3.2.36 PCI/PCI-X Input AC Timing Measurement Conditions. The PCI/PCI-X Input AC Timing Measurement Conditions shall be as specified on figure 36.
- 3.2.37 PCI/PCI-X Output AC Timing Measurement Condition. The PCI/PCI-X Output AC Timing Measurement Condition shall be as specified on figure 37.
- 3.2.38 PCI/PCI-X Output AC Timing Measurement Condition. The PCI/PCI-X Output AC Timing Measurement Condition shall be as specified on figure 38.
- 3.2.39 Differential Voltage Definitions for Transmitter or Receiver. The Differential Voltage Definitions for Transmitter or Receiver shall be as specified on figure 39.
- 3.2.40 Receiver of SerDes Reference Clocks. The Receiver of SerDes Reference Clocks shall be as specified on figure 40.
- 3.2.41 Differential Reference Clock Input DC Requirements (External DC-Coupled). The Differential Reference Clock Input DC Requirements (External DC-Coupled) shall be as specified on figure 41.
- 3.2.42 Differential Reference Clock Input DC Requirements (External AC-Coupled). The Differential Reference Clock Input DC Requirements (External AC-Coupled) shall be as specified on figure 42.
- 3.2.43 Single-Ended Reference Clock Input DC Requirements. The Single-Ended Reference Clock Input DC Requirements shall be as specified on figure 43.

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- 3.2.44 DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only). The DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only) shall be as specified on figure 44.
- 3.2.45 AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only). The AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only) shall be as specified on figure 45.
- 3.2.46 AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only). The AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only) shall be as specified on figure 46.
- 3.2.47 Single-Ended Connection (Reference Only). The Single-Ended Connection (Reference Only) shall be as specified on figure 47.
- 3.2.48 SerDes Transmitter and Receiver Reference Circuits. The SerDes Transmitter and Receiver Reference Circuits shall be as specified on figure 48.
- 3.2.49 Minimum Transmitter Timing and Voltage Output Compliance Specifications. The Minimum Transmitter Timing and Voltage Output Compliance Specifications shall be as specified on figure 49.
- 3.2.50 Minimum Receiver Eye Timing and Voltage Compliance Specification. The Minimum Receiver Eye Timing and Voltage Compliance Specification shall be as specified on figure 50.
- 3.2.51 Compliance Test/Measurement Load. Compliance Test/Measurement Load shall be as specified on figure 51.
- 3.2.52 Differential Peak-to-Peak Voltage of Transmitter or Receiver. The Differential Peak-to-Peak Voltage of Transmitter or Receiver shall be as specified on figure 52.
- 3.2.53 Transmitter Output Compliance Mask. The Transmitter Output Compliance Mask shall be as specified on figure 53.
- 3.2.54 Single Frequency Sinusoidal Jitter Limits. The Single Frequency Sinusoidal Jitter Limits shall be as specified on figure 54.
- 3.2.55 Receiver Input Compliance Mask. The Receiver Input Compliance Mask shall be as specified on figure 55.

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3.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5.1 Solderability test for BGA/CGA packages: Solderability test for case outline X for BGA and Y for CGA package have been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For class Y packages wherein marking of the entire SMD PIN number is required (see herein 1.2). For RHA product, the RHA designator shall still be marked. Marking for device class Y shall be used ink or laser mark in accordance with MIL-PRF-38535.

3.6.1 Certification/compliance mark. The certification mark for device class Y shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.7 Electrostatic discharge (ESD) sensitivity mark. ESD marking on devices and, on container/carriers are required as specified in MIL-PRF-38535. All of the markings shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive items (e.g., JESD471 symbol) shall be marked on the carrier or container.

3.8 Moisture sensitivity level (MSL) mark. Non-hermetic devices such as class Y can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device in accordance with J-STD-020.

3.9 Lot date code. Flip chip devices lot date code shall be assigned after underfill cured to identify the device with the assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, underfill sealing week and assembly location.

3.10 Certificate of compliance. For device class Y, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets for device class Y and the requirements of MIL-PRF-38535.

3.11 Certificate of conformance. A certificate of conformance as required for device class Y in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions	Group A subgroups	Limits			Unit
				Min	Typ	Max	
INPUT CLOCKS							
SYSCLK AC timing specifications 1/							
SYSCLK frequency 2/ 3/ 4/ 5/	f _{SYSCLK}		9, 10, 11	16		133	MHz
SYSCLK cycle time 3/ 4/ 5/	t _{SYSCLK}		167/	7.5		60	ns
SYSCLK rise and fall time 6/	t _{KH} , t _{KL}		167/	0.6	1.0	1.2	ns
SYSCLK duty cycle 7/	t _{KHK} /t _{SYSCLK}		167/	40		60	%
SYSCLK jitter 8/ 9/			9, 10, 11			±150	ps
EC GTX_CLK125 AC timing specifications							
EC GTX_CLK125 frequency	f _{G125}		9, 10, 11		125		MHz
EC GTX_CLK125 cycle time	t _{G125}		9, 10, 11		8		ns
EC GTX_CLK125 rise and fall time 12/	t _{G125R} /t _{G125F}	L/TVDD = 2.5V	9, 10, 11			0.75	ns
		L/TVDD = 3.3V	167/			1.0	
EC GTX_CLK125 duty cycle 9/ 13/	t _{G125H} /t _{G125}	GMII, TBI	167/	45		55	%
		1000Base-T for RGMII, RTBI	167/	47		53	
PCIn_CLK AC timing specifications 1/							
PCIn_CLK frequency	f _{PCICLK}		9, 10, 11	16		133	MHz
PCIn_CLK cycle time	t _{PCICLK}		9, 10, 11	7.5		60	ns
PCIn_CLK rise and fall time 12/ 7/	t _{PCIKH} , t _{PCIKL}		167/	0.6	1.0	2.1	ns
PCIn_CLK duty cycle 7/	t _{PCIKHKL} /t _{PCICLK}		167/	40		60	%
RESET INITIALIZATION							
RESET initialization timing specifications							
Required assertion time of HRESET			9, 10, 11	100			μs
Minimum assertion time for SRESET 13/			9, 10, 11	3			SYSCLKs
PLL input setup time with stable SYSCLK before HRESET negation 13/			9, 10, 11	100			μs
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET 13/			9, 10, 11	4			SYSCLKs
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET 13/			9, 10, 11	2			SYSCLKs
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET 13/			9, 10, 11			5	SYSCLKs
PLL lock times							
Core and platform PLL lock times			167/			100	μs
Local bus PLL lock time			167/			50	
PCI/PCI-X bus PLL lock time			167/			50	
Power supply ramp rate							
Required ramp rate for MVREF 14/			167/			3500	V/s
Required ramp rate for VDD 14/ 15/			167/			4000	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 16/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
DDR and DDR2 SDRAM							
DDR2 SDRAM DC Electrical characteristics for GV _{DD} (typ) = 1.8 V							
I/O supply voltage 17/	GV _{DD}		1, 2, 3	1.71		1.89	V
I/O reference voltage 18/	MV _{REF}		1, 2, 3	0.49 × GV _{DD}		0.51 × GV _{DD}	V
I/O termination voltage 19/	V _{TT}		1, 2, 3	MV _{REF} – 0.04		MV _{REF} + 0.04	V
Input high voltage	V _{IH}		1, 2, 3	MV _{REF} + 0.125		GV _{DD} + 0.3	V
Input low voltage	V _{IL}		1, 2, 3	–0.3		MV _{REF} – 0.125	V
Output leakage current 20/	I _{OZ}		1, 2, 3	–50		50	µA
Output high current (V _{OUT} = 1.420 V)	I _{OH}		1, 2, 3	–13.4			mA
Output low current (V _{OUT} = 0.280 V)	I _{OL}		1, 2, 3	13.4			mA
DDR2 SDRAM Capacitance for GV _{DD} (typ)=1.8V							
Input/output capacitance: DQ, DQS, <u>DQS</u> 21/	C _{IO}		167/	6		8	pF
Delta input/output capacitance: DQ, DQS, <u>DQS</u> 21/	C _{DIO}		167/			0.5	pF
DDR SDRAM DC electrical characteristics for GV _{DD} (typ) = 2.5 V							
I/O supply voltage 17/	GV _{DD}		1, 2, 3	2.375		2.625	V
I/O reference voltage 22/	MV _{REF}		1, 2, 3	0.49 × GV _{DD}		0.51 × GV _{DD}	V
I/O termination voltage 19/	V _{TT}		1, 2, 3	MV _{REF} – 0.04		MV _{REF} + 0.04	V
Input high voltage	V _{IH}		1, 2, 3	MV _{REF} + 0.15		GV _{DD} + 0.3	V
Input low voltage	V _{IL}		1, 2, 3	–0.3		MV _{REF} – 0.15	V
Output leakage current 20/	I _{OZ}		1, 2, 3	–50		50	µA
Output high current (V _{OUT} = 1.95 V)	I _{OH}		1, 2, 3	–16.2			mA
Output low current (V _{OUT} = 0.35 V)	I _{OL}		1, 2, 3	16.2			mA
DDR SDRAM capacitance for GV _{DD} (typ) = 2.5 V							
Input/output capacitance: DQ, DQS, <u>23/</u>	C _{IO}		167/	6		8	pF
Delta input/output capacitance: DQ, DQS, <u>23/</u>	C _{DIO}		167/			0.5	pF
Current draw characteristics for MV _{REF}							
Current draw for MV _{REF} 24/	I _{MVREF}					500	µA
DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface (At Recommended Operating Conditions)							
AC input low voltage	V _{IL}		9, 10, 11			MV _{REF} – 0.25	V
AC input high voltage	V _{IH}		9, 10, 11	MV _{REF} + 0.25			V
DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface (At Recommended Operating Conditions)							
AC input low voltage	V _{IL}		9, 10, 11			MV _{REF} – 0.31	V
AC input high voltage	V _{IH}		9, 10, 11	MV _{REF} + 0.31			V

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol <u>27/</u>	Test conditions <u>2/</u>	Group A subgroups	Limits		Unit
				Min	Max	
DDR and DDR2 SDRAM - Continued						
DDR SDRAM Input AC Timing Specifications (At Recommended Operating Conditions)						
Controller Skew for MDQS-MDQ/MECC <u>25/ 26/</u>	t_{CISKEW}	533 MHz	9, 10 ,11	-300	300	ps
		400 MHz	9, 10 ,11	-365	365	
		333 MHz	9, 10 ,11	-390	390	
DDR SDRAM Output AC Timing Specifications (At Recommended Operating Conditions) See FIGURE 5 to 7						
MCK[n] cycle time, $\overline{\text{MCK}}[n]/\text{MCK}[n]$ crossing <u>28/</u>	t_{MCK}		9, 10 ,11	3.75		ns
ADDR/CMD output setup with respect to MCK <u>29/</u>	t_{DDKHAS}	533 MHz	9, 10 ,11	1.48		
		400 MHz	9, 10 ,11	1.95		
		333 MHz	9, 10 ,11	2.40		
ADDR/CMD output hold with respect to MCK <u>29/</u>	t_{DDKHAX}	533 MHz	9, 10 ,11	1.48		
		400 MHz	9, 10 ,11	1.95		
		333 MHz	9, 10 ,11	2.40		
$\overline{\text{MCS}}[n]$ output setup with respect to MCK <u>29/</u>	t_{DDKHCS}	533 MHz	9, 10 ,11	1.48		
		400 MHz	9, 10 ,11	1.95		
		333 MHz	9, 10 ,11	2.40		
$\overline{\text{MCS}}[n]$ output hold with respect to MCK <u>29/</u>	t_{DDKHCS}	533 MHz	9, 10 ,11	1.48		
		400 MHz	9, 10 ,11	1.95		
		333 MHz	9, 10 ,11	2.40		
MCK to MDQS Skew <u>30/</u>	t_{DDKMH}		9, 10 ,11	-0.6	0.6	
MDQ/MECC/MDM output setup with respect to MDQS <u>31/</u>	$t_{\text{DDKHDS}},$ t_{DDKLDS}	533 MHz	9, 10 ,11	538		ps
		400 MHz	9, 10 ,11	700		
		333 MHz	9, 10 ,11	900		
MDQ/MECC/MDM output hold with respect to MDQS <u>31/</u>	$t_{\text{DDKHDX}},$ t_{DDKLDX}	533 MHz	9, 10 ,11	538		
		400 MHz	9, 10 ,11	700		
		333 MHz	9, 10 ,11	900		
MDQS preamble start <u>32/</u>	t_{DDKHMP}		9, 10 ,11	$-0.5 \times t_{\text{MCK}}$ $- 0.6$	$-0.5 \times t_{\text{MCK}}$ $+ 0.6$	ns
MDQS epilogue end <u>32/</u>	t_{DDKHME}		9, 10 ,11	-0.6	0.6	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>2/</u>	Group A subgroups	Limits		Unit
				Min	Max	
DUART						
DUART DC electrical characteristics						
High-level input voltage	V _{IH}		1, 2, 3	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		1, 2, 3	-0.3	0.8	
Input current (V _{IN} <u>33/</u> = 0V or V _{IN} = V _{DD})	I _{IN}		1, 2, 3		±5	µA
High-level output voltage (OV _{DD} = min, I _{OH} = -100 µA)	V _{OH}		1, 2, 3	OV _{DD} - 0.2		V
Low-level output voltage (OV _{DD} = min, I _{OL} = 100 µA)	V _{OL}		1, 2, 3		0.2	
DUART AC Timing specifications						
Minimum baud rate <u>34/ 35/</u>			<u>167/</u>	f _{CCB} /1,048,576		baud
Maximum baud rate <u>34/ 35/ 36/</u>			<u>167/</u>		f _{CCB} clock/16	
Oversample rate <u>34/ 37/</u>			<u>167/</u>	16		
ETHERNET: Enhanced three-Speed Ethernet (eTSEC), MII management						
GMII, MII, RMII, and TBI DC Electrical Characteristics						
Supply voltage 3.3V <u>38/ 39/</u>	LV _{DD} TV _{DD}		1, 2, 3	3.13	3.47	V
Output high voltage	V _{OH}	LV _{DD} /TV _{DD} = Min, I _{OH} = -4.0 mA	1, 2, 3	2.40	LV _{DD} /TV _{DD} + 0.3	
Output low voltage	V _{OL}	LV _{DD} /TV _{DD} = Min, I _{OL} = 4.0 mA	1, 2, 3	GND	0.50	
Input high voltage	V _{IH}		1, 2, 3	2.0	LV _{DD} /TV _{DD} + 0.3	
Input low voltage	V _{IL}		1, 2, 3	-0.3	0.90	
Input high current <u>38/ 39/ 40/</u>	I _{IH}	V _{IN} = LV _{DD} , V _{IN} = TV _{DD}	1, 2, 3		40	µA
Input low current <u>40</u>	I _{IL}	V _{IN} = GND	1, 2, 3	-600		
GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics						
Supply voltage 2.5V <u>38/ 39/</u>	LV _{DD} TV _{DD}		1, 2, 3	2.37	2.63	V
Output high voltage	V _{OH}	LV _{DD} /TV _{DD} = Min, I _{OH} = -1.0 mA	1, 2, 3	2	LV _{DD} /TV _{DD} + 0.3	
Output low voltage	V _{OL}	LV _{DD} /TV _{DD} = Min, I _{OL} = 1.0 mA	1, 2, 3	GND - 0.3	0.40	
Input high voltage	V _{IH}		1, 2, 3	1.70	LV _{DD} /TV _{DD} + 0.3	
Input low voltage	V _{IL}		1, 2, 3	-0.3	0.90	
Input high current <u>38/ 39/ 40/</u>	I _{IH}	V _{IN} = LV _{DD} , V _{IN} = TV _{DD}	1, 2, 3		10	µA
Input low current <u>40</u>	I _{IL}	V _{IN} = GND	1, 2, 3	-15		

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>2/</u>	Group A subgroups	Limits			Unit
				Min	Typ	Max	
ETHERNET: Enhanced three-Speed Ethernet (eTSEC), MII management – Continued.							
FIFO Mode transmit AC Timing specification (see FIGURE 8)							
TX_CLK, GTX_CLK clock period	t _{FIT}		9, 10, 11	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t _{FITH} /t _{FIT}		<u>167/</u>	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}		<u>167/</u>			250	ps
Rise time TX_CLK (20%–80%)	t _{FITR}		<u>167/</u>			0.75	ns
Fall time TX_CLK (80%–20%)	t _{FITF}		<u>167</u>			0.75	
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t _{FITDV}		9, 10, 11	2.0			
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}		9, 10, 11	0.5		3.0	
FIFO Mode Receive AC Timing Specification <u>41/</u> (see FIGURE 9)							
RX_CLK clock period	t _{FIR}		9, 10, 11	5.3	8.0	100	ns
RX_CLK duty cycle	t _{FIRH} /t _{FIR}		<u>167/</u>	45	50	55	%
RX_CLK peak-to-peak jitter	t _{FIRJ}		<u>167/</u>			250	ps
Rise time RX_CLK (20%–80%)	t _{FIRR}		<u>167/</u>			0.75	ns
Fall time RX_CLK (80%–20%)	t _{FIRF}		<u>167</u>			0.75	
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}		9, 10, 11	1.5			
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{FIRDV}		9, 10, 11	0.5			
GMII Transmit AC Timing Specifications <u>42/</u> (see FIGURE 10)							
GMII data TXD[7:0], TX_ER, TX_EN setup time	t _{GTKHDV}		9, 10, 11	2.5			ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}		<u>167/</u>	0.5		5.0	
GTX_CLK data clock rise time (20%–80%) <u>34/</u>	t _{GTXR}		<u>167/</u>			1.0	
GTX_CLK data clock fall time (80%–20%) <u>34/</u>	t _{GTXF}		<u>167</u>			1.0	
GMII Receive AC Timing Specifications <u>42/</u> (see FIGURE 11)							
RX_CLK clock period	t _{GRX}		9, 10, 11		8.0		ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}		<u>167/</u>	35		75	
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}		9, 10, 11	2.0			
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}		9, 10, 11	0			
RX_CLK clock rise (20%–80%) <u>34/</u>	t _{GRXR}		<u>167/</u>			1.0	
RX_CLK clock fall time (80%–20%) <u>34/</u>	t _{GRXF}		<u>167/</u>			1.0	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>2/</u>	Group A subgroups	Limits			Unit
				Min	Typ	Max	
ETHERNET: Enhanced three-Speed Ethernet (eTSEC), MII management – Continued.MII Transmit AC Timing Specifications <u>43/</u> (see FIGURE 12)							
TX_CLK clock period 10 Mbps <u>34/</u>	t _{MTX}		9, 10 ,11		400		ns
TX_CLK clock period 100 Mbps	t _{MTX}		9, 10 ,11		40		
TX_CLK duty cycle	t _{MTXH} /t _{MTX}		<u>167/</u>	35		65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}		9, 10 ,11	1.0	5	15	ns
TX_CLK data clock rise (20%–80%) <u>34/</u>	t _{MTXR}		<u>167/</u>	1.0		4	
TX_CLK data clock fall (80%–20%) <u>34/</u>	t _{MTXF}		<u>167/</u>	1.0		4	
MII Receive AC Timing Specifications <u>44/</u> (see FIGURE 13 and FIGURE 14)							
RX_CLK clock period 10 Mbps <u>34/</u>	t _{MRX}		9, 10 ,11		400		ns
RX_CLK clock period 100 Mbps	t _{MRX}		9, 10 ,11		40		
RX_CLK duty cycle	t _{MRXH} /t _{MRX}		<u>167/</u>	35		65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}		<u>167/</u>	10			ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}		<u>167/</u>	10			
RX_CLK clock rise (20%–80%) <u>34/</u>	t _{MRXR}		<u>167/</u>	1.0		4	
RX_CLK clock fall time (80%–20%) <u>34/</u>	t _{MRXF}		<u>167/</u>	1.0		4	
TBI Transmit AC Timing Specifications <u>45/</u> (see FIGURE 15)							
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}		9, 10 ,11	2.0			ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}		9, 10 ,11	1.0			
GTX_CLK rise (20%–80%) <u>34/</u>	t _{TTXR}		<u>167/</u>			1.0	
GTX_CLK fall time (80%–20%) <u>34/</u>	t _{TTXF}		<u>167/</u>			1.0	
TBI Receive AC Timing Specifications <u>46/</u> (see FIGURE 16)							
TSEC _n RX_CLK[0:1] clock period	t _{TRX}		9, 10 ,11		16.0		ns
TSEC _n RX_CLK[0:1] skew	t _{SKTRX}		<u>167/</u>	7.5		8.5	
TSEC _n RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}		<u>167/</u>	40		60	%
RCG[9:0] setup time to rising TSEC _n RX_CLK	t _{TRDVKH}		9, 10 ,11	2.5			ns
RCG[9:0] hold time to rising TSEC _n RX_CLK	t _{TRDXKH}		9, 10 ,11	1.5			
TSEC _n RX_CLK[0:1] clock rise time (20%–80%) <u>34/</u>	t _{TRXR}		<u>167/</u>	0.7		2.4	
TSEC _n RX_CLK[0:1] clock fall time (80%–20%) <u>34/</u>	t _{TRXF}		<u>167/</u>	0.7		2.4	
TBI single-clock Mode Receive AC Timing Specification (see FIGURE 17)							
RX_CLK clock period	t _{TRRX}		9, 10 ,11	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH} /t _{TRRX}		<u>167/</u>	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}		<u>167/</u>			250	ps
Rise time RX_CLK (20%–80%)	t _{TRRR}		<u>167/</u>			1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}		<u>167/</u>			1.0	
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}		9, 10 ,11	2.0			
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXXH}		9, 10 ,11	1.0			

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
ETHERNET: Enhanced three-Speed Ethernet (eTSEC), MII management – Continued.							
RGMII and RTBI AC Timing Specifications 47/ (see FIGURE 18)							
Data to clock output skew (at transmitter)	t _{SKRGT} 51/		9, 10 ,11	-500 52/	0	500 52/	ps
Data to clock input skew (at receiver) 48/	t _{SKRGT}		167/	1.0	-	2.8	ns
Clock period 49/	t _{RGT} 51/		9, 10 ,11	7.2	8	8.8	
Duty cycle for 10BASE-T and 100BASE-TX 49/ 50/	t _{RGTH} /t _{RGT} 51/		167/	40	50	60	%
Rise time (20%–80%)	t _{RGTR} 51/		167/			0.75	ns
Fall time (20%–80%)	t _{RGTF} 51/		167/			0.75	
RMII Transmit AC Timing Specifications 53/ (see FIGURE 19)							
TSEC _n TX CLK clock period	t _{RMT}		9, 10 ,11	15.0	20.0	25.0	ns
TSEC _n TX CLK duty cycle	t _{RMTH}		167/	35	50	65	%
TSEC _n TX CLK peak-to-peak jitter	t _{RMTJ}		167/			250	ps
Rise time TSEC _n TX CLK (20%–80%)	t _{RMTR}		167/	1.0		2.0	ns
Fall time TSEC _n TX CLK (80%–20%)	t _{RMTF}		167/	1.0		2.0	
TSEC _n TX CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}		9, 10 ,11	1.0		10	
RMII Receive AC Timing Specifications (At Recommended Operating Conditions with LVDD of 3.3V ± 5%) 54/ (see FIGURE 20 and FIGURE 21)							
TSEC _n TX CLK clock period	t _{RMR}		9, 10 ,11	15.0	20.0	25.0	ns
TSEC _n TX CLK duty cycle	t _{RMRH}		167/	35	50	65	%
TSEC _n TX CLK peak-to-peak jitter	t _{RMRJ}		167/			250	ps
Rise time TSEC _n TX CLK (20%–80%)	t _{RMRR}		167/	1.0		2.0	ns
Fall time TSEC _n TX CLK (80%–20%)	t _{RMRF}		167/	1.0		2.0	
RXD[1:0], CRS_DV, RX_ER setup time to TSEC _n TX CLK rising edge	t _{RMRDV}		9, 10 ,11	4.0			
RXD[1:0], CRS_DV, RX_ER hold time to TSEC _n TX CLK rising edge	t _{RMRDX}		9, 10 ,11	2.0			

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
ETHERNET MANAGEMENT INTERFACE ELECTRICAL CHARACTERISTICS							
MII Management DC Electrical Characteristics							
Supply voltage (3.3V)	OV _{DD}		1, 2, 3	3.13		3.47	V
Output high voltage	V _{OH}	OV _{DD} = Min, I _{OH} = -1 mA	1, 2, 3	2.10		OV _{DD} + 0.3	
Output low voltage	V _{OL}	OV _{DD} = Min, I _{OL} = 1 mA	1, 2, 3	GND		0.50	
Input high voltage	V _{IH}		1, 2, 3	2.0			
Input low voltage	V _{IL}		1, 2, 3			0.90	
Input high current	I _{IH}	OV _{DD} = Max, V _{IN} = 2.1 V 55/	1, 2, 3			40	μA
Input low current	I _{IL}	OV _{DD} = Max, V _{IN} = 0.5 V	1, 2, 3	-600			
MII Management AC Timing Specifications (At Recommended Operating Conditions with OVDD is 3.3 V ± 5%) 56/ (see FIGURE 22)							
MDC frequency 51/ 57/ 58/	f _{MDC}		9, 10 ,11	0.72	2.5	8.3	MHz
MDC period	t _{MDC}		9, 10 ,11	120.5		1389	ns
MDC clock pulse width high	t _{MDCH}		167/	32			
MDC to MDIO valid 59/	t _{MDKHdV}		9, 10 ,11	16 × t _{CCB}			
MDC to MDIO delay 59/	t _{MDKHdX}		9, 10 ,11	(16 × t _{CCB} × 8) - 3		(16 × t _{CCB} × 8) + 3	
MDIO to MDC setup time	t _{MDDVKH}		9, 10 ,11	5			
MDIO to MDC hold time	t _{MDDXKH}		9, 10 ,11	0			
MDC rise time 51/	t _{MDCR}		9, 10 ,11			10	
MDC fall time 51/	t _{MDHF}		9, 10 ,11			10	
LOCAL BUS(see FIGURE 23 and FIGURE 24)							
Local Bus DC Electrical Characteristics (3.3 V DC)							
High-level input voltage	V _{IH}		1, 2, 3	2		BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		1, 2, 3	-0.3		0.8	
Input current (V _{IN} 60/ = 0V or V _{IN} = BV _{DD})	I _{IN}	V _{IN} = 0V or V _{IN} = BV _{DD} 60/	1, 2, 3			±5	μA
High-level output voltage	V _{OH}	BV _{DD} = min, I _{OH} = -2 mA	1, 2, 3	BV _{DD} - 0.2			V
Low-level output voltage	V _{OL}	BV _{DD} = min, I _{OL} = 2 mA	1, 2, 3			0.2	
Local Bus DC Electrical Characteristics (2.5 V DC)							
High-level input voltage	V _{IH}		1, 2, 3	1.70		BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		1, 2, 3	-0.3		0.7	
Input current (V _{IN} 60/ = 0V or V _{IN} = BV _{DD})	I _{IH}		1, 2, 3			10	μA
	I _{IL}		1, 2, 3			-15	
High-level output voltage	V _{OH}	BV _{DD} = min, I _{OH} = -1 mA	1, 2, 3	2.0		BV _{DD} + 0.3	V
Low-level output voltage	V _{OL}	BV _{DD} = min, I _{OL} = 1 mA	1, 2, 3	GND - 0.3		0.4	

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
LOCAL BUS – Continued.							
Local Bus General Timing Parameters (BV _{DD} = 3.3 V DC) – PLL Enabled 61/ (see FIGURE 25 to FIGURE 29)							
Local bus cycle time 62/	t _{LBK}		9, 10 ,11	7.5		12	ns
Local bus duty cycle	t _{LBKH} /t _{LBK}		167/	43		57	%
LCLK[n] skew to LCLK[m] or LSYNC_OUT 34/ 67/	t _{LBKSKEW}		167/			150	ps
Input setup to local bus clock (except LGTĀ/LUPWAIT) 63/ 64/	t _{LBIVKH1}		9, 10 ,11	1.8			ns
LGTĀ/LUPWAIT input setup to local bus clock 63/ 64/	t _{LBIVKH2}		9, 10 ,11	1.7			
Input hold from local bus clock (except LGTĀ/LUPWAIT) 63/ 64/	t _{LBIXKH1}		9, 10 ,11	1.0			
LGTĀ/LUPWAIT input hold from local bus clock 63/ 64/	t _{LBIXKH2}		9, 10 ,11	1.0			
LALE output transition to LAD/LDP output transition (LATCH hold time) 66/	t _{LBOTOT}		9, 10 ,11	1.5			
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}		9, 10 ,11			2.0	
Local bus clock to data valid for LAD/LDP 63/	t _{LBKHOV2}		9, 10 ,11			2.2	
Local bus clock to address valid for LAD 63/	t _{LBKHOV3}		9, 10 ,11			2.3	
Local bus clock to LALE assertion 63/	t _{LBKHOV4}		9, 10 ,11			2.3	
Output hold from local bus clock (except LAD/LDP and LALE) 63/	t _{LBKHOX1}		9, 10 ,11	0.7			
Output hold from local bus clock for LAD/LDP 63/	t _{LBKHOX2}		9, 10 ,11	0.7			
Local bus clock to output high Impedance (except LAD/LDP and LALE) 65/	t _{LBKHOZ1}		9, 10 ,11			2.5	
Local bus clock to output high impedance for LAD/LDP 65/	t _{LBKHOZ2}		9, 10 ,11			2.5	

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
LOCAL BUS – Continued.							
Local Bus Timing Parameters (BV _{DD} = 2.5 V) - PLL Enabled 61/ (see FIGURE 23 to FIGURE 29)							
Local bus cycle time 62/	t _{LBK}		9, 10 ,11	7.5		12	ns
Local bus duty cycle	t _{LBKH} /t _{LBK}		167/	43		57	%
LCLK[n] skew to LCLK[m] or LSYNC_OUT 34/ 67/	t _{LBKSKEW}		167/			150	ps
Input setup to local bus clock (except LGTA/LUPWAIT) 63/ 64/	t _{LBIVKH1}		9, 10 ,11	1.9			ns
LGTA/LUPWAIT input setup to local bus clock 63/ 64/	t _{LBIVKH2}		9, 10 ,11	1.8			
Input hold from local bus clock (except LGTA/LUPWAIT) 63/ 64/	t _{LBIXKH1}		9, 10 ,11	1.1			
LGTA/LUPWAIT input hold from local bus clock 63/ 64/	t _{LBIXKH2}		9, 10 ,11	1.1			
LALE output transition to LAD/LDP output transition (LATCH hold time) 68/	t _{LBOTOT}		9, 10 ,11	1.5			
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}		9, 10 ,11			2.1	
Local bus clock to data valid for LAD/LDP 63/	t _{LBKHOV2}		9, 10 ,11			2.3	
Local bus clock to address valid for LAD 63/	t _{LBKHOV3}		9, 10 ,11			2.4	
Local bus clock to LALE assertion 63/	t _{LBKHOV4}		9, 10 ,11			2.4	
Output hold from local bus clock (except LAD/LDP and LALE) 63/	t _{LBKH0X1}		9, 10 ,11	0.8			
Output hold from local bus clock for LAD/LDP 63/	t _{LBKH0X2}		9, 10 ,11	0.8			
Local bus clock to output high Impedance (except LAD/LDP and LALE) 65/	t _{LBKHOZ1}		9, 10 ,11			2.6	
Local bus clock to output high impedance for LAD/LDP 65/	t _{LBKHOZ2}		9, 10 ,11			2.6	

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
LOCAL BUS – Continued.							
Local Bus Timing Parameters: PLL Bypassed 61/ (see FIGURE 23 to FIGURE 29)							
Local bus cycle time 68/	t _{LBK}		9, 10 ,11	12			ns
Local bus duty cycle	t _{LBKH} /t _{LBK}		167/	43		57	%
Internal launch/capture clock to LCLK delay 51/	t _{LBKHK} T		9, 10 ,11	2.3		4.4	ns
Input setup to local bus clock (except LGTA/LUPWAIT) 70/ 71/	t _{LBIVKH} 1		9, 10 ,11	6.2		4.4	
LGTA/LUPWAIT input setup to local bus clock 70/ 71/	t _{LBIVKL} 2		9, 10 ,11	6.1			
Input hold from local bus clock (except LGTA/LUPWAIT) 70/ 71/	t _{LBIXKH} 1		9, 10 ,11	-1.8			
LGTA/LUPWAIT input hold from local bus clock 70/ 71/	t _{LBIXKL} 2		9, 10 ,11	-1.3			
LAL output transition to LAD/LDP output transition (LATCH hold time) 72/	t _{LBOTOT}		9, 10 ,11	1.5			
Local bus clock to output valid (except LAD/LDP and LAL)	t _{LBKHOV} 1		9, 10 ,11			-0.3	
Local bus clock to data valid for LAD/LDP 70/	t _{LBKHOV} 2		9, 10 ,11			-0.1	
Local bus clock to address valid for LAD 70/	t _{LBKHOV} 3		9, 10 ,11			0	
Output hold from local bus clock (except LAD/LDP and LAL) 70/	t _{LBKHOX} 1		9, 10 ,11	-3.7			
Output hold from local bus clock for LAD/LDP 70/	t _{LBKHOX} 2		9, 10 ,11	-3.7			
Local bus clock to output high Impedance (except LAD/LDP and LAL) 73/	t _{LBKHOZ} 1		9, 10 ,11			0.2	
Local bus clock to output high impedance for LAD/LDP 73/	t _{LBKHOZ} 2		9, 10 ,11			0.2	

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits		Unit
				Min	Max	
JTAG (See FIGURE 30)						
JTAG DC Electrical Characteristics						
High-level input voltage	V _{IH}		1, 2, 3	2.0	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		1, 2, 3	-0.3	0.8	V
Input current	I _{IN}	V _{IN} = 0 V or V _{IN} = V _{DD} 74/	1, 2, 3		±5	µA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = -2 mA	1, 2, 3	2.4		V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 2 mA	1, 2, 3		0.4	V
JTAG AC Timing Specifications (Independent of SYSCLK) 75/ 76/ (See FIGURE 31 to FIGURE 33)						
JTAG external clock frequency of operation	f _{JTG}		9, 10 ,11	0	33.3	MHz

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TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Test conditions 2/	Group A subgroups	Limits		Unit
					Min	Max	
I ² C (See FIGURE 34 to FIGURE 35)							
I ² C DC Electrical Characteristics (At Recommended Operating Conditions with OV _{DD} of 3.3V ± 5%)							
Input high voltage level		V _{IH}		1, 2, 3	0.7 × OV _{DD}	OV _{DD} + 0.3	V
Input low voltage level		V _{IL}		1, 2, 3	-0.3	0.3 × OV _{DD}	
Low level output voltage 80/		V _{OL}		1, 2, 3	0	0.2 × OV _{DD}	
Pulse width of spikes which must be suppressed by the input filter 81/		t _{I2KHKL}		1, 2, 3	0	50	ns
Input current each I/O pin (input voltage is between 0.1 × OV _{DD} and 0.9 × OV _{DD} (max) 82/		I _I		1, 2, 3	-10	10	µA
Capacitance for each I/O pin		C _I		167/		10	pF
I ² C AC Electrical Specifications (All Values Refer to V _{IH} (min) and V _{IL} (max) Levels, see I ² C DC Electrical Characteristics table) 83/ 167/							
SCL clock frequency		f _{I2C}		9, 10, 11	0	400	kHz
Low period of the SCL clock		t _{I2CL} 34/		9, 10, 11	1.3		µs
High period of the SCL clock		t _{I2CH} 34/		9, 10, 11	0.6		
Setup time for a repeated START condition		t _{I2SVKH} 34/		9, 10, 11	0.6		
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		t _{I2SXKL} 34/		9, 10, 11	0.6		
Data setup time		t _{I2DVKH} 34/		9, 10, 11	100		ns
Data hold time:	CBUS compatible masters 86/	t _{I2DXKL}		9, 10, 11			µs
	I ² C bus devices			9, 10, 11	0 84/	0.9 85/	
Set-up time for STOP condition		t _{I2PVKH}		9, 10, 11	0.6		
Bus free time between a STOP and START condition		t _{I2KHDX}		9, 10, 11	1.3		
Noise margin at the LOW level for each connected device (including hysteresis)		V _{NL}		9, 10, 11	0.1 × OV _{DD}		V
Noise margin at the HIGH level for each connected device (including hysteresis)		V _{NH}		9, 10, 11	0.2 × OV _{DD}		

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions <u>2/</u>	Group A subgroups	Limits		Unit
				Min	Max	
GP _{OUT} /GP _{IN}						
GP _{OUT} DC Electrical Characteristics (3.3 V DC)						
Supply voltage 3.3 V	BV _{DD}		1, 2, 3	3.13	3.47	V
High-level output voltage	V _{OH}	BV _{DD} = min, I _{OH} = -2 mA	1, 2, 3	BV _{DD} -0.2		
Low-level output voltage	V _{OL}	BV _{DD} = min, I _{OL} = 2.mA	1, 2, 3		0.2	
GP _{OUT} DC Electrical Characteristics (2.5 V DC)						
Supply voltage 2.5 V	BV _{DD}		1, 2, 3	2.37	2.63	V
High-level output voltage	V _{OH}	BV _{DD} = min, I _{OH} = -1 mA	1, 2, 3	2.0	BV _{DD} + 0.3	
Low-level output voltage	V _{OL}	BV _{DD} = min, I _{OL} = 1mA	1, 2, 3	GND - 0.3	0.4	
GP _{IN} DC Electrical Characteristics (3.3 V DC)						
Supply voltage 3.3 V	BV _{DD}		1, 2, 3	3.13	3.47	V
High-level input voltage	V _{IH}		1, 2, 3	2	BV _{DD} + 0.3	
Low-level input voltage	V _{IL}		1, 2, 3	-0.3	0.8	
Input current	I _{IN}	BV _{IN} = 0V or BV _{IN} = BV _{DD} 87/	1, 2, 3		±5	µA
GP _{IN} DC Electrical Characteristics (2.5 V DC)						
Supply voltage 2.5 V	BV _{DD}		1, 2, 3	2.37	2.63	V
High-level input voltage	V _{IH}		1, 2, 3	1.70	BV _{DD} + 0.3	
Low-level input voltage	V _{IL}		1, 2, 3	-0.3	0.7	
Input current	I _{IN}	BV _{IN} = 0V or BV _{IN} = BV _{DD} 87/	1, 2, 3		10	µA

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/	Group A subgroups	Limits		Unit
				Min	Max	
PCI/PCI-X (See FIGURE 36 to FIGURE 38)						
PCI/PCI-X DC Electrical Characteristics 88/						
High-level input voltage	V _{IH}		1, 2, 3	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}		1, 2, 3	-0.3	0.8	
Input current	I _{IN}	V _{IN} = 0V or V _{IN} = V _{DD} 89/	1, 2, 3		±5	μA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = −100 μA	1, 2, 3	OV _{DD} - 0.2		V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 100 μA	1, 2, 3		0.2	
PCI AC Timing Specifications at 66 MHz 90/						
SYSCLK to output valid 91/ 92/	t _{PCKHOV}		9, 10 ,11		6	ns
Output hold from SYSCLK 51/ 91/	t _{PCKHOX}		9, 10 ,11	2		
SYSCLK to output high impedance 91/ 93/ 34/	t _{PCKHOZ}		9, 10 ,11		14	
Input setup to SYSCLK 51/ 91/ 94/	t _{PCIVKH}		9, 10 ,11	3		
Input hold from SYSCLK 51/ 91/ 94/	t _{PCIXKH}		9, 10 ,11	0		
REQ64 to HRESET setup time 34/ 95/ 96/ 98/	t _{PCRVRH}		9, 10 ,11	10 x t _{sys}		clocks
HRESET to REQ64 hold time 34/ 96/	t _{PCRHRX}		9, 10 ,11	0	50	ns
HRESET high to first FRAME assertion 34/ 97/	t _{PCRHFV}		9, 10 ,11	10		clocks
PCI-X AC Timing Specifications at 66 MHz						
SYSCLK to signal valid delay 99/ 100/ 101/ 105/ 106/	t _{PCKHOV}		9, 10 ,11		3.8	ns
Output hold from SYSCLK 51/ 99/	t _{PCKHOX}		9, 10 ,11	0.7		
SYSCLK to output high impedance 34/ 99/ 102/ 106/	t _{PCKHOZ}		9, 10 ,11		7	
Input setup time to SYSCLK 101/ 103/	t _{PCIVKH}		9, 10 ,11	1.7		
Input hold time from SYSCLK 51/	t _{PCIXKH}		9, 10 ,11	0.5		
REQ64 to HRESET setup time 34/	t _{PCRVRH}		9, 10 ,11	10		clocks
HRESET to REQ64 hold time 34/	t _{PCRHRX}		9, 10 ,11	0	50	ns
HRESET high to first FRAME assertion 34/ 107/	t _{PCRHFV}		9, 10 ,11	10		clocks
PCI-X initialization pattern to HRESET setup time 34/	t _{PCIVRH}		9, 10 ,11	10		clocks
HRESET to PCI-X initialization pattern hold time 34/ 104/	t _{PCRHIX}		9, 10 ,11	0	50	ns

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/	Group A subgroups	Limits		Unit
				Min	Max	
PCI/PCI-X - Continued (See FIGURE 36 to FIGURE 38)PCI-X AC Timing Specifications at 133 MHz 82/						
SYSCLK to signal valid delay 99/ 100/ 101/ 105/ 106/	tPCKHOV		9, 10 ,11		3.8	ns
Output hold from SYSCLK 51/ 99/	tPCKHOX		9, 10 ,11	0.7		
SYSCLK to output high impedance 34/ 99/ 102/ 106/	tPCKHOZ		9, 10 ,11		7	
Input setup time to SYSCLK 51/ 101/ 103/ 108/	tPCIVKH		9, 10 ,11	1.2		
Input hold time from SYSCLK 51/	tPCIXKH		9, 10 ,11	0.5		
REQ64 to HRESET setup time 34/	tPCRVRH		9, 10 ,11	10		clocks
HRESET to REQ64 hold time 34/	tPCRHRX		9, 10 ,11	0	50	ns
HRESET high to first FRAME assertion 34/ 107/	tPCRHFV		9, 10 ,11	10		clocks
PCI-X initialization pattern to HRESET setup time 34/	tPCIVRH		9, 10 ,11	10		clocks
HRESET to PCI-X initialization pattern hold time 34/ 104/	tPCRHIX		9, 10 ,11	0	50	ns

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
PCI EXPRESS							
AC Requirements for PCI Express SerDes Clocks							
SD_REF_CLK and SD_REF_CLK AC Requirements							
REFCLK cycle time 109/	tREF		9, 10 ,11		10		ns
REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	tREFCJ		167/			100	ps
Phase jitter. Deviation edge location in edge location with respect to mean	tREFPJ		167/	-50		50	ps
Physical Layer Specifications 168/							
Differential Transmitter (TX) Output Specifications							
Unit Interval	UI	110/ 111/	9, 10 ,11	399.98	400	400.12	ps
Differential Peak-to-Peak Output Voltage	V _{TX-DIFFp-p}	112/ 113/	9, 10 ,11	0.8		1.2	V
De- Emphasized Differential Output Voltage (Ratio)	V _{TX-DE-RATIO}	114/ 113/	9, 10 ,11	-3.0	-3.5	-4.0	dB
Minimum TX Eye Width	T _{TX-EYE}	115/ 113/ 116/	9, 10 ,11	0.70			UI
Maximum time between the jitter median and maximum deviation from the median	T _{TX-EYE-MEDIAN-to- MAX-JITTER}	117/ 113/ 116/	9, 10 ,11			0.15	
D+/D- TX Output Rise/Fall Time	T _{TX-RISE, TTX-FALL}	113/ 119/	9, 10 ,11	0.125			
RMS AC Peak Common Mode Output Voltage	V _{TX-CM-ACp}	123/ 113/	9, 10 ,11			20	mV
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	V _{TX-CM-DC- ACTIVEIDLE- DELTA}	124/ 113/	9, 10 ,11	0		100	
Absolute Delta of DC Common Mode between D+ and D–	V _{TX-CM-DC- LINEDELTA}	125/ 113/	9, 10 ,11	0		25	
Electrical Idle differential Peak Output Voltage	V _{TX-IDLE-DIFFp}	126/ 113/	9, 10 ,11	0		20	
The amount of voltage change allowed during Receiver Detection 109/	V _{TX-RCV-DETECT}	127/ 120/	9, 10 ,11			600	
The TX DC Common Mode Voltage	V _{TX-DC-CM}	128/ 120/	9, 10 ,11	0		3.6	V
TX Short Circuit Current Limit	I _{TX-SHORT}	129/	9, 10 ,11			90	mA
Minimum time spent in Electrical Idle	T _{TX-IDLE-MIN}	130/	9, 10 ,11	50			UI
Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	T _{TX-IDLE-SET- TOIDLE}	131/	9, 10 ,11			20	
Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	T _{TX-IDLE-TO- DIFFDATA}	132/	9, 10 ,11			20	

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
PCI EXPRESS - Continued							
Physical Layer Specifications - Continued							
Differential Transmitter (TX) Output Specifications - Cotinued							
Differential Return Loss	R _{LTX-DIFF}	133/ 118/	1, 2, 3	12			UI
Common Mode Return Loss	R _{LTX-CM}	133/ 118/	1, 2, 3	6			
DC Differential TX Impedance	Z _{TX-DIFF-DC}	134/	1, 2, 3	80	100	120	Ω
Transmitter DC Impedance	Z _{TX-DC}	135/	1, 2, 3	40			
Lane-to-Lane Output Skew	L _{TX-SKEW}	136/	1, 2, 3			50 + 2 UI	ps
AC Coupling Capacitor	C _{TX}	137/ 122/	1, 2, 3	75		200	nF
Crosslink Random Timeout	T _{crosslink}	138/ 121/	1, 2, 3	0		1	ms
Differential Receiver (RX) Input Specifications							
Unit Interval	UI	139/ 140/	1, 2, 3	399.98	400	400.12	ps
Differential Peak-to-Peak Output Voltage	V _{RX-DIFFp-p}	141/ 142/	1, 2, 3	0.175		1.200	V
Minimum Receiver Eye Width	T _{RX-EYE}	143/ 142/ 144/	1, 2, 3	0.4			UI
Maximum time between the jitter median and maximum deviation from the median	T _{RX-EYE-MEDIAN-to- MAX-JITTER}	145/ 142/ 144/ 155/	1, 2, 3			0.3	
AC Peak Common Mode Input Voltage	V _{RX-CM-ACp}	146/ 142/	1, 2, 3			150	mV
Differential Return Loss	R _{LRX-DIFF}	147/ 148/	1, 2, 3	15			dB
Common Mode Return Loss	R _{LRX-CM}	149/ 148/	1, 2, 3	6			
DC Differential Input Impedance	Z _{RX-DIFF-DC}	150/ 151/	1, 2, 3	80	100	120	Ω
DC Input Impedance	Z _{RX-DC}	152/ 151/ 142/	1, 2, 3	40	50	60	
Powered Down DC Input Impedance	Z _{RX-HIGH-IMP-DC}	153/ 154/	1, 2, 3	200 k			
Electrical Idle Detect Threshold	V _{RX-IDLE-DET-DIFFp-p}	156/	1, 2, 3	65		175	mV
Unexpected Electrical Idle Enter Detect Threshold Integration Time	T _{RX-IDLE-DET-DIFF- ENTERTIME}	157/	1, 2, 3			10	ms
Total	L _{TX-SKEW}	158/	1, 2, 3	Skew		20	ns

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
SERIAL RAPIDIO 168/							
SDn_REF_CLK and SDn_REF_CLK AC Requirements 103/							
REFCLK cycle time	tREF	159/	9, 10, 11		10 (8)		ns
REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	tREFCJ		9, 10, 11			80	ps
Phase jitter. Deviation in edge location with respect to mean edge location	tREFPJ		9, 10, 11	-40		40	
Short Run Transmitter AC Timing Specifications: 1.25 GBaud							
Output Voltage	VO	160/	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	VDIFFPP		9, 10, 11	500		1000	mV p-p
Deterministic Jitter	JD		9, 10, 11			0.17	UI p-p
Total Jitter	JT		9, 10, 11			0.35	
Multiple output skew	SMO	161/	9, 10, 11			1000	ps
Unit Interval	UI	162/	9, 10, 11	800		800	
Short Run Transmitter AC Timing Specifications: 2.5 GBaud							
Output Voltage	VO	160/	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	VDIFFPP		9, 10, 11	500		1000	mV p-p
Deterministic Jitter	JD		9, 10, 11			0.17	UI p-p
Total Jitter	JT		9, 10, 11			0.35	
Multiple output skew	SMO	161/	9, 10, 11			1000	ps
Unit Interval	UI	162/	9, 10, 11	400		400	
Short Run Transmitter AC Timing Specifications: 3.125 GBaud							
Output Voltage	VO	160/	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	VDIFFPP		9, 10, 11	500		1000	mV p-p
Deterministic Jitter	JD		9, 10, 11			0.17	UI p-p
Total Jitter	JT		9, 10, 11			0.35	
Multiple output skew	SMO	161/	9, 10, 11			1000	ps
Unit Interval	UI	162/	9, 10, 11	320		320	
Long Run Transmitter AC Timing Specifications: 1.25 GBaud							
Output Voltage	VO	160/	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	VDIFFPP		9, 10, 11	800		1600	mV p-p
Deterministic Jitter	JD		9, 10, 11			0.17	UI p-p
Total Jitter	JT		9, 10, 11			0.35	
Multiple output skew	SMO	161/	9, 10, 11			1000	ps
Unit Interval	UI	162/	9, 10, 11	800		800	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>2/</u>	Group A subgroups	Limits			Unit
				Min	Typ	Max	

SERIAL RAPIDIO - Continued**Long Run Transmitter AC Timing Specifications: 2.5 GBaud**

Output Voltage	V _O	<u>160/</u>	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	V _{DIFFPP}		9, 10, 11	800		1600	mV p-p
Deterministic Jitter	J _D		9, 10, 11			0.17	UI p-p
Total Jitter	J _T		9, 10, 11			0.35	
Multiple output skew	S _{MO}	<u>161/</u>	9, 10, 11			1000	ps
Unit Interval	UI	<u>162/</u>	9, 10, 11	400		400	

Long Run Transmitter AC Timing Specifications: 3.125 GBaud

Output Voltage	V _O	<u>160/</u>	9, 10, 11	-0.40		2.30	V
Differential Output Voltage	V _{DIFFPP}		9, 10, 11	800		1600	mV p-p
Deterministic Jitter	J _D		9, 10, 11			0.17	UI p-p
Total Jitter	J _T		9, 10, 11			0.35	
Multiple output skew	S _{MO}	<u>161/</u>	9, 10, 11			1000	ps
Unit Interval	UI	<u>162/</u>	9, 10, 11	320		320	

Transmitter Differential Output Eye Diagram Parameters (see FIGURE 34)

Transmitter Type			V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range			250	500	0.175	0.39
1.25 GBaud long range			400	800	0.175	0.39
2.5 GBaud short range			250	500	0.175	0.39
2.5 GBaud long range			400	800	0.175	0.39
3.125 GBaud short range			250	500	0.175	0.39
3.125 GBaud long range			400	800	0.175	0.39

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Group A subgroups	Limits			Unit
				Min	Typ	Max	
SERIAL RAPIDIO - Continued							
Receiver AC Timing Specifications: 1.25 GBaud							
Differential Input Voltage	V _{IN}	164/	9, 10 ,11	200		1600	mV p-p
Deterministic Jitter Tolerance	J _D	164/	9, 10 ,11	0.37			UI p-p
Combined Deterministic and Random Jitter Tolerance	J _{DR}	164/	9, 10 ,11	0.55			
Total Jitter Tolerance 165/	J _T	164/	9, 10 ,11	0.65			
Multiple Input Skew	S _{MI}	166/	9, 10 ,11			24	ns
Bit Error Rate	BER		9, 10 ,11			10 ⁻¹²	
Unit Interval	UI	162/	9, 10 ,11	800		800	ps
Receiver AC Timing Specifications: 2.5 GBaud							
Differential Input Voltage	V _{IN}	164/	9, 10 ,11	200		1600	mV p-p
Deterministic Jitter Tolerance	J _D	164/	9, 10 ,11	0.37			UI p-p
Combined Deterministic and Random Jitter Tolerance	J _{DR}	164/	9, 10 ,11	0.55			
Total Jitter Tolerance 165/	J _T	164/	9, 10 ,11	0.65			
Multiple Input Skew	S _{MI}	166/	9, 10 ,11			24	ns
Bit Error Rate	BER		9, 10 ,11			10 ⁻¹²	
Unit Interval	UI	162/	9, 10 ,11	400		400	ps
Receiver AC Timing Specifications: 3.125 GBaud							
Differential Input Voltage	V _{IN}	164/	9, 10 ,11	200		1600	mV p-p
Deterministic Jitter Tolerance	J _D	164/	9, 10 ,11	0.37			UI p-p
Combined Deterministic and Random Jitter Tolerance	J _{DR}	164/	9, 10 ,11	0.55			
Total Jitter Tolerance 165//	J _T	164/	9, 10 ,11	0.65			
Multiple Input Skew	S _{MI}	166/	9, 10 ,11			22	ns
Bit Error Rate	BER		9, 10 ,11			10 ⁻¹²	
Unit Interval	UI	162/	9, 10 ,11	320		320	ps

Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type			V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud			100	800	0.275	0.4
2.5 GBaud			100	800	0.275	0.4
3.125 GBaud			100	800	0.275	0.4

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ At Recommended Operating Conditions with $OV_{DD} = 3.3V \pm 165 \text{ mV}$
- 2/ Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum operating frequencies. Refer to manufacturer data on "CCB/SYSCLK PLL Ratio" and "e500 Core PLL Ratio", for ratio settings.
- 3/ This parameter has been adjusted slower according to the workaround for device erratum GEN-13.
- 4/ For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 5/ System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.
- 6/ Rise and fall times for SYSCLK are measured at 0.6V and 2.7V.
- 7/ Timing is guaranteed by design and characterization.
- 8/ This represents the total input jitter – short term and long term – and is guaranteed by design.
- 9/ The SYSCLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 10/ Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for $L/TVDD = 2.5V$, and from 0.6 and 2.7V for $L/TVDD = 3.3V$.
- 11/ EC_GTX_CLK125 is used to generate the GTX clock $TSECn_GTX_CLK$ for the eTSEC transmitter with 2% degradation EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the $TSECn_GTX_CLK$. See manufacturer data sheet for "RGMII and RTBI AC Timing Specifications" for duty cycle for 10Base-T and 100Base-T reference clock.
- 12/ Rise and fall times for SYSCLK are measured at 0.6V and 2.7V.
- 13/ SYSCLK is identical to the PCI_CLK signal and is the primary clock input for this device.
- 14/ Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.
- 15/ V_{DD} itself is not vulnerable to false ESD triggering; however, as per manufacturer data sheet on "PLL Power Supply Filtering" the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.
- 16/ $GV_{DD}(typ) = 2.5V$ for DDR SDRAM, and $GV_{DD}(typ) = 1.8V$ for DDR2 SDRAM.
- 17/ GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- 18/ MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- 19/ V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- 20/ Output leakage is measured with all outputs disabled, $0V \leq V_{OUT} \leq GV_{DD}$.
- 21/ This parameter is sampled. $GV_{DD} = 1.8V \pm 0.090V$, $f = 1 \text{ MHz}$, $T_A = 25^\circ C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to peak) = 0.2V.
- 22/ MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- 23/ This parameter is sampled. $GV_{DD} = 2.5V \pm 0.125 V$, $f = 1 \text{ MHz}$, $T_A = 25^\circ C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2V.
- 24/ The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.
- 25/ t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
- 26/ The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

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TABLE I. Electrical performance characteristics - Continued.

- 27/ The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- 28/ All $\text{MCK}/\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals $\pm 0.1\text{V}$.
- 29/ ADDR/CMD includes all DDR SDRAM output signals except $\text{MCK}/\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
- 30/ Note that t_{DDKMHM} follows the symbol conventions described in note 27/. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the $\text{MCK}[n]$ clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in $\text{DDR_SDRAM_CLK_CNTL}[\text{CLK_ADJUST}]$. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the PC8548E Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- 31/ Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC(MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 32/ All outputs are referenced to the rising edge of $\text{MCK}[n]$ at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 27/.
- 33/ Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol see manufacturer for more info.
- 34/ Guaranteed by design.
- 35/ f_{CCB} refers to the internal platform clock.
- 36/ Actual attainable baud rate will be limited by the latency of interrupt processing.
- 37/ The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
- 38/ LV_{DD} supports eTSECs 1 and 2.
- 39/ TV_{DD} supports eTSECs 3 and 4.
- 40/ The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in manufacturer data.
- 41/ The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. Refer to manufacturer data "Platform to FIFO restriction".
- 42/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 43/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDV} symbolizes MII transmit timing (MT) with respect to the t_{MTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the invalid state (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

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TABLE I. Electrical performance characteristics - Continued.

- 44/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 45/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 46/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- 47/ Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 48/ This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 49/ For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- 50/ Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 51/ Guaranteed by characterization.
- 52/ In rev 1.0 silicon, due to errata, t_{SKRGT} is –650 ps (Min) and 650 ps (Max). Please refer to “eTSEC 10” in the device errata document.
- 53/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDV} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 54/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 55/ Note that the symbol VIN, in this case, represents the OVIN symbol referenced in section 1.3 and section 1.4 herein.

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TABLE I. Electrical performance characteristics - Continued.

- 56/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 57/ This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of PC8548E's MIICFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533/(2*4*8) = 533/64 = 8.3$ MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. Refer to MPC8572E reference manual's MIICFG register section for more detail.
- 58/ The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for PC8548E (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for PC8548E (333 MHz) divided by 448, following the formula described in Note 57/ above.
- 59/ t_{CCB} is the platform (CCB) clock period.
- 60/ Note that the symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in manufacturer data.
- 61/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 62/ All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 63/ All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 BV_{DD}$ of the signal in question for 3.3 V signaling levels.
- 64/ Input timings are measured at the pin.
- 65/ For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 66/ t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 67/ Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
- 68/ All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which preceeds LCLK by t_{LBKHKT} .
- 69/ Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
- 70/ All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3V signaling levels.
- 71/ Input timings are measured at the pin.
- 72/ The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
- 73/ For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 74/ The symbol V_{IN} , in this case, represents the OV_{IN} .
- 75/ All outputs are measured from the midpoint voltage of the falling/rising edge of t_{CLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 30). Timeof-flight delays must be added for trace lengths, vias, and connectors in the system.

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TABLE I. Electrical performance characteristics - Continued.

- 76/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{\text{JTDV KH}}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, $t_{\text{JTDX KH}}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 77/ $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 78/ Non-JTAG signal input timing with respect to t_{CLK} .
- 79/ Non-JTAG signal output timing with respect to t_{CLK} .
- 80/ Output voltage (open drain or open collector) condition = 3 mA sink current.
- 81/ Refer to the PC8548E PowerQUICC III Integrated Host Processor Reference Manual for information on the digital filter used.
- 82/ I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.
- 83/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{\text{I2DV KH}}$ symbolizes I²C timing (I²) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, $t_{\text{I2SX KL}}$ symbolizes I²C timing (I²) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, $t_{\text{I2PV KH}}$ symbolizes I²C timing (I²) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 84/ PC8548E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL. As a transmitter, the PC8548E provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When PC8548E acts as the I²C bus master while transmitting, PC8548E drives both SCL and SDA. As long as the load on SCL and SDA are balanced, PC8548E would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for PC8548E as transmitter, the following setting is recommended for the FDR bit field of the I²CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 KHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I ² C Source Clock Frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR Bit Setting	0x2A	0x05	0x26	0x00
Actual FDR Divider Selected	896	704	512	384
Actual I ² C SCL Frequency Generated	371 KHz	378 KHz	390 KHz	346 KHz

For the detail of I²C frequency calculation, refer to the application note AN2919 "Determining the I²C Frequency Divider Ratio for SCL". Note that the I²C Source Clock Frequency is half of the CCB clock frequency for PC8548E.

- 85/ The maximum $t_{\text{I2DV KH}}$ has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 86/ C_{B} = capacitance of one bus line in pF.
- 87/ The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced manufacturer data Table 1.
- 88/ Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications in manufacturer data.
- 89/ Note that the symbol VIN , in this case, represents the OVIN symbol referenced in Table 2-1 and Table 2-2 in manufacturer data.

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TABLE I. Electrical performance characteristics - Continued. 1/

- 90/ The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 91/ See the timing measurement conditions in the PCI 2.2 Local Bus Specifications in the manufacturer data sheet.
- 92/ All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels
- 93/ For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 94/ Input timings are measured at the pin.
- 95/ The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 20. "Clocking" on page 94 of the manufacturer data sheet.
- 96/ The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
- 97/ The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI 2.2 Local Bus Specifications.
- 98/ The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs .
- 99/ See the timing measurement conditions in the PCI-X 1.0a Specification from manufacturer data sheet.
- 100/ Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 101/ Setup time for point-to-point signals applies to $\overline{\text{REQ}}$ and $\overline{\text{GNT}}$ only. All other signals are bused.
- 102/ For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 103/ Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 104/ Maximum value is also limited by delay to the first transaction (time for $\overline{\text{HRESET}}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{\text{HRESET}}$ must be negated no later than two clocks before the first $\overline{\text{FRAME}}$ and must be floated no later than one clock before $\overline{\text{FRAME}}$ is asserted.
- 105/ A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 106/ Device must meet this specification independent of how many outputs switch simultaneously.
- 107/ The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI-X 1.0a Specification from manufacturer data sheet.
- 108/ The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the PCI-X 1.0a Specification from manufacturer data sheet.
- 109/ Typical based on PCI Express Specification 2.0 in the manufacturer data sheet.
- 110/ Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations.
- 111/ No test load is necessarily associated with this value.
- 112/ $V_{\text{TX-DIFFP-P}} = 2 \times |V_{\text{TX-D+}} - V_{\text{TX-D-}}|$.
- 113/ Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 49).
- 114/ Ratio of the $V_{\text{TX-DIFFP-P}}$ of the second and following bits after a transition divided by the $V_{\text{TX-DIFFP-P}}$ of the first bit after a transition.
- 115/ The maximum Transmitter jitter can be derived as $T_{\text{TXMAX-JITTER}} = 1 - T_{\text{TX-EYE}} = 0.3 \text{ UI}$.
- 116/ A $T_{\text{TX-EYE}} = 0.70 \text{ UI}$ provides for a total sum of deterministic and random jitter budget of $T_{\text{TX-JITTER-MAX}} = 0.30 \text{ UI}$ for the Transmitter collected over any 250 consecutive TX UIs. The $T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

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TABLE I. Electrical performance characteristics - Continued. 1/

- 117/ Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.
- 118/ The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes; see Figure 51). Note that the series capacitors CTX is optional for the return loss measurement.
- 119/ Measured between 20–80% at transmitter package pins into a test load as shown in Figure 51 for both V_{TX-D+} and V_{TX-D-} .
- 120/ See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a from manufacturer data sheet.
- 121/ See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a from manufacturer data sheet.
- 122/ PC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.
- 123/ $V_{TX-CM-ACp} = \text{RMS}(|V_{TXD+} + V_{TXD-}|/2 - V_{TX-CM-DC})$
 $V_{TX-CM-DC} = \text{DC}_{(avg)} \text{ of } |V_{TX-D+} + V_{TX-D-}|/2$.
- 124/ $|V_{TX-CM-DC} \text{ (during L0)} + V_{TX-CM-Idle-DC} \text{ (during electrical idle)}| \leq 100 \text{ mV}$
 $V_{TX-CM-DC} = \text{DC}_{(avg)} \text{ of } |V_{TX-D+} + V_{TX-D-}|/2 \text{ [L0]}$
 $V_{TX-CM-Idle-DC} = \text{DC}_{(avg)} \text{ of } |V_{TX-D+} + V_{TX-D-}|/2 \text{ [electrical idle]}$
- 125/ $|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}| \leq 25 \text{ mV}$
 $V_{TX-CM-DC-D+} = \text{DC}_{(avg)} \text{ of } |V_{TX-D+}|$
 $V_{TX-CM-DC-D-} = \text{DC}_{(avg)} \text{ of } |V_{TX-D-}|$.
- 126/ $V_{TX-IDLE-DIFFp} = |V_{TX-IDLE-D+} - V_{TX-IDLE-D-}| \leq 20 \text{ mV}$.
- 127/ The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present.
- 128/ The allowed DC Common Mode voltage under any conditions.
- 129/ The total current the Transmitter can provide when shorted to its ground
- 130/ Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set.
- 131/ After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
- 132/ Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle.
- 133/ Measured over 50 MHz to 1.25 GHz.
- 134/ TX DC Differential mode Low Impedance.
- 135/ Required TX D+ as wellall states.
- 136/ Static skew between any two Transmitter Lanes within a single Link.
- 137/ All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
- 138/ This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.
- 139/ Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations.
- 140/ No test load is necessarily associated with this value.
- 141/ $V_{RX-DIFFp-p} = 2 * |V_{RX-D+} - V_{RX-D-}|$.
- 142/ Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 50). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

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TABLE I. Electrical performance characteristics - Continued. 1/

- 143/ The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.
- 144/ A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 145/ Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.
- 146/ $V_{RX-CM-ACp} = |V_{RXD+} - V_{RXD-}|/2 + V_{RX-CM-DC}$
 $V_{RX-CM-DC} = DC_{(avg)}$ of $|V_{RX-D+} + V_{RX-D-}|/2$.
- 147/ Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at +300 mV and -300 mV, respectively.
- 148/ The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes - see Figure 51). Note: that the series capacitors CTX is optional for the return loss measurement.
- 149/ Measured over 50 MHz to 1.25 GHz with the D+ and D-lines biased at 0V.
- 150/ RX DC Differential
- 151/ Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 152/ Required RX D+ as well as D-DC Impedance ($50 \pm 20\%$ tolerance).
- 153/ Required RX D+ as well as D-DC Impedance when the Receiver terminations do not have power.
- 154/ The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 155/ It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
- 156/ $V_{RX-IDLE-DET-DIFFp-p} = 2 * |V_{RX-D+} - V_{RX-D-}|$. Measured at the package pins of the Receiver
- 157/ An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
- 158/ Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.
- 159/ 8 ns applies only to serial RapidIO with 125-MHz reference clock.
- 160/ Voltage relative to COMMON of either signal comprising a differential pair.
- 161/ Skew at the transmitter output between lanes of a multilane link.
- 162/ ± 100 ppm.
- 164/ Measured at receiver.
- 165/ Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
- 166/ Skew at the receiver input between lanes of a multilane link.
- 167/ Guaranteed by design or characterization. Not by electrical test.
- 168/ This subject is guaranteed by design or characterization. Not by electrical test.

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[illegible]

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

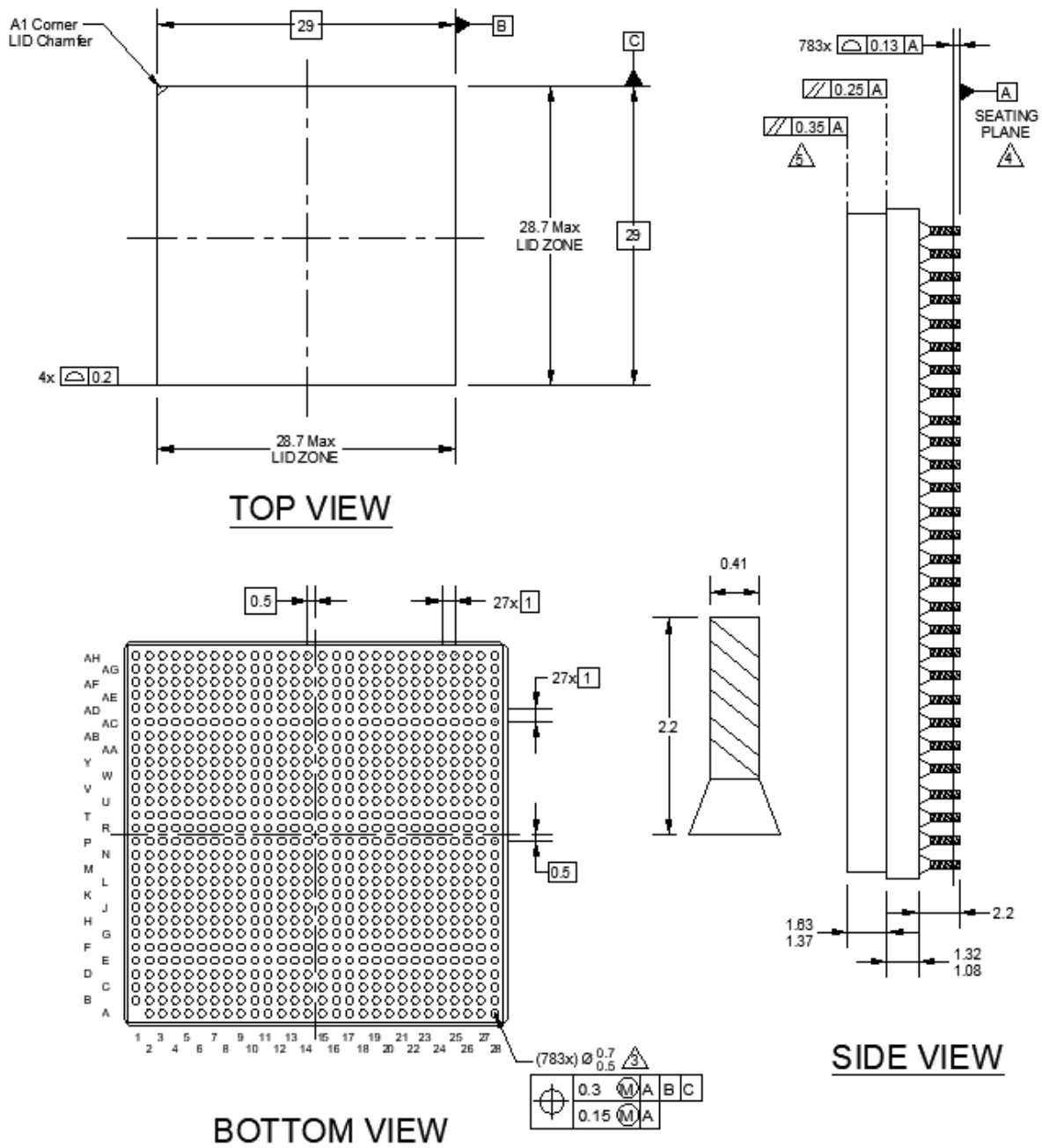
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Case Y



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

FIGURE 2. Case outline.

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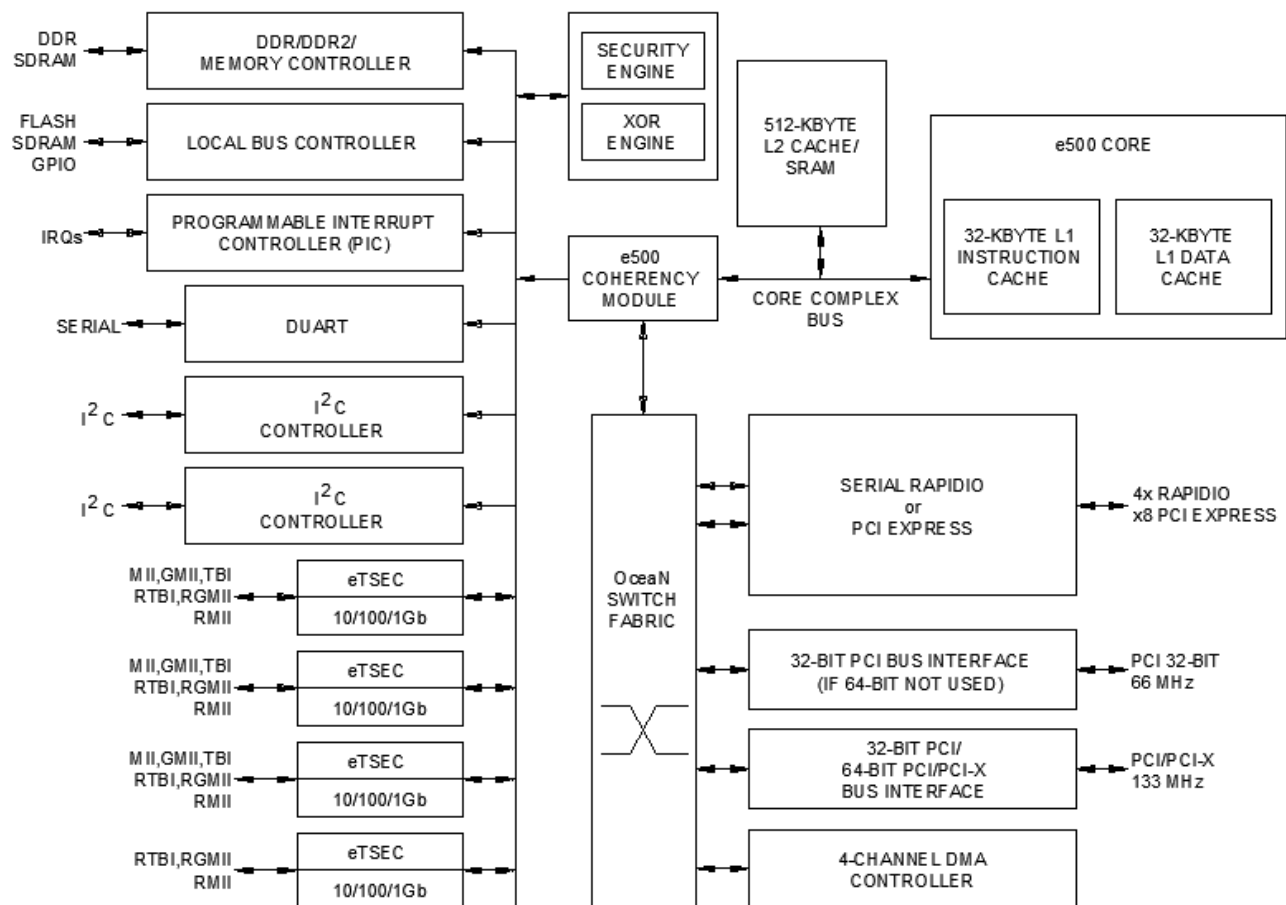


FIGURE 3. Block diagram.

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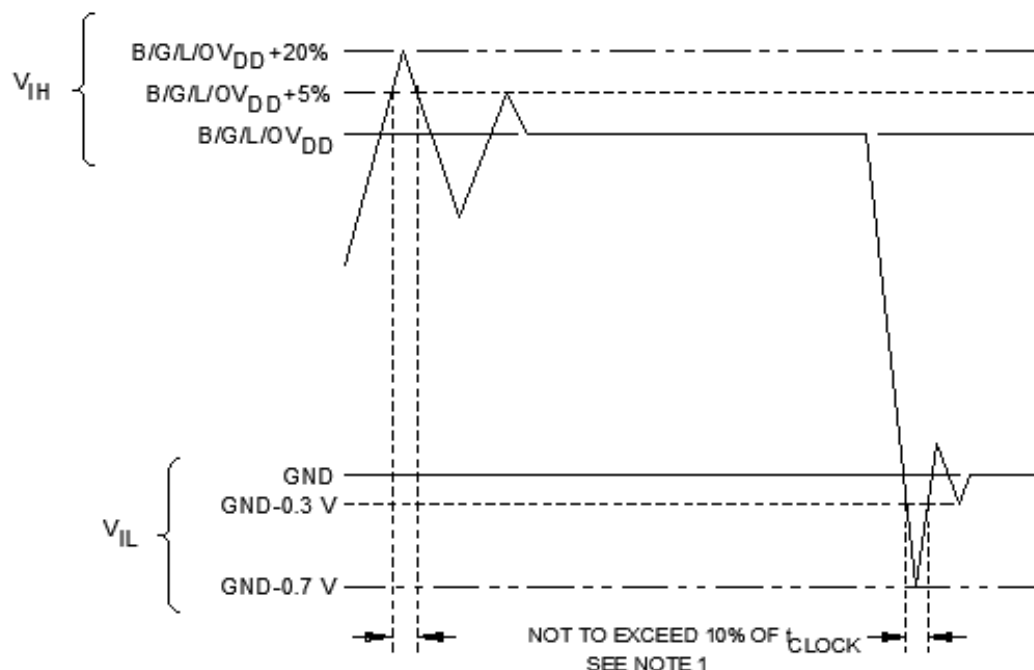
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NOTES:

- t_{CLOCK} refers to the clock period associated with the respective interface:
 For I²C and JTAG, t_{CLOCK} references SYSCLK.
 For DDR, t_{CLOCK} references MCLK.
 For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
 For LBIU, t_{CLOCK} references LCLK.
 For PCI, t_{CLOCK} references PCIn_{CLK} or SYSCLK.
 For SerDes, t_{CLOCK} references SD_REF_CLK.
- Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

FIGURE 4. Overshoot/Undershoot Voltage for GVDD/OVDD/LVDD/BVDD.

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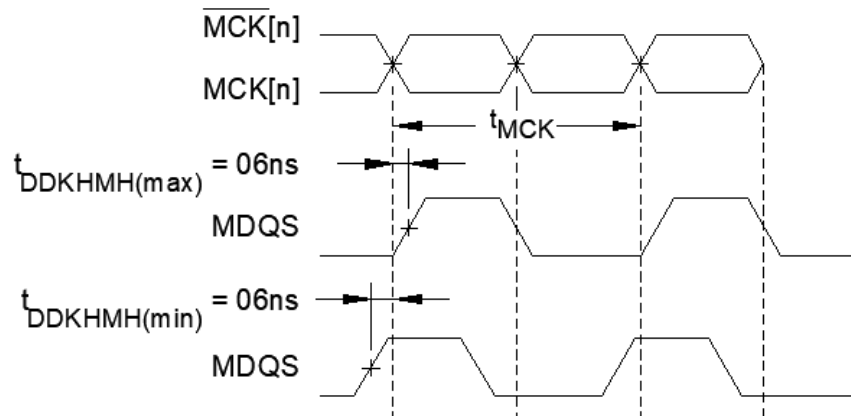


FIGURE 5. Timing Diagram for t_{DDKMH} .

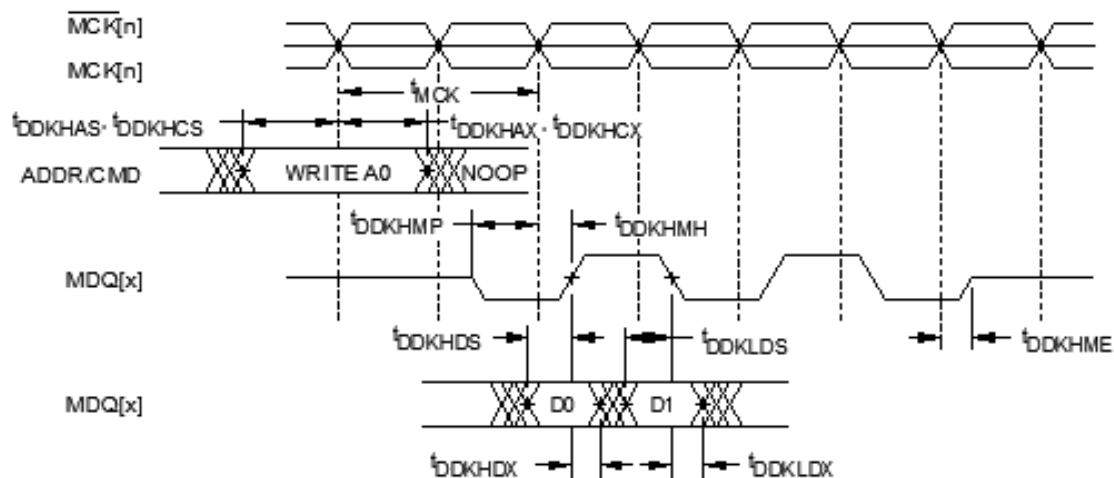


FIGURE 6. DDR SDRAM Output Timing Diagram.

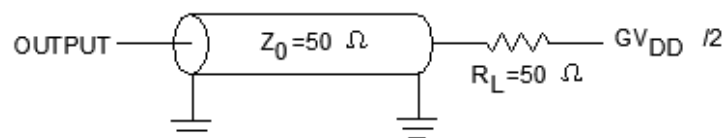


FIGURE 7. DDR AC Test Load.

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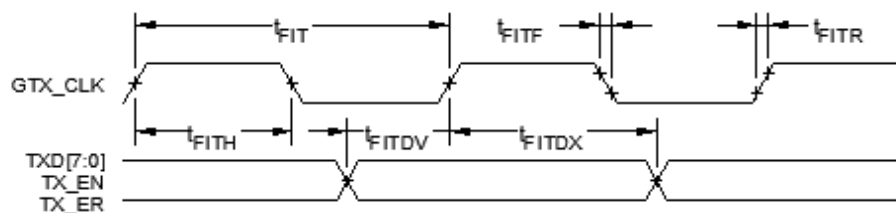


FIGURE 8. FIFO Transmit AC Timing Diagram.

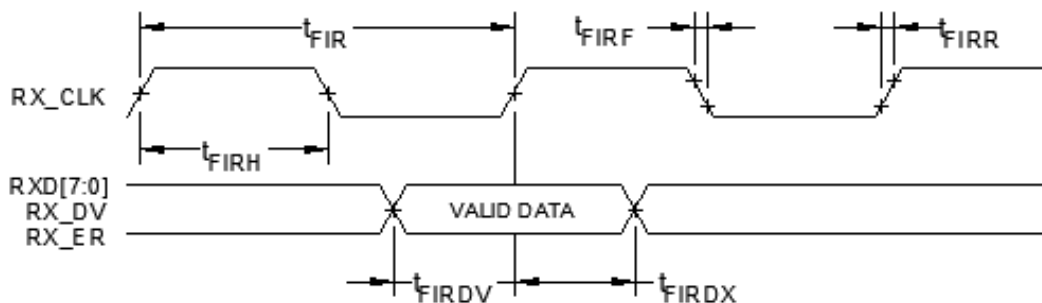


FIGURE 9. FIFO Receive AC Timing Diagram.

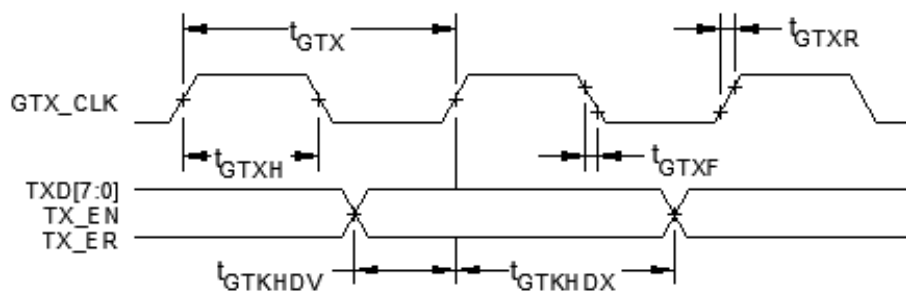


FIGURE 10. GMII Transmit AC Timing Diagram.

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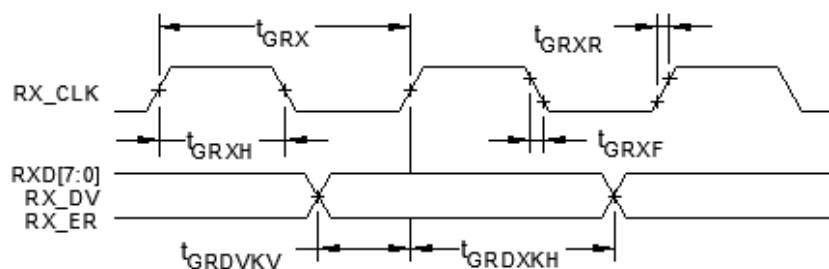


FIGURE 11. GMII Receive AC Timing Diagram.

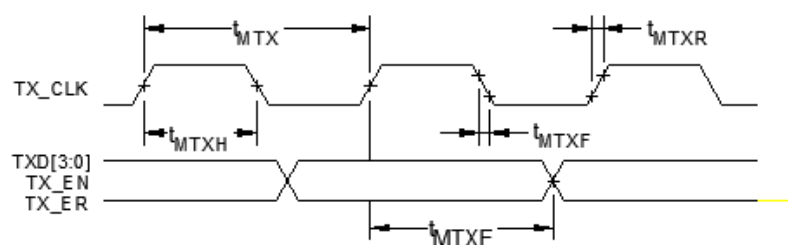


FIGURE 12. MII Transmit AC Timing Diagram.

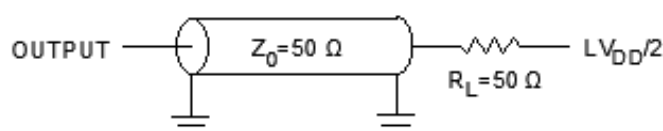


FIGURE 13. eTSEC AC Test Load.

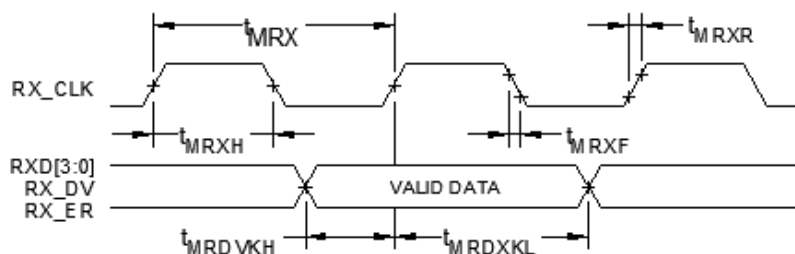


FIGURE 14. MII Receive AC Timing Diagram.

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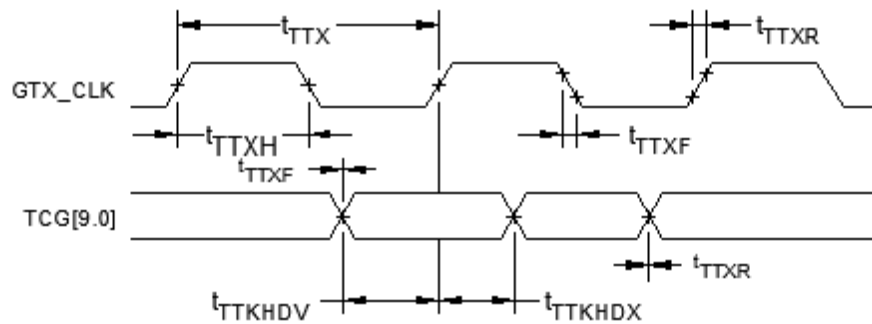


FIGURE 15. TBI Transmit AC Timing Diagram.

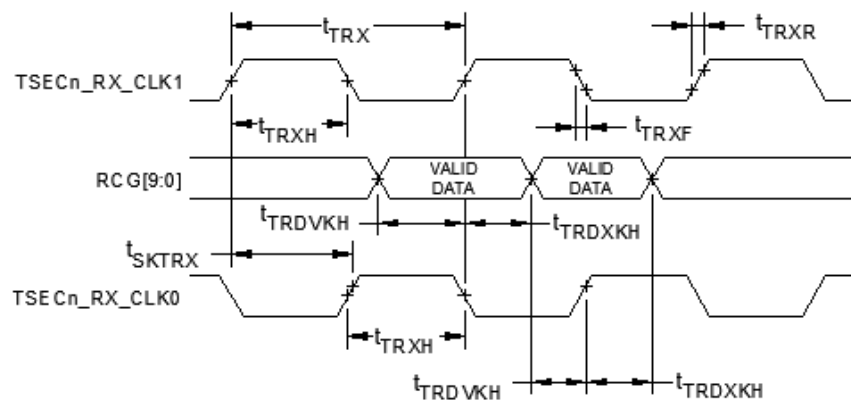


FIGURE 16. TBI Receive AC Timing Diagram.

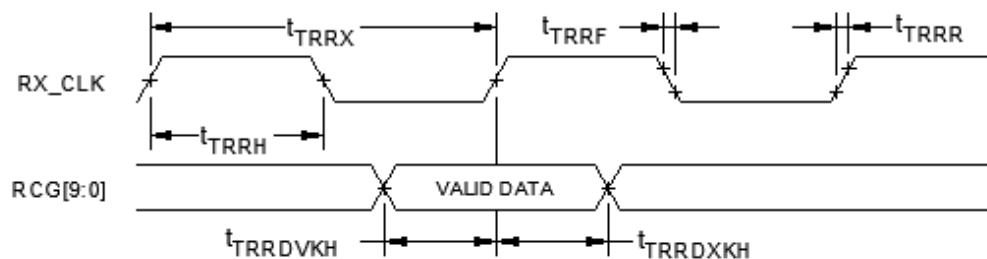


FIGURE 17. TBI Single-Clock Mode Receive AC Timing Diagram.

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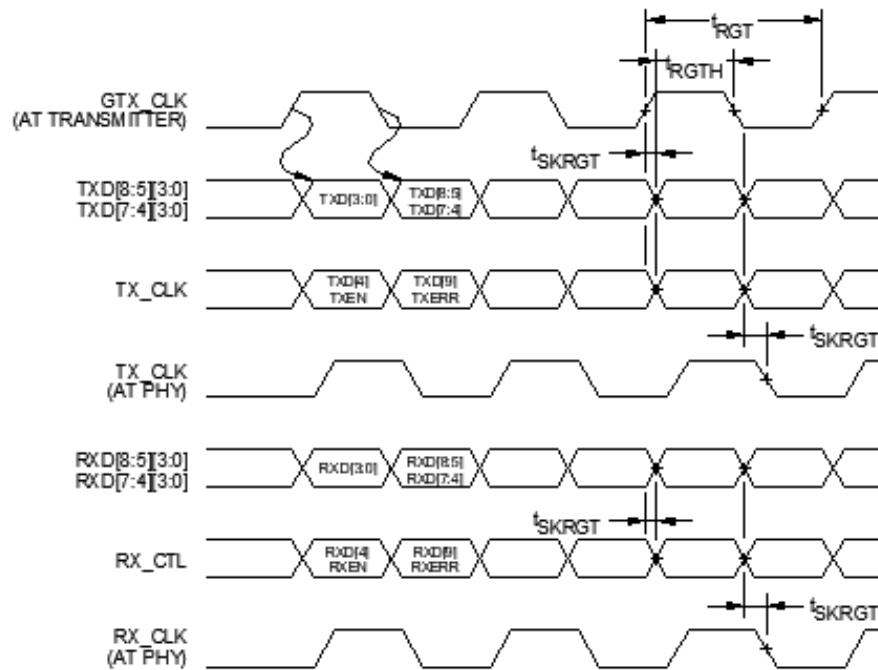


FIGURE 18. RGMII and RTBI AC Timing and Multiplexing Diagrams.

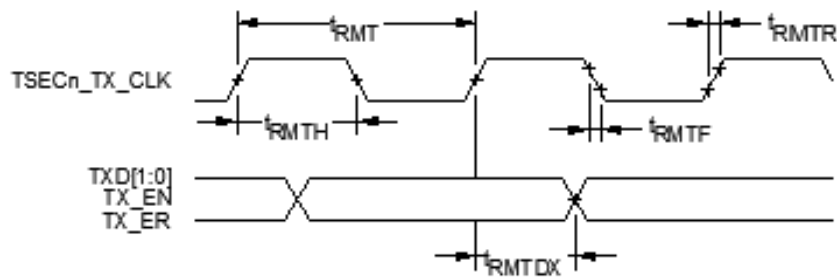


FIGURE 19. RMII Transmit AC Timing Diagram.

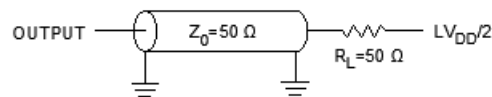


FIGURE 20. eTSEC AC Test Load

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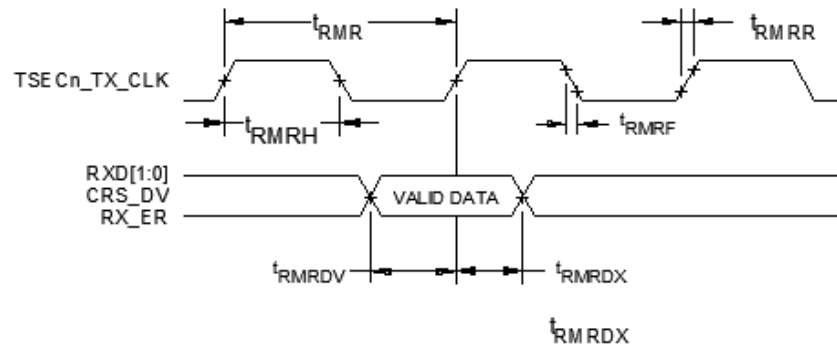


FIGURE 21. RMII Receive AC Timing Diagram.

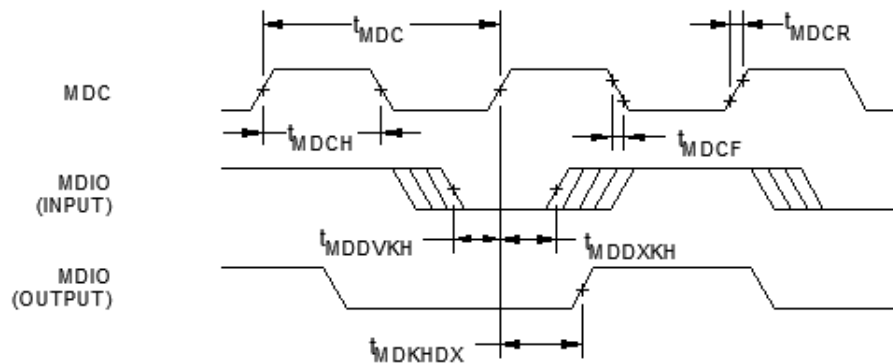


FIGURE 22. MII Management Interface Timing Diagram.

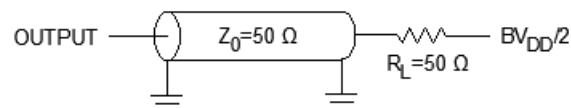


FIGURE 23. Local Bus AC Test Load.

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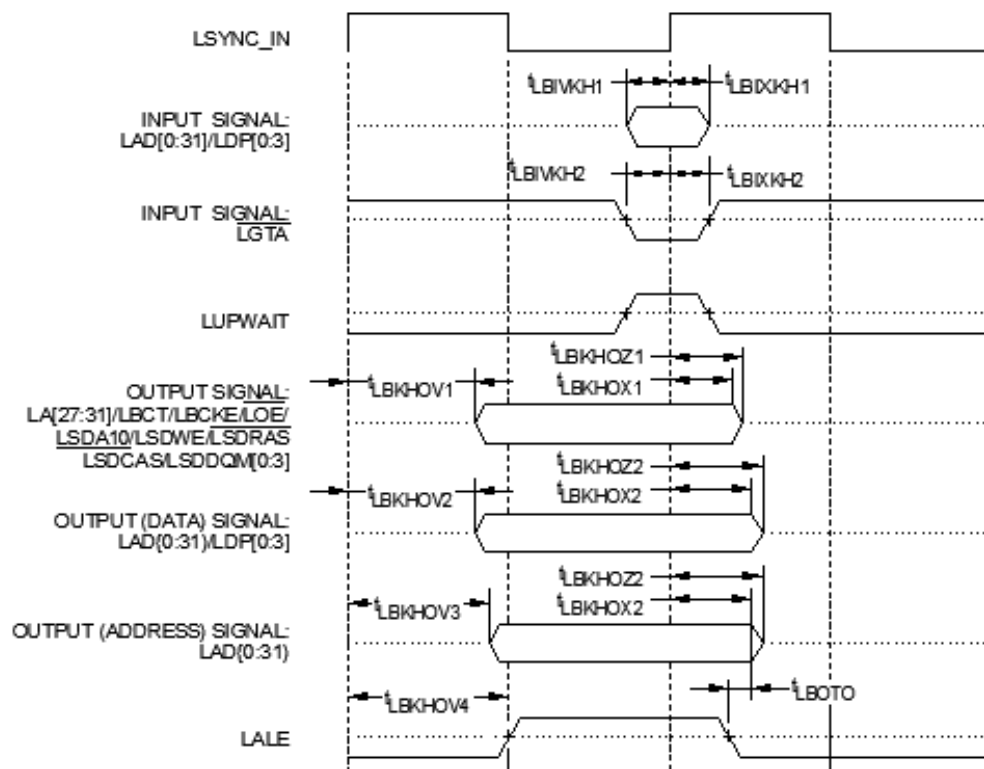


FIGURE 24. Local Bus Signals. (PLL Enabled).

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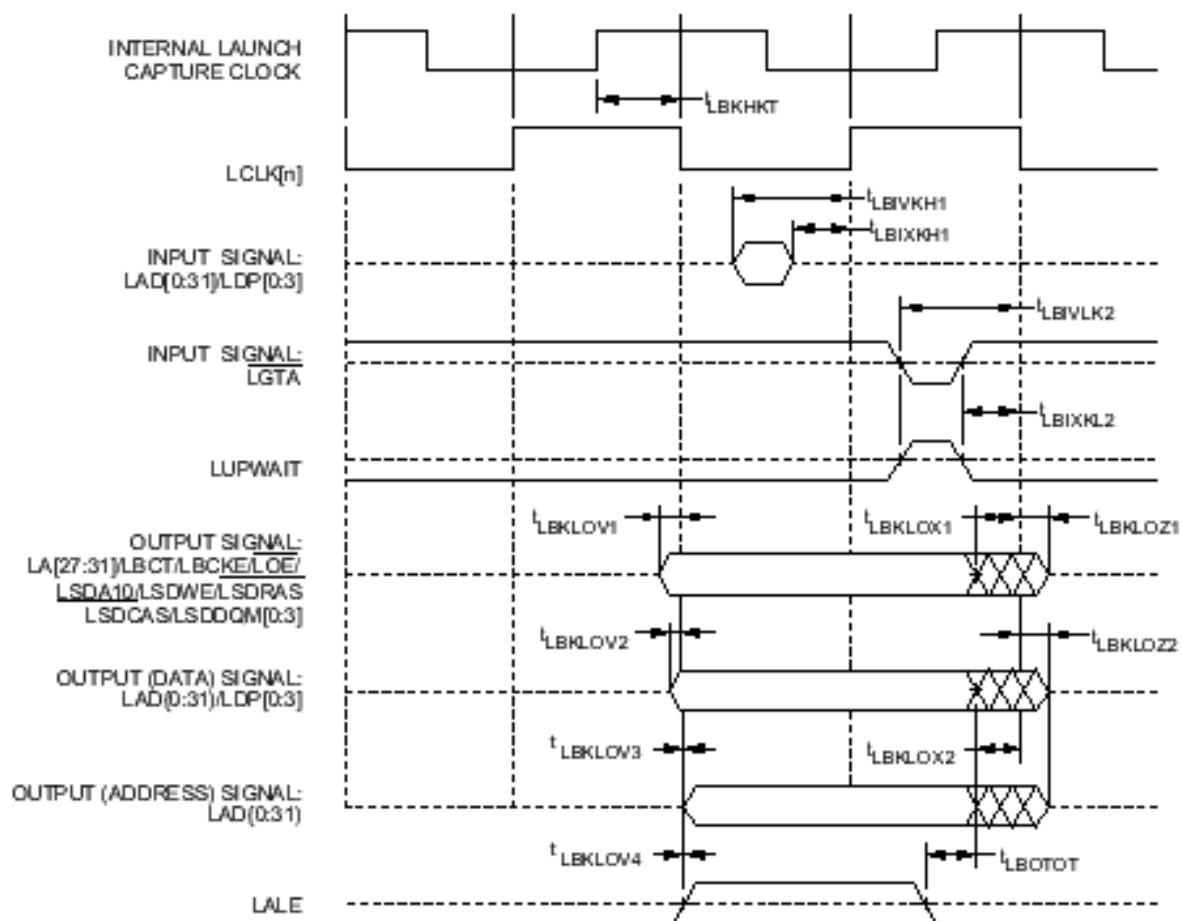
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NOTES:

1. In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHK1} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).

FIGURE 25. Local Bus Signals (PLL Bypass Mode).

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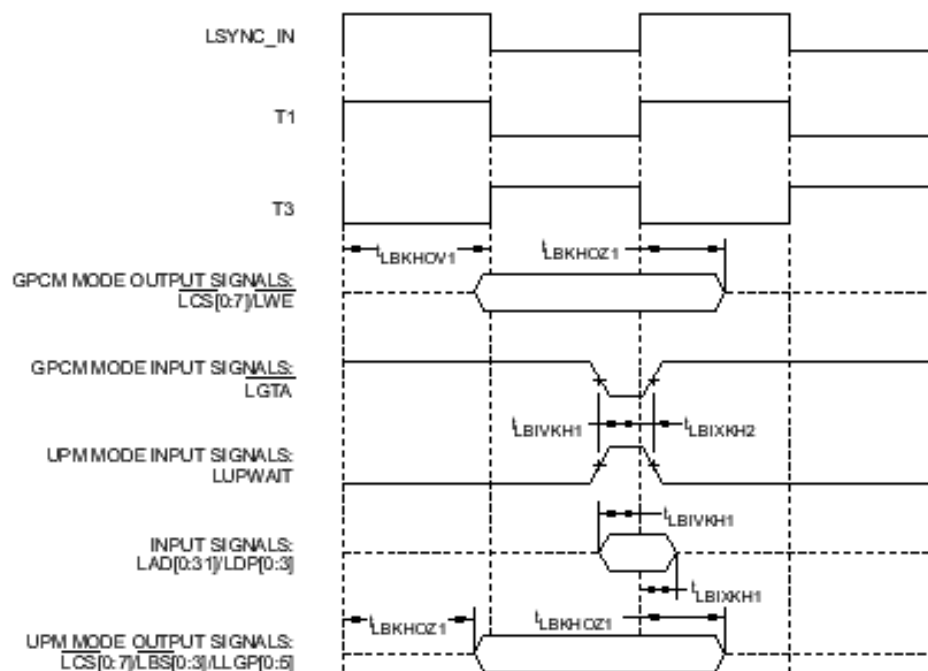


FIGURE 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled).

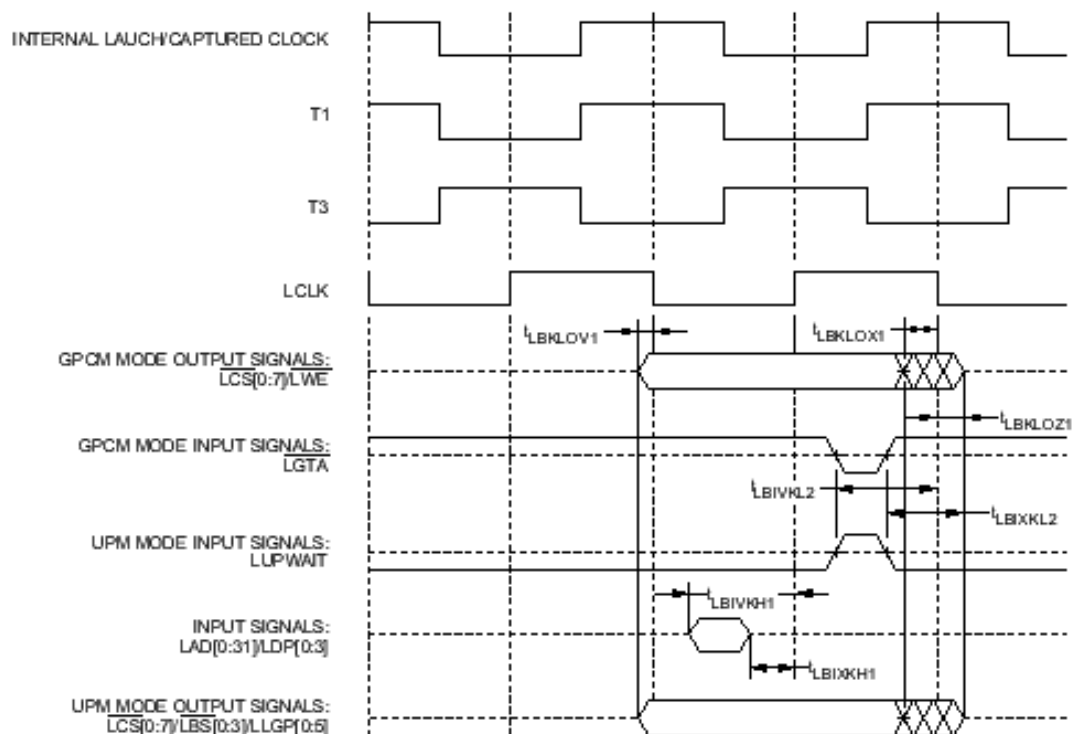


FIGURE 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode).

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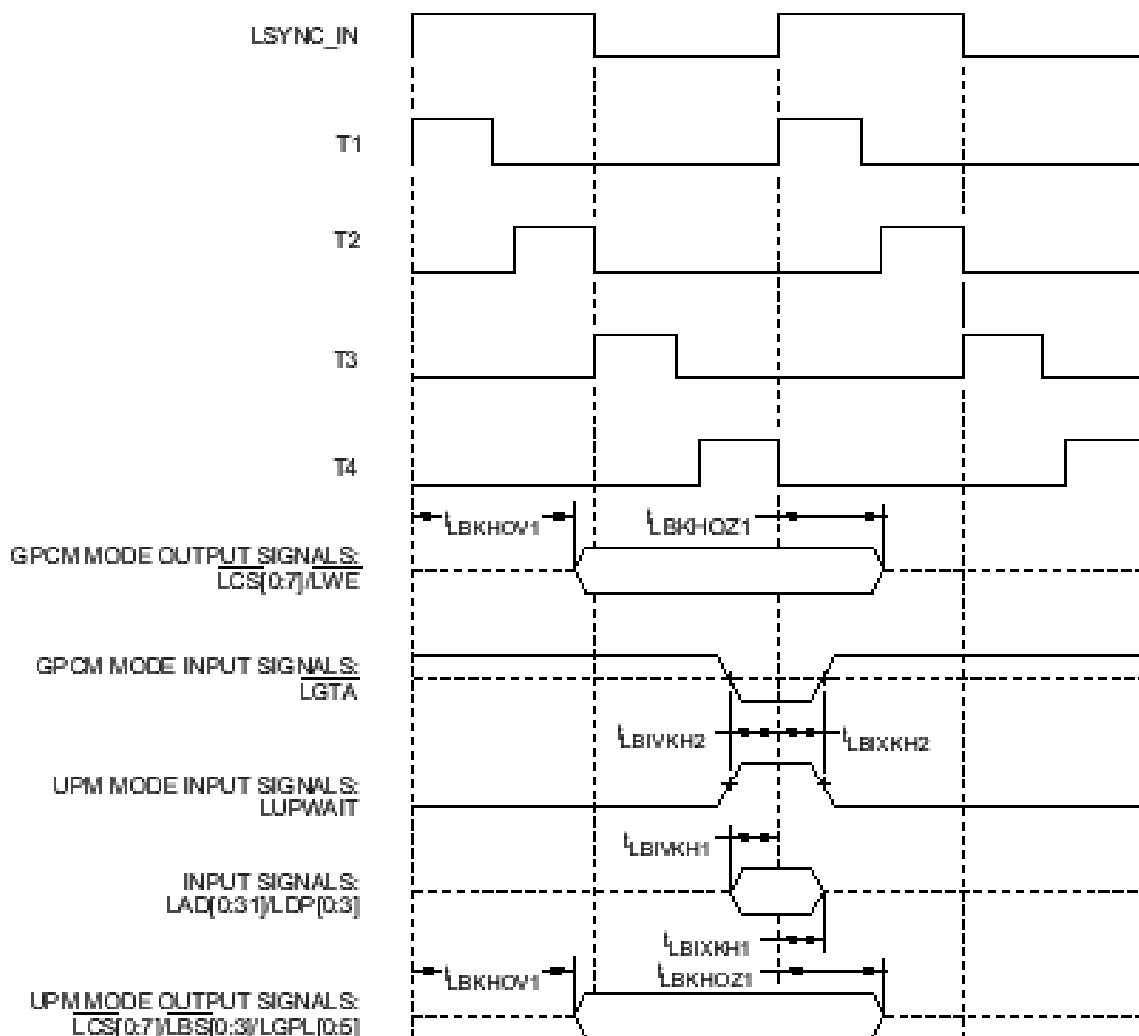


FIGURE 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled).

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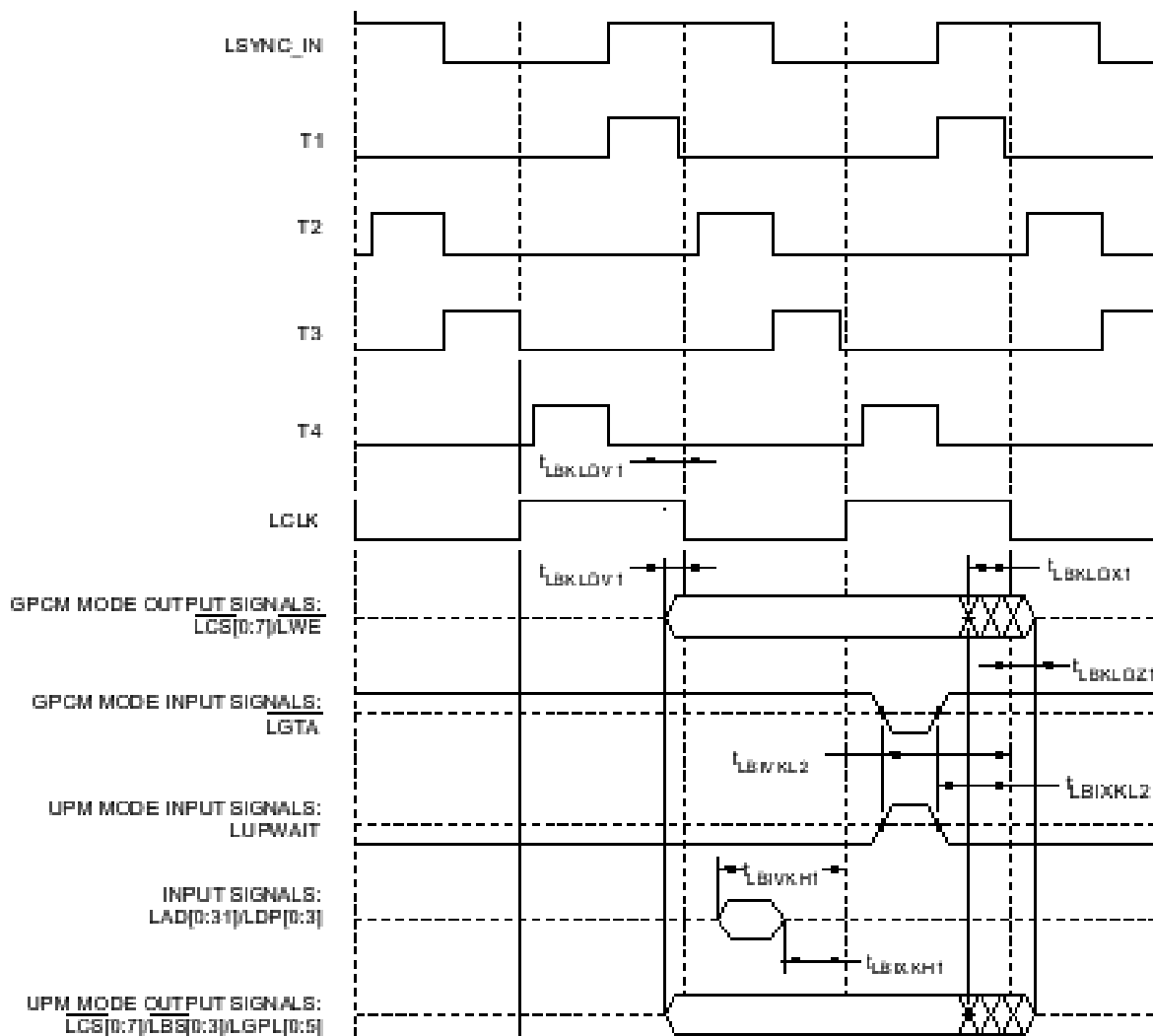


FIGURE 29. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode).

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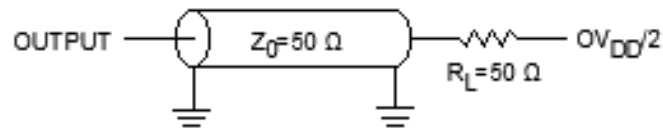


FIGURE 30. AC Test Load for the JTAG Interface.

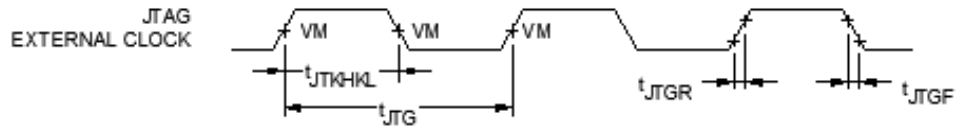


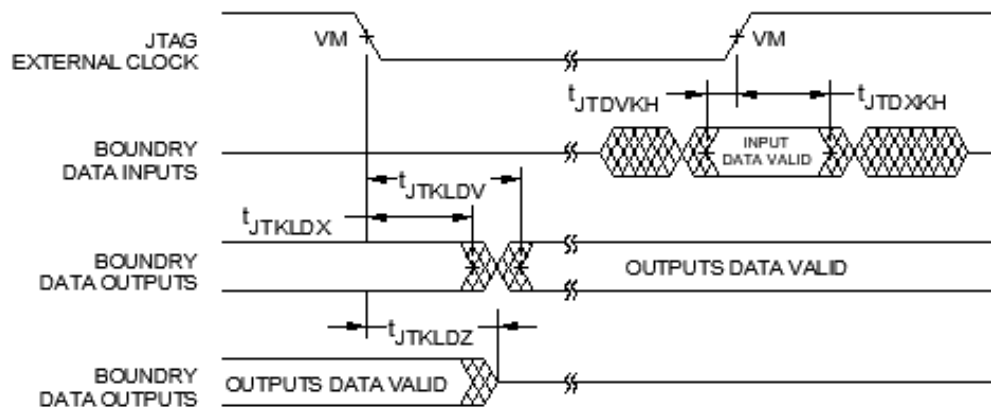
FIGURE 31. JTAG Clock Input Timing Diagram.



NOTES:

1. VM = Midpoint Voltage ($OV_{DD}/2$).

FIGURE 32. $\overline{TRST}$ Timing Diagram.



NOTES:

1. VM = Midpoint Voltage ($OV_{DD}/2$).

FIGURE 33. Boundary-scan Timing Diagram.

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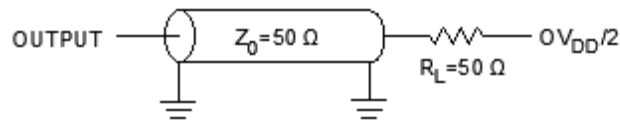


FIGURE 34. I²C Bus AC Test Load.

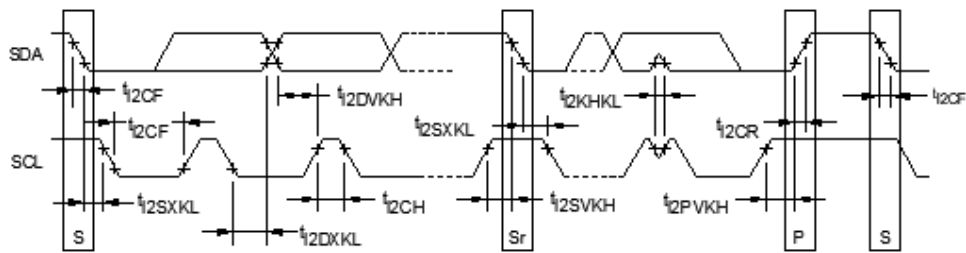


FIGURE 35. I²C Bus AC Timing Diagram.

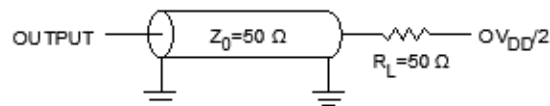


FIGURE 36. PCI/PCI-X AC Test Load.

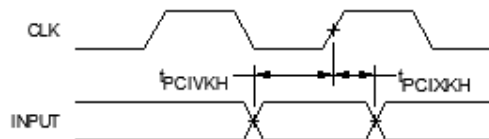


FIGURE 37. PCI/PCI-X Input AC Timing Measurement Conditions.

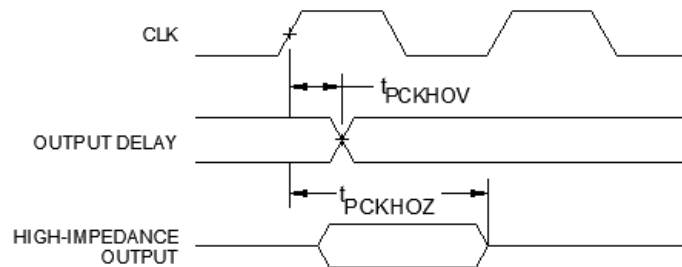


FIGURE 38. PCI/PCI-X Output AC Timing Measurement Condition.

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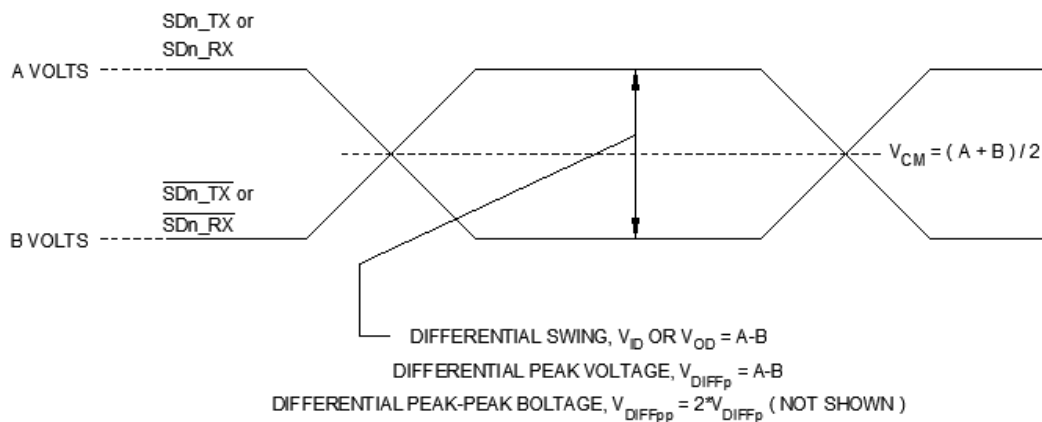


FIGURE 39. Differential Voltage Definitions for Transmitter or Receiver.

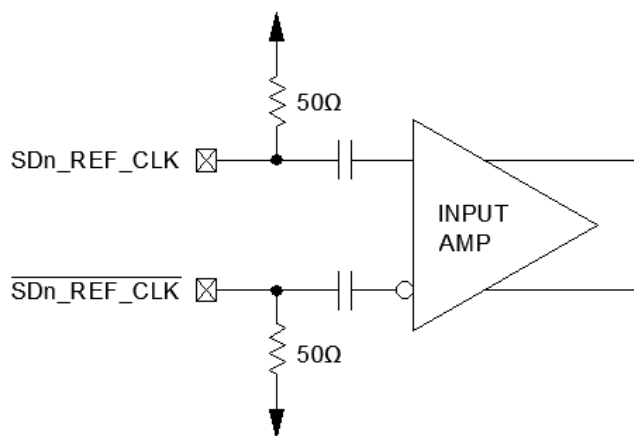


FIGURE 40. Receiver of SerDes Reference Clocks.

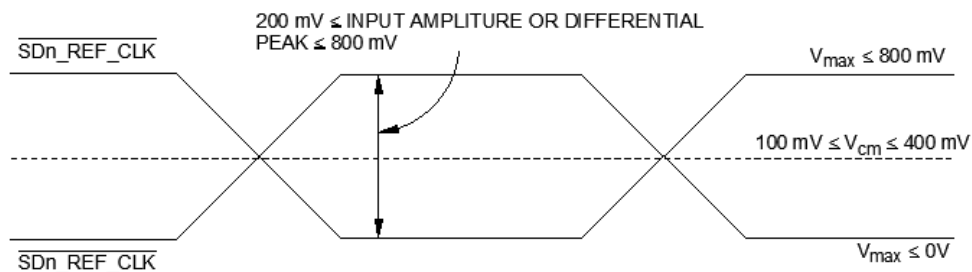


FIGURE 41. Differential Reference Clock Input DC Requirements (External DC-Coupled).

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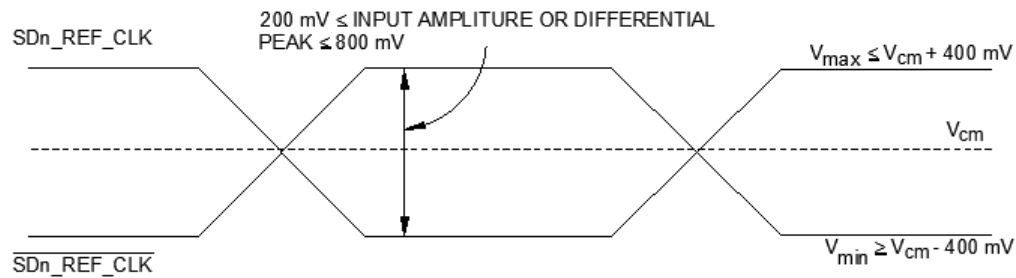


FIGURE 42. Differential Reference Clock Input DC Requirements (External AC-Coupled).

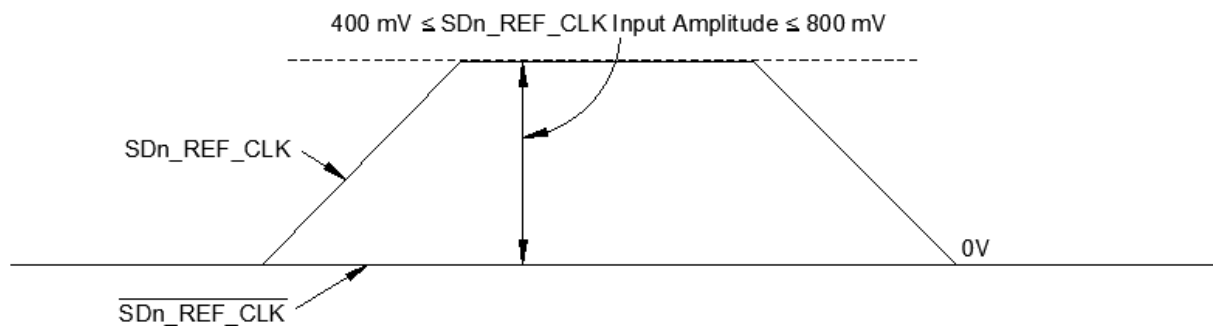


FIGURE 43. Single-Ended Reference Clock Input DC Requirements.

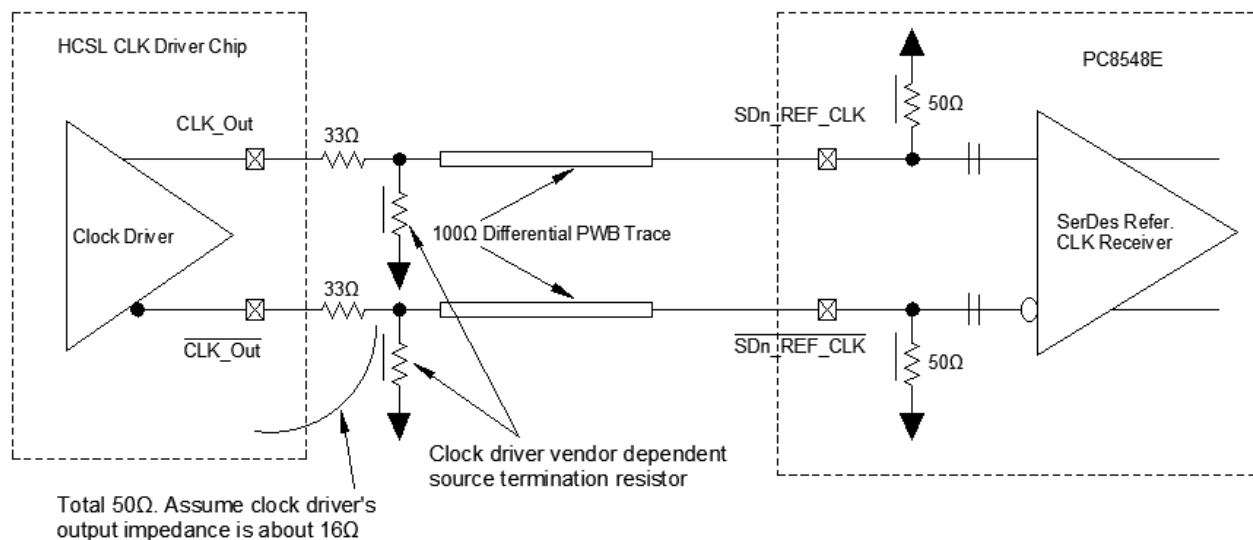


FIGURE 44. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only).

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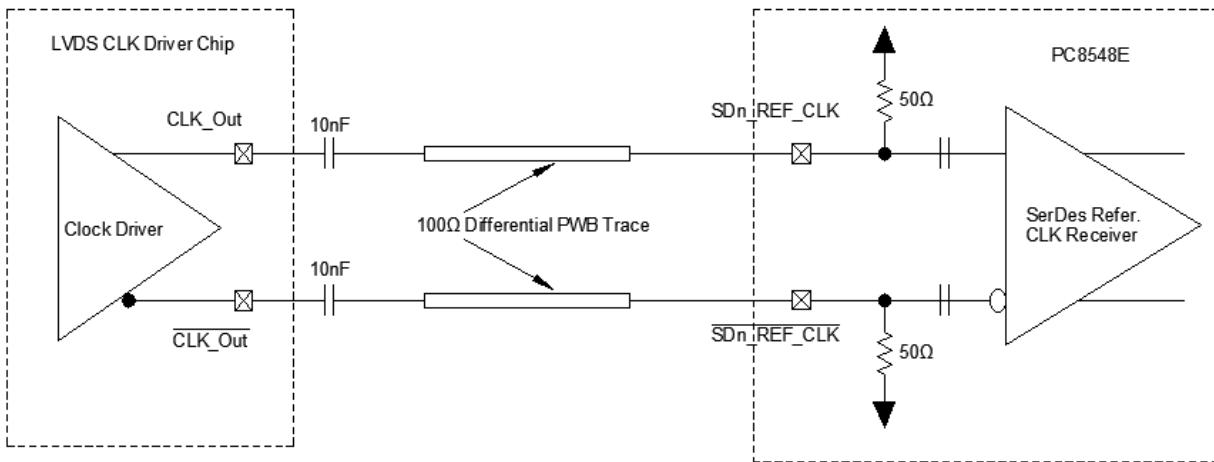


FIGURE 45. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only).

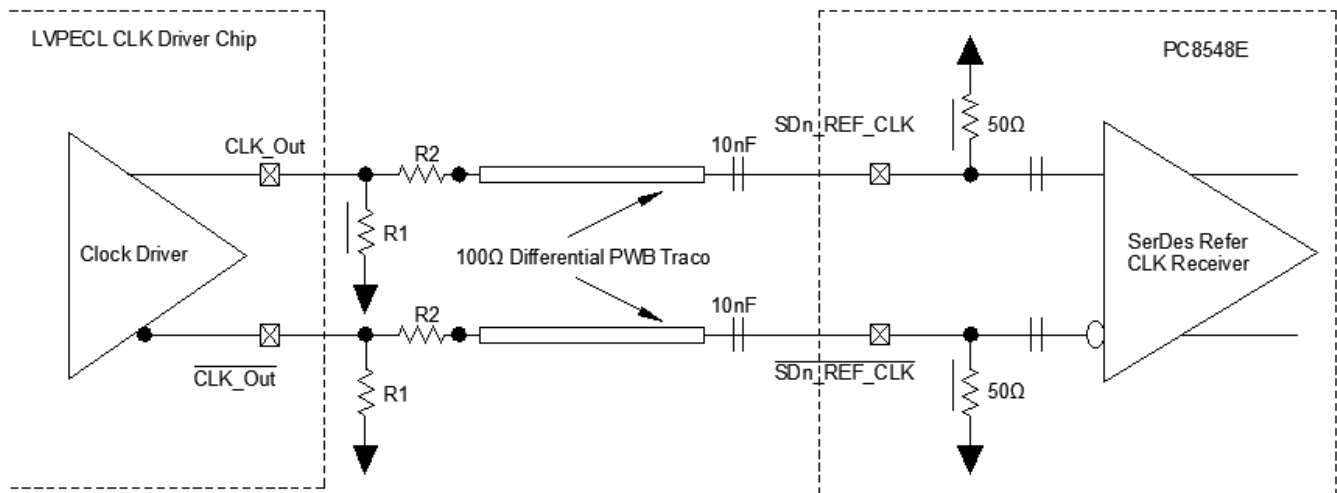


FIGURE 46. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only).

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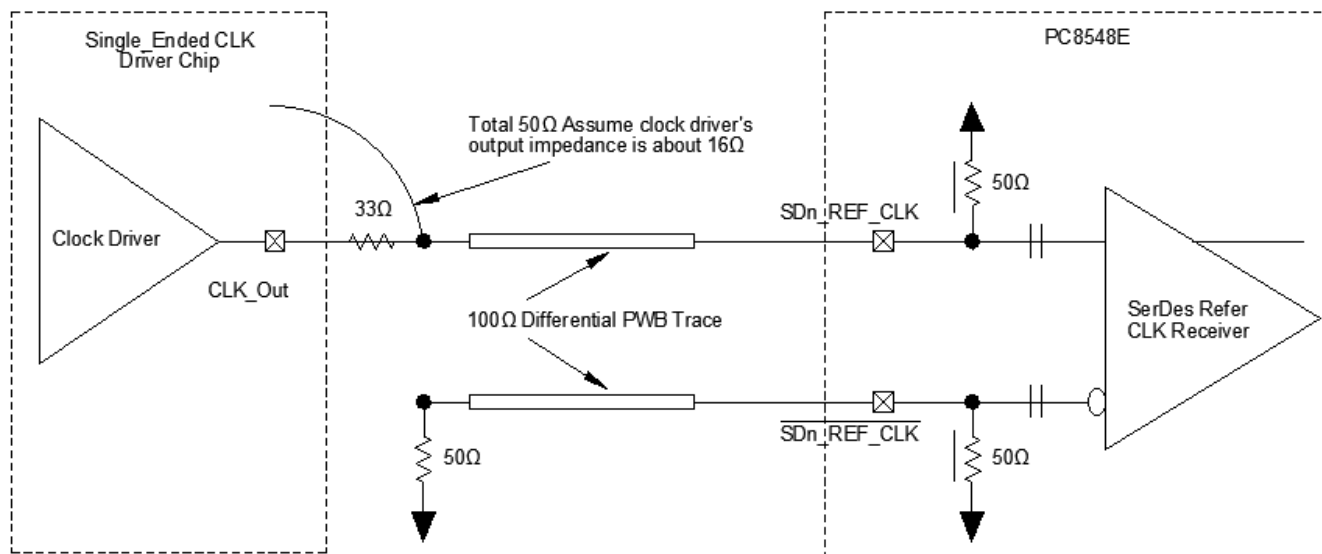


FIGURE 47. Single-Ended Connection (Reference Only).

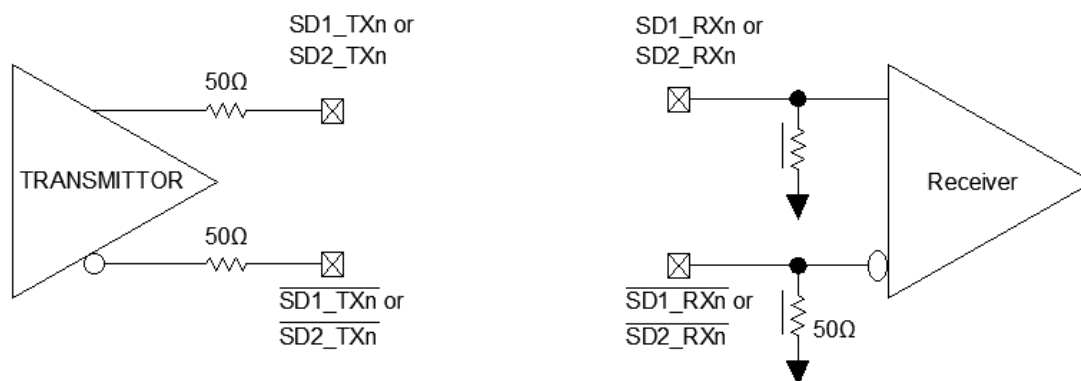


FIGURE 48. SerDes Transmitter and Receiver Reference Circuits.

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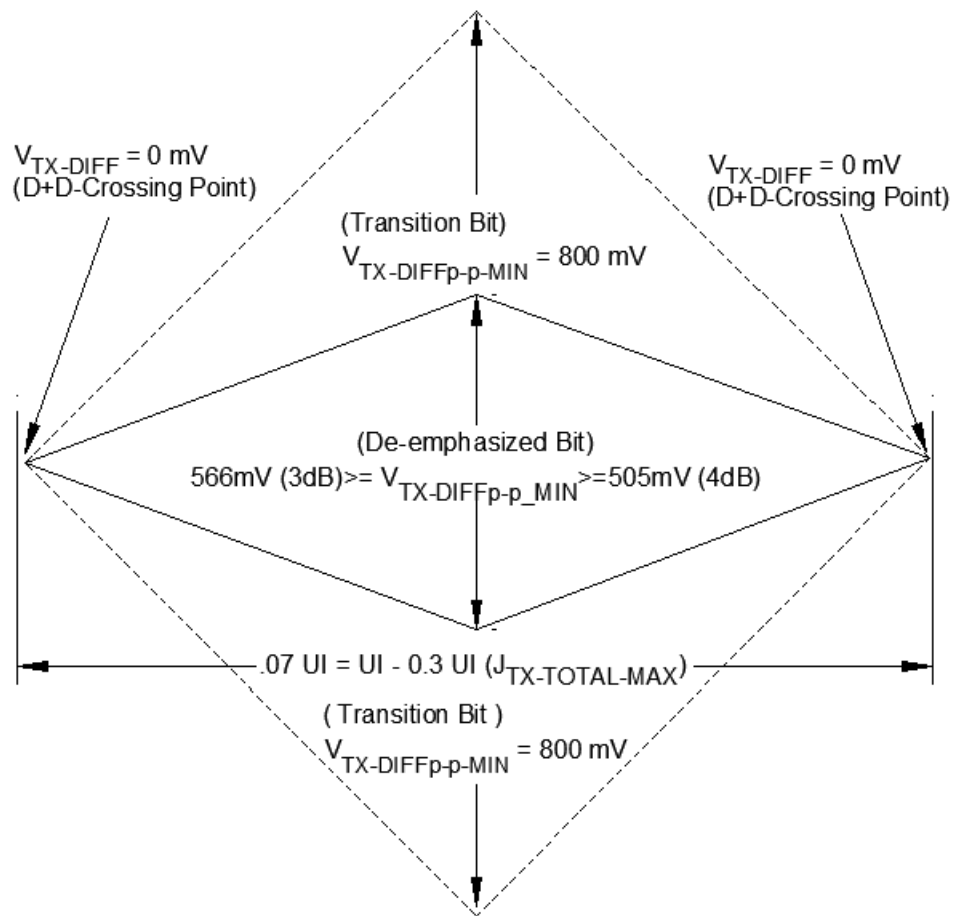


FIGURE 49. Minimum Transmitter Timing and Voltage Output Compliance Specifications.

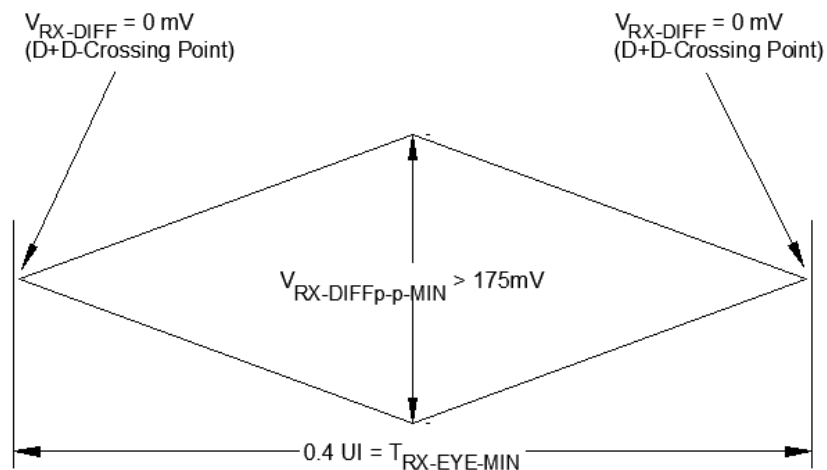


FIGURE 50. Minimum Receiver Eye Timing and Voltage Compliance Specification.

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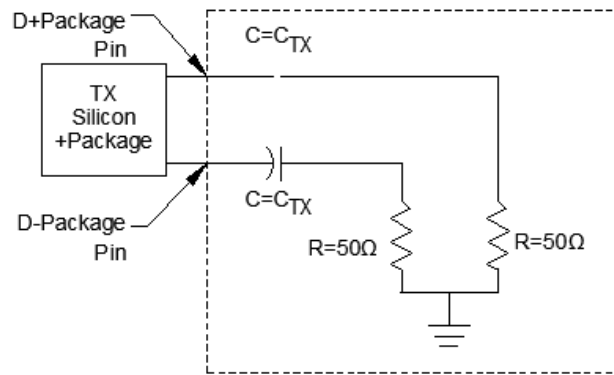


FIGURE 51. Compliance Test/Measurement Load.

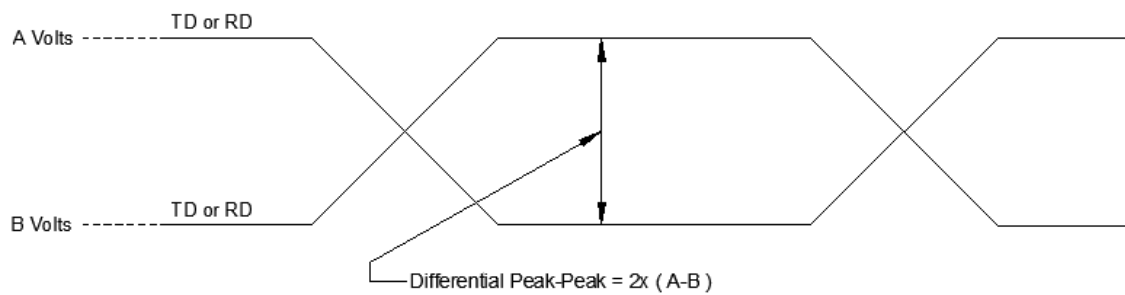


FIGURE 52. Differential Peak-to-Peak Voltage of Transmitter or Receiver.

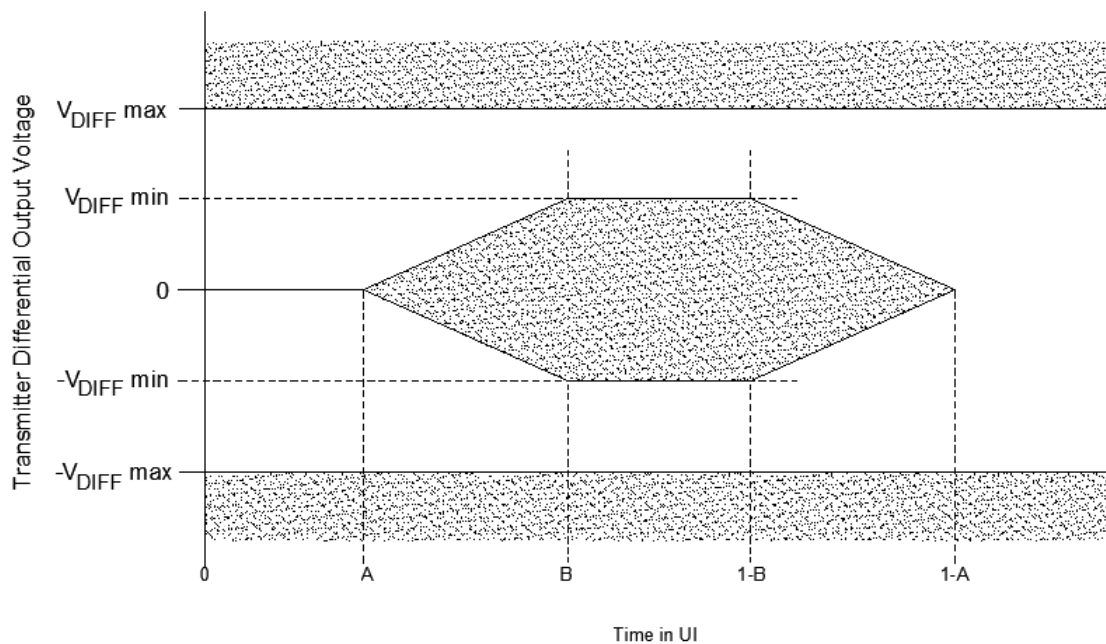


FIGURE 53. Transmitter Output Compliance Mask.

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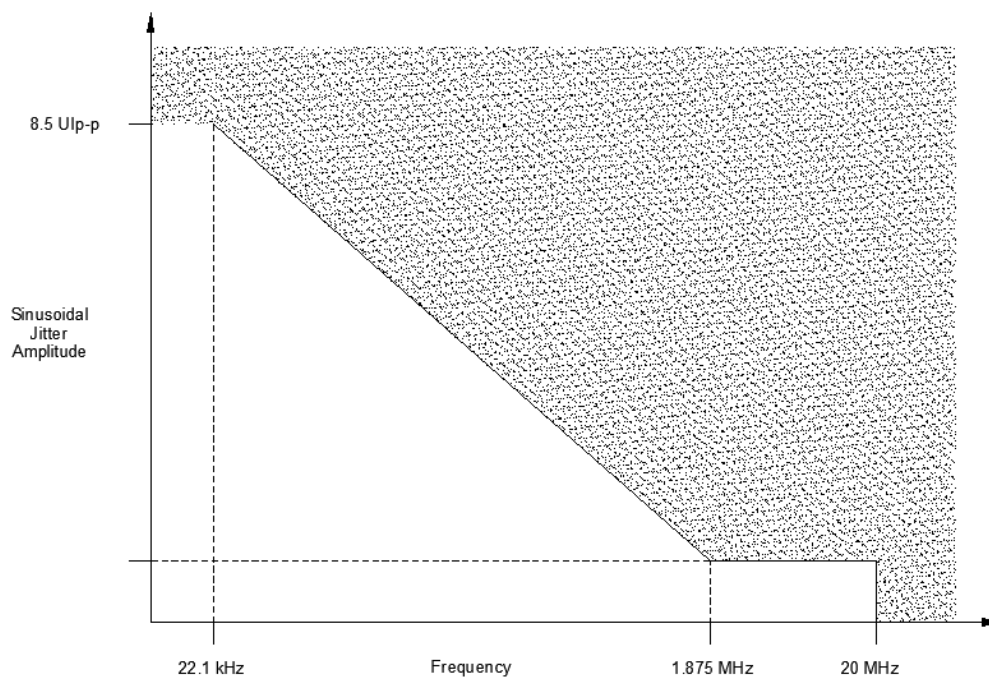


FIGURE 54. Single Frequency Sinusoidal Jitter Limits.

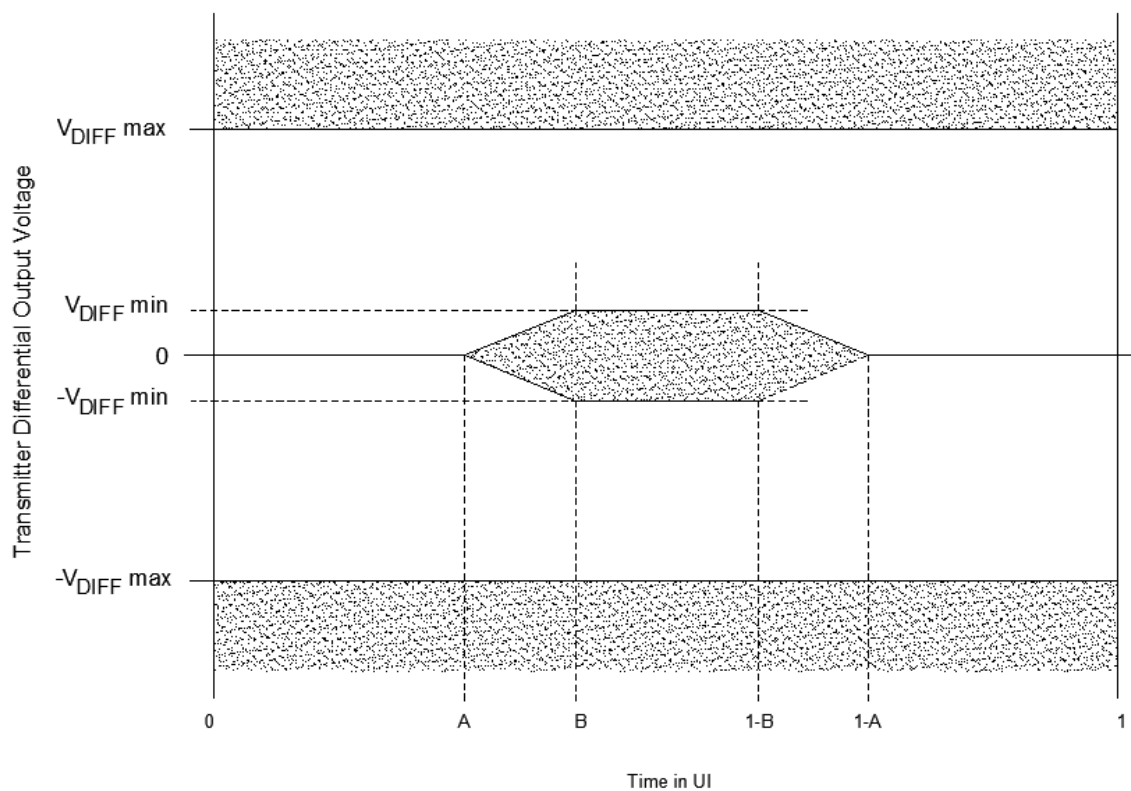


FIGURE 55. Receiver Input Compliance Mask.

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4. VERIFICATION

4.1 Sampling and inspection. For class Y device, sampling and inspection procedures shall be performed in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For class Y device, screening test shall be performed in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Burn-in criteria for class Y device.

- a. The manufacturers shall provide appropriate burn-in information herein table II in accordance with JEDEC publication JEP163. The burn-in test duration, test condition and test temperature shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table III herein.
- c. Additional screening for device class Y shall be required as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device class Y. Qualification inspection for device class Y shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for class Y shall be performed in accordance with MIL-PRF-38535 including groups A, B, C, D, and E (RHA test) and as specified.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Devices induced latch-up tests are required for device class Y. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD20 and table IA herein. For C_{IN} and C_{PD} , test all applicable pins on five devices with zero failures.
- d. For device class Y, subgroups 7 and 8 tests shall be sufficient to verify the truth table on figure 2 herein or verifying the functionality of the device.

4.4.2 Group B inspection.

- a. For class Y flip chip devices with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures of lid shear test for approval.
- b. For ball grid array (BGA) packages, ball shear test shall be performed in accordance with JESD22-B117.
- c. For column grid array (CGA) packages, solder column pull test shall be performed in accordance with TM 2038 of MIL-STD-883.

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4.4.3. Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein. For device class Y steady-state life tests circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.2.1 Additional criteria for device class Y. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device class Y, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K Rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

- a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.
- b. Transient dose rate upset testing for class Y devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

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4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or C JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip. Range of the ion which shall be sufficiently penetrate well beyond the deepest part volume of the devices to of the sensitive detect latch-up.
- e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature $\pm 10^\circ\text{C}$.
- f. Bias conditions shall be defined by the manufacturer for latchup measurements.
- g. SEP test limits are available upon request.

4.4.4.5 Neutron irradiation/displacement damage testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ after an exposure of 1×10^{12} neutrons/cm².

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TABLE II. Electrical test requirements.

Test requirements (in accordance with MIL-PRF-38535, screening table IA, group A, B, C, D, E and MIL-STD-883 test method)	Subgroups (in accordance with MIL-PRF-38535, table III)
	Device class Y
Interim electrical parameters, (screening table IA)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Static burn-in I, method 1015 (see 4.2.1a)	Required <u>1/</u>
Static burn-in II method 1015 (see 4.2.1a)	Required <u>1/</u>
Dynamic burn-in , method 1015 (see 4.2.1a)	Required <u>1/</u>
Final electrical parameters, (screening table IA)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group B end point electrical parameters, (see 4.4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters, (see 4.4.3)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group D end-point electrical parameters, (see 4.4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group E end-point electrical parameters, (see 4.4.5) <u>3/</u>	1,7,9
Post-column attach electrical parameters test (see 4.2) <u>3/</u>	1

1/ The manufacturers shall be provide appropriate burn-in information herein table II in accordance with burn-in publication JEP163.

2/ PDA applies to subgroups 1 and 7.

3/ For flip chip class Y BGA/CGA devices, screening and group A, B, C, D and RHA test group E shall be preformed at land grid array (LGA) level. i.e. before ball or column attached to the devices. After ball or column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

x/ For flip chip Class Y device, Nondestructive bond pull (NDBP) test is not required.

x/ For devices without a cavity such as class Y or flip chip devices with underfill, Particle impact noise detection (PIND) test is not applicable.

x/ For flip chip technology C-SAM inspection is required. C-SAM inspection shall be performed on each flip chip device in accordance with TM 2030 of MIL-STD-883.

x/ C-SAM test shall be performed on each device when a heat sink or lid is attached directly to the back side of the flip chip die in accordance with TM 2030 of MIL-STD-883.

x/ Seal test (TM 1014) is not required for class Y non-hermetic devices.

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TABLE III. Burn-in and operating life test delta parameters (+25°C).

All critical parameter <u>1/</u> <u>2/</u>	Symbol	Device types	Delta limits <u>3/</u>
Power Sleep	power_mgmt_ sleep_vdd	A	±0.250A
I _{DD} Max 1200 MHz	p_idd_max_core 1200_0301_nom 11	A	±10%
Fmax Nom Level	s_fmax_elf_1801 _nom1045	MHz	±10%
Platform Fmax Nom Level	s_fmax_tsecplat _3001_nom1033	MHz	±10%

1/ These parameters shall be recorded before and after the required burn-in to determine delta drift limits.

2/ Manufacturer shall be specified in table III all critical parameters that have delta drift values during burn-in test.

3/ The delta drift limit shall be computed with reference to the previous interim electrical parameters. The delta drift limit shall be specified in table III.

4.5 Delta measurements for device class Y. Class Y devices, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535, table III. Delta limits shall be required on class Y devices, and shall be recorded before and after the required burn-in screens and steady-state life tests to determine delta limit compliance. The electrical parameters to be measured, with associated delta limits are listed in table III.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class Y.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device class Y. Sources of supply for device class Y are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Package integrity demonstration test plan (PIDTP). For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Flip chip PIDTP also shall address the materials and processes unique to solder bump interconnect attach, underfill and thermal interface materials (TIM). The QA approved PIDTP shall be documented in the product QM plan and shall be available upon requested in the purchase order or contract.

6.8 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplying to this drawing with terminal lead finish mark "F". Terminal lead finish F is tin (Sn) and lead (Pb) alloy with copper spiral column, and solder column material contains compositions of Sn= 15% and Pb=85% and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

6.9 BGA packages lead finish: Microcircuits devices for ball grid array (BGA) packages are supplying to this drawing with terminal lead finish mark "F". Terminal lead finish F is tin (Sn) and lead (Pb) and Bismuth (Bi) alloy, and solder ball material contains compositions of Sn= 63% and Pb=37% .

6.10 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latchup (SEL).

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DATE: 21-03-09

Approved sources of supply for SMD 5962-20209 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-2020901YXF	F8385	PC8548EMGHBYLATGB
5962-2020901YYF	F8385	PC8548EMGCBYLATGB
5962-2020902YXF	F8385	PC8548EMGHBYLAUHB
5962-2020902YYF	F8385	PC8548EMGCBYLAUHB
5962-2020903YXF	F8385	PC8548MGHBYLATGB
5962-2020903YYF	F8385	PC8548MGCBYLATGB
5962-2020904YXF	F8385	PC8548MGHBYLAUHB
5962-2020904YYF	F8385	PC8548MGCBYLAUHB

- 1/ Microcircuits devices for column grid array (CGA) or ball grid array (BGA) packages are supplied to this drawing with terminal lead finish mark "F" which are a tin (Sn) and lead (Pb) alloy. See section 6.8 and 6.9 for the solder column material contains compositions.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

F8385

Vendor name
and address

Teledyne e2v Semiconductors
Avenue De Rochepleine
BP 123
Saint Egreve CEDEX-38521, France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.