

.....REVISIONS

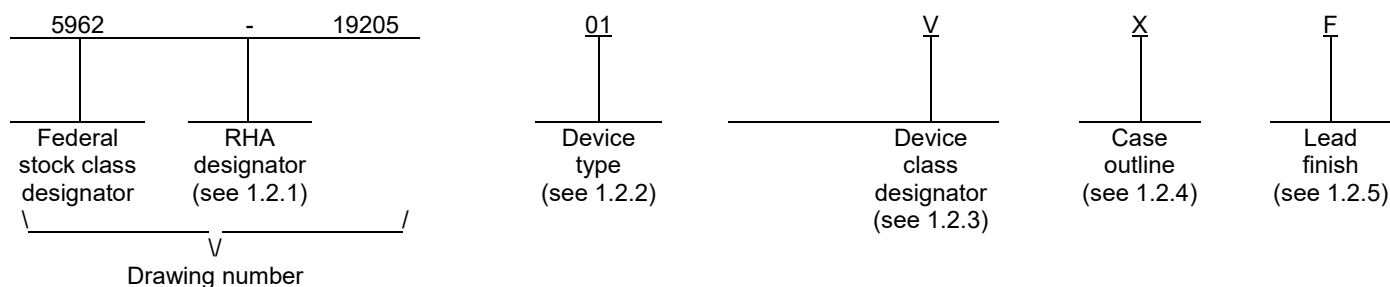
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED			
REV																		
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SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
REV STATUS OF SHEETS				REV														
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13
PMIC N/A				PREPARED BY Muhammad Akbar						DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime								
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Muhammad Akbar														
				APPROVED BY Thomas M Hess						MICROCIRCUIT, FLIP CHIP, 3.2 GHz SiGe BiCMOS 130nm, LOW POWER DUAL CHANNEL 12BIT 1.60 Gsps ANALOG TO DIGITAL CONVERTER (ADC) WITH LVDS DEMUX 1:1 OR DEMUX 1:2, MONOLITHIC SILICON								
				DRAWING APPROVAL DATE 19-07-18														
								REVISION LEVEL						SIZE A	CAGE CODE 67268	5962-19205		
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1. SCOPE

1.1 Scope. This drawing documents product assurance class level consisting of space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device class V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	EV12AD550A	Dual channel 12 bit 1.5 Gbps ADC with LVDS DEMUX
02	EV12AD550B	Dual channel 12 bit 1.6 Gbps ADC with LVDS DEMUX

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1.a	323	Ceramic land grid array (CLGA-Au pad termination)
Z	See figure 1.b	323	Ceramic column grid array (CCGA-Cu spiral column)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class V.

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1.3 Absolute maximum ratings. 1/ 2/ 3/ 4/ 5/

Absolute Maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
V _{CCA} Analog supply voltage	V _{CCA}	AGND – 0.3	3.8	V
V _{CCIOX} output supply voltage	V _{CCIOX}	GNDIO – 0.3	3.8	V
V _{CCD} digital supply voltage	V _{CCD}	DGND – 0.3	3.8	V
Analog input swing (mode ON)	A _{INP} - A _{INN} , B _{INP} - B _{INN}		4.8	V
Analog input swing (mode OFF)	A _{INP} - A _{INN} , B _{INP} - B _{INN}		1.2	V
Analog input voltage	A _{INP} , A _{INN} , B _{INP} , B _{INN}	AGND – 0.3	3.6	V
Clock input swing (mode ON)	[CLK - CLKN]		4	V _{PPD}
Clock input swing (mode OFF)	[CLK - CLKN]		1.2	V _{PPD}
Clock input voltage	CLK, CLKN	AGND – 0.3	3.75	V
SYNC input voltage	SYNC, SYNCN	AGND – 0.3	V _{CCA} + 0.3	V
SYNC input swing (Mode ON)	SYNC - SYNCN		4	V _{PPD}
SYNC input swing (Mode OFF)	SYNC - SYNCN		1.2	V _{PPD}
SPI input voltage	RSTN, SCLK, CSN, MOSI	DGND - 0.3	V _{CCD} + 0.3	V
VDIODEA input voltage	DIODEA	-0.9	0.3	V
Absolute maximum Junction Temperature	T _J		150°C	°C
Storage temperature	T _{STG}		-65°C to 150°C	°C
Soldering temperature	T _{SOL}		+225°C	°C
ESD (HBM)			2000V	V
ESD (CDM)			500V	V

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
- 3/ All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
- 4/ For cold sparing application, see application note AN1200A.
- 5/ T_J refers to the hot spot junction temperature on the die.

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1.4 Recommended operating conditions. 1/ 2/

Recommended Conditions of Use

Parameter	Symbol	Value		Unit
		Min	Max	
V _{CCA} Analog supply voltage	V _{CCA}		3.4	V
V _{CCIOX} output supply voltage 1	V _{CCIOX1}		3.4 or 2.5	V
V _{CCIOX} output supply voltage 2	V _{CCIOX2}		3.4	V
V _{CCD} digital supply voltage	V _{CCD}		3.4 or 2.5	V
Differential analog input Full swing	A _{INP} - A _{INN} , B _{INP} - B _{INN}		1.0	V _{PPD}
Differential analog input Full scale power	P _A , P _B		1.0	dBm
Differential clock input power	P _{CLK}		1.0	dBm
External clock frequency	f _c		≤ 3.2	GHz
SPI input voltage	V _{IL}		0	V
	V _{IH}		V _{CCD}	V
Operating temperature range for devices life time <10 years.	T _C ; T _J		-55°C < T _C , - T _J < 125°C	°C
Operating temperature range for devices life time <17 years.	T _C ; T _J		-55°C < T _C , - T _J < 110°C	°C

1/. V_{CCIOX1} = 2.5V and V_{CCD} = 2.5V can be used to reduce power consumption. Refer to Datasheet in section DEMUX 1:1 or 1:2 for more information.

2/. T_J refers to the hot spot junction temperature on the die.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figures 1.a and 1.b.

3.2.2 Terminal connections. The terminal connections, pin out table and function description shall be as specified respectively on figures 2.1, 2.2 and 2.3.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Input and output protection networks shall be as specified on Pinout table.

3.2.7 Thermal characteristic shall be as specified on figure 6.

3.2.8 Solderability test for BGA/CGA packages: Solderability test for case outline Y or Z for column grid array (CGA) or ball grid array(BGA) package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

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3.3 Electrical performance characteristics parameter limits. Unless otherwise specified herein, the electrical performance characteristics limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device class V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device class V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Handling precaution. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling. These components are categorized as ESDS class 1C in accordance with MIL-PRF-38535.

3.9 Mounting and storage recommendation. In order to avoid the risk of solderability (or wettability) it is recommended to mount the component onto the PCB within 2 years after the date of sealing.

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TABLE I. Electrical performance characteristics.

Test description	Symbol	Conditions -55°C ≤ T _J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Power Supply requirements:							
Analog power supply voltage	V _{CCA}		All	1,2,3	3.25	3.55	V
V _{CCIOX} output supply voltage 1	V _{CCIOX1}	V _{CCIOX1} = 3.4 V	All	1,2,3	3.25	3.55	V
		V _{CCIOX1} = 2.5 V	All	1,2,3	2.35	2.65	V
V _{CCIOX} output supply voltage 2	V _{CCIOX2}			1, 2, 3	3.25	3.55	V
Digital power supply voltage	V _{CCD}	V _{CCD} = 2.5 V	All	1,2,3	2.35	2.65	V
		V _{CCD} =3.4 V	All	1,2,3	3.25	3.55	
Power supply current (DEMUX 1:1)							
Analog power supply current	I _{CCA}	V _{CCA} = 3.4V	All	1	950	1110	mA
				2,3	930	1200	mA
Output supply current 1 (single rail)	I _{CCO1}	Reduced swing V _{CCIOH1} = 2.5 V	All	1	80	120	mA
				2, 3	63	150	
		Reduced swing V _{CCIOH2} = 3.4 V	All	1	80	120	mA
				2, 3	60	153	
Output supply current 2 (dual rail)	I _{CCO2}	Reduced swing V _{CCIOH2} = 3.4 V	All	1	50	75	mA
				2, 3	40	90	
Digital power supply Current (single and dual rail)	I _{CCD}	V _{CCD} = 2.5 V (dual rail)	All	1	140	190	mA
				2,3	130	200	
		V _{CCD} =3.4 V(single rail)	All	1	130	190	
				2, 3	120	195	
Power supply current (DEMUX 1:2)							
Analog power supply current	I _{CCA}	V _{CCA} = 3.4V	All	1	950	1110	mA
				2,3	930	1200	
Output supply current 1 (single rail)	I _{CCO1}	Reduced swing V _{CCIOH1} = 3.4 V	All	1	55	90	mA
				2,3	40	100	
		Reduced swing V _{CCIOH1} = 3.4 V		1	80	120	
				2, 3	60	153	
Output supply current 1 (dual rail)	I _{CCO1}	Reduced swing V _{CCIOH1} = 2.5 V	All	1	50	90	mA
				2,3	40	140	
		Reduced swing V _{CCIOH1} = 2.5 V		1	80	120	
				2,3	63	150	
Output supply current 2	I _{CCO2}	Reduced swing V _{CCIOH2} = 3.4 V	All	1	30	45	mA
				2,3	20	60	
		Reduced swing V _{CCIOH2} = 3.4 V		1	50	75	mA
				2,3	40	90	
Digital power supply Current (single and dual rail)	I _{CCD}	V _{CCD} = 2.5 V (dual rail)	All	1	115	170	mA
				2,3	95	180	
		V _{CCD} =3.4 V(single rail)	All	1	120	175	
				2,3	100	185	

See footnote end of the table

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TABLE I. Electrical performance characteristics – continued.

Test description	Symbol	Conditions -55°C ≤ T _J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Power supply current (Full standby mode)							
Analog power supply current	I _{CCA}		All	1	310	360	mA
				2,3	300	400	
Output supply current (DEMUX 1:1)	I _{CCO}		All	1	155	190	mA
				2,3	140	235	
Output supply current (DEMUX 1:2)	I _{CCO}		All	1	250	310	mA
				2,3	200	470	
Digital power supply current	I _{CCD}		All	1	45	85	mA
				2,3	40	95	
Power dissipation							
Power dissipation at DEMUX 1:1 (single rail)	P _D	V _{CCA} = V _{CCD} =V _{CCIOX} =3.4 V Reduced swing	All	1		5.0	W
				2,3		5.3	
Power dissipation at DEMUX 1:2 (single rail)				1		5.3	
				2,3		5.7	
Power dissipation at DEMUX 1:1 (dual rail)	P _D	V _{CCA} = V _{CCD} =V _{CCIOX2} =3.4 V or V _{CCD} =V _{CCIOX1} =2.5V Reduced swing	All	1		4.7	W
				2,3		5.0	
Power dissipation at DEMUX 1:2 (dual rail)				1		5.0	
				2,3		5.3	
Power dissipation at Full standby mode (DEMUX 1:1)	P _D	V _{CCA} = V _{CCD} =V _{CCIOX2} =3.4 V	All	1		2.1	W
				2,3		2.2	
Power dissipation at Full standby mode (DEMUX 1:2)	P _D	V _{CCA} = V _{CCD} =V _{CCIOX2} =3.4 V	All	1		2.5	W
				2,3		2.6	

See footnote end of the table

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TABLE I. Electrical performance characteristics – continued.

Test description	Symbol	Conditions -55°C ≤ T _J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	

ANALOG INPUTS

Common mode voltage	V _{INCM}		All	4	2.4 (typ) 4/		V
Analog differential input full scale Voltage	A _{INP} -A _{IN_N} B _{INP} -B _{IN_N}			4		1	V _{ppd}
Analog input leakage current	I _{IN}		All	4	40 (typ) 4/		μA
Crosstalk between analog inputs	Xtalk			4	80 (typ) 4/		dB

CLOCK INPUTS

Clock common mode voltage	V _{CCM}		All	4	2.4	2.75	V
Clock differential input power	P _{CLK}			4	-3	7	dBm
Clock differential input resistance	R _{CLK}		All	4	80	120	Ω
Clock slew rate	SR _{CLK}			4	8		GV/s
Clock Jitter	Jitter			4		100	fs _{rms}
Clock duty cycle	Duty cycle			4	45	55	%

SYNCTRIG INPUTS

SYNCTRIG common mode voltage	V _{ICM}		All	4,5,6	1.125	1.8	V
SYNCTRIG differential voltage	V _{IH} - V _{IL}		All	4,5,6	100	450	mVp

SPI INPUTS (RSTN, SCLK, CSN, MOSI)

CMOS Schmitt trigger low level threshold	V _{IL}		All	4		0.3V _{CCD}	V
CMOS Schmitt trigger high level threshold	V _{IH}		All	4	0.6V _{CCD}		

SPI OUTPUTS (MISO)

CMOS low level output voltage	V _{OL}		All	4		0.2V _{CCD}	V
CMOS high level output voltage	V _{OH}		All	4	0.8V _{CCD}		

LVDS OUTPUT

Full swing common mode voltage	V _{OCM}		All	4	1.20	1.55	V
Swing mode	V _{OH} - V _{OL}			4	230	480	mVp
Logic low	V _{OL}		All	4		1.30	V
Logic high	V _{OH}			4	1.40		

DC accuracy / Fs = 1.5GSps, Fin = 100MHz, -1dBFS

Dc offset			All	4	2045	2051	LSB
Integral Non Linearity	INL			4	5	5	LSB
INL rms	INL rms		All	4		1.60	LSB

See footnote end of the table

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TABLE I. Electrical performance characteristics – continued.

Test description	Symbol	Conditions -55°C ≤ T _J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
DYNAMIC Performance							
Spurious Free Dynamic range (output level -8dBFS)	SFDR	Fin= 1900MHz, NBW	All	9	69		dBFS
				10,11	66		
		Fin= 2980MHz, EBW		9	64		dBFS
				10,11	63		
Spurious Free Dynamic range (output level -12dBFS)	SFDR	Fin= 1900MHz, NBW	All	9	66		dBFS
				10,11	64		
		Fin= 2980MHz, EBW		9	67		dBFS
			10,11	63			
Total harmonic distortion (output level -8dBFS)	THD	Fin= 1900MHz, NBW	All	9	63		dBFS
				10,11	61		
		Fin= 2980MHz, EBW		9	62		dBFS
			10,11	58			
Total harmonic distortion (output level -12dBFS)	THD	Fin= 1900MHz, NBW	All	9	62		dBFS
				10,11	59		
		Fin= 2980MHz, EBW		9	62		dBFS
			10,11	60			
Signal to Noise ratio (output level -8dBFS)	SNR	Fin= 1900MHz, NBW	All	9	57		dBFS
				10,11	55		
		Fin= 2980MHz, EBW		9	54.5		dBFS
				10,11	53.5		
Signal to Noise ratio (output level -12dBFS)	SNR	Fin= 1900MHz, NBW	All	9	57		dBFS
				10,11	55.5		
		Fin= 2980MHz, EBW		9	55.5		dBFS
			10,11	54			
Signal to Noise and distortion (output level -8dBFS)	SINAD	Fin= 1900MHz, NBW	All	9	56		dBFS
				10,11	54		
		Fin= 2980MHz, EBW		9	54		dBFS
			10,11	51			
Signal to Noise and distortion (output level -12dBFS)	SINAD	Fin= 1900MHz, NBW	All	9	56.5		dBFS
				10,11	54		
		Fin= 2980MHz, EBW		9	55		dBFS
			10,11	53			
Effective number of Bits (output level -8dBFS)	ENOB	Fin= 1900MHz, NBW	All	9	9		Bit Fs
				10,11	8.8		
		Fin= 2980MHz, EBW		9	8.8		
				10,11	8.4		
Effective number of Bits (output level -12dBFS)	ENOB	Fin= 1900MHz, NBW	All	9	9.1		Bit Fs
				10,11	8.7		
		Fin= 2980MHz, EBW		9	9		
			10,11	8.6			

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TABLE I. Electrical performance characteristics – continued.

Test description	Symbol	Conditions -55°C ≤ T _J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	

Transient Characteristics

ADC code error rate at 1.5GSps <u>1/</u>	CER	CLK frequency 3GHz	All	9,10,11	10 ⁻¹²		
ADC code error rate at 1.5GSps <u>2/</u>		CLK frequency 2.5GHz		9,10,11	10 ⁻¹⁵		
Overvoltage recovery time	ORT		All	9,10,11	666		ps

Switching characteristics

External clock frequency	F _{CLK}		All	9,10,11		3200	MHz
Sampling frequency for performance <u>3/</u>	F _{S1:1}	DEMUX 1:1	All	9,10,11	200	1500	MSps
	F _{S1:2}	DEMUX 1:2	All	9,10,11	200	1600	MSps
Sampling frequency for operations <u>3/</u>	F _{S1:1}	DEMUX 1:1	All	9,10,11	200	1500	MSps
	F _{S1:2}	DEMUX 1:2	All	9,10,11	200	1600	MSps
Aperture delay	T _A	SDA disable	All	9,10,11	135 (Typ) <u>4/</u>		ps
Aperture delay tuning range(SDA enable)	T _A	SDA disable	All	9,10,11	120		ps

LVDS outputs

Rise time for data (20-80%)	T _r		All	9,10,11	165 (Typ) <u>4/</u>		ps
Fall time for data (20-80%)	T _f		All	9,10,11	165 (Typ) <u>4/</u>		ps
Output data skew within 1 port reference to data ready	T _{dxsk}		All	9,10,11	-23	+14.5	
SYNC pulse width	T _{SYNC}		All	9,10,11	16		T _{CLK}
SYCN to SYNCO propagation delay	T _{ODS}		All	9,10,11	1 (Typ) <u>4/</u>		ns
TRIG propagation delay	T _{ODT}		All	9,10,11	4.34		ns

1/ Output error amplitude > 128 LSB (3% of the full-scale). At F_s = 1.5 GSps, ambient temperature.

2/ Output error amplitude > 64 LSB (1.5% of the full-scale). At F_s = 1.25 GSps, ambient temperature.

3/ Performance only guaranteed at 1.5 GSps max in DEMUX 1:2 mode and 1.3 GSps max in DEMUX 1:1 mode although devices still exhibit very good performance at 1.6GSps.

4/ Typical (Typ) values listed for electrical parameters are tested in functional mode and may not be independently tested in production. This parameter is for informational purpose only.

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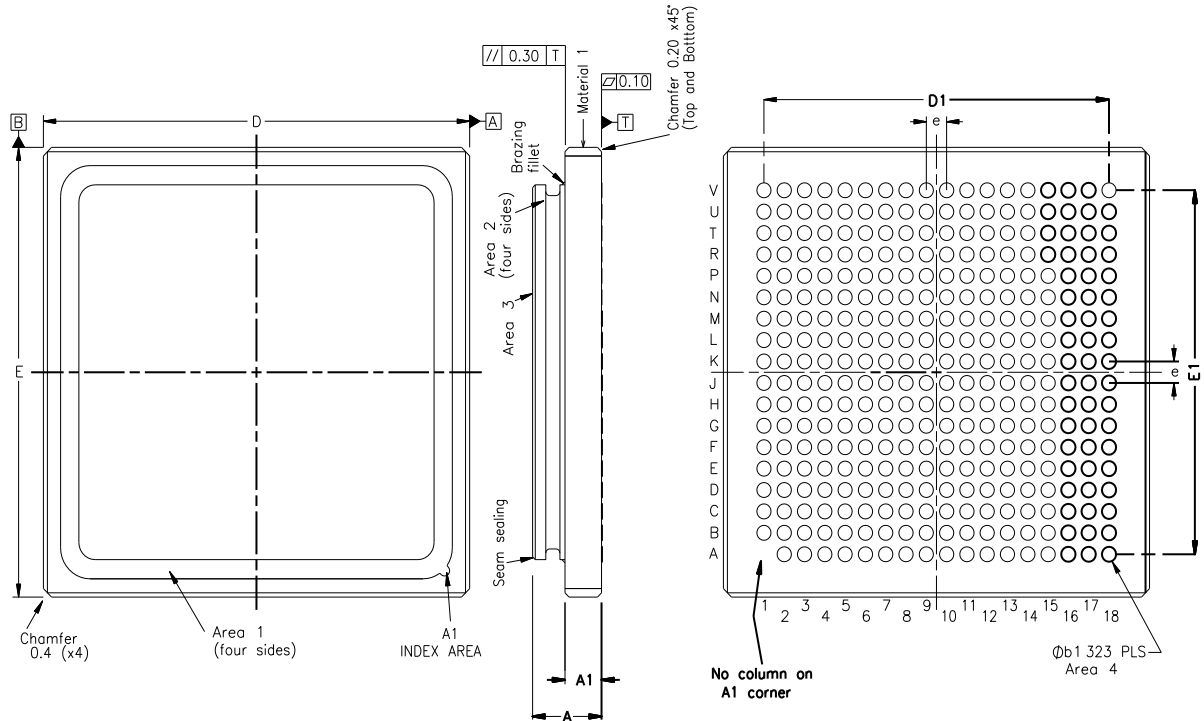
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Case outline. "X"
LGA323 top, bottom & side view (Seal ring connected to AGND)



Notes:

Area1 : Plating on ceramic for wall brazing. Finish is Gold 1.5 micron Min over Nickel

Area2 : Metal wall, finish is Gold 1.5 micron Min over Nickel

Area3 : Metal lid, finish is Nickel plating

Material 1 : Alumina nitride ceramic, black color

Area4 : Plating on ceramic for pin brazing, 323 places. Finish is Gold 1.5 micron Min over Nickel

Marking area : on top of lid (= above Area 3)

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	3.07	3.73	D1/E1	17.00 TYP	
A1	1.62	1.98	e	1.00 TYP	
b1	0.60	0.80			
D/E	20.8	21.2			

FIGURE 1.a Case outline "X"

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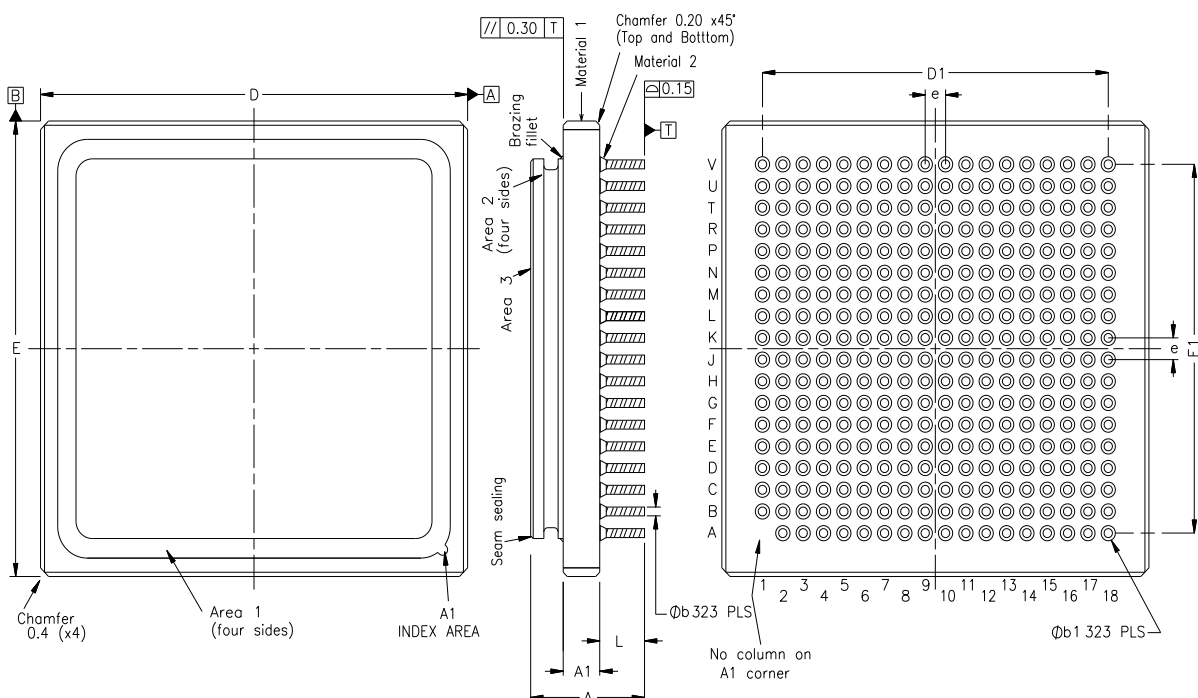
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Case outline "Z"

CCGA323 top, bottom & side view (seal ring connected to AGND)



Notes:

Area1 : Plating on ceramic for wall brazing. Finish is Gold 1.5 micron Min over Nickel

Area2 : Metal wall, finish is Gold 1.5 micron Min over Nickel

Area3 : Metal lid, finish is Nickel plating

Material 1 : Alumina nitride ceramic, black color

Material 2 : Assembly of columns on LGA using 63/37 Tin/Lead solder

Initial column core composition (prior to column wire manufacturing): Sn15-Pb85 (wt %).

Final column core composition (after column attach on CLGA packages): 55 ≤ Pb wt% ≤ 85

Copper spiral wrapped around columns with SnPb finish.

Marking area : on top of lid (= above Area 3)

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	5.01	6.10	D1/E1	17.00 TYP	
A1	1.62	1.98	e	1.00 TYP	
b	0.31	0.51	L	2.00	2.40
D/E	20.8	21.2	b1	0.60	0.80

FIGURE 1.b Case outline "Z"- continued.

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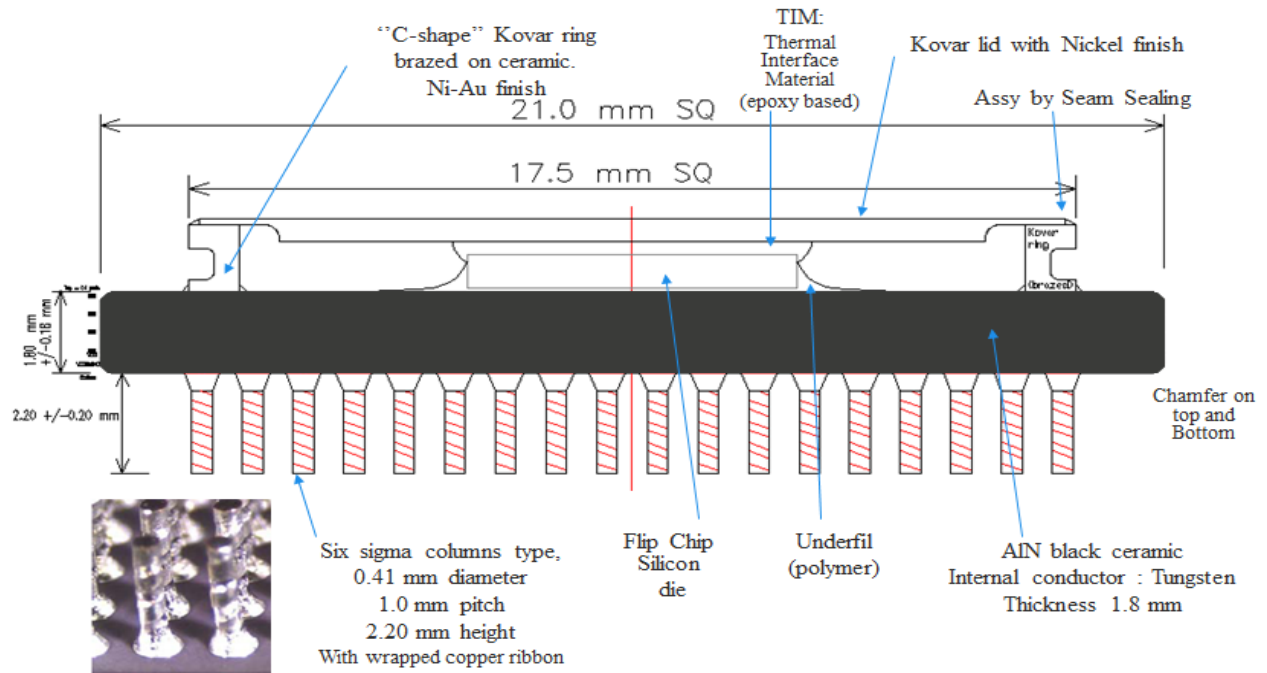
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Case outline "Z"
CCGA323 top, bottom & side view (seal ring connected to AGND)



Note: Total mass 7.5g including columns.

FIGURE 1.b Case outline "Z" - continued.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AGND	SYNC TRGP	AGND	AGND	AGND	AGND	AGND	CLK N	CLK P	AGND	AGND	AGND	AGND	AGND	DIODE_C	AGND	AGND	A
B	AGND	AGND	SYNC TRGN	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DIODE_A	AGND	AGND	B
C	SSO P	SSO N	AGND	AGND	AGND	AIN N	AIN P	AGND	AGND	AGND	AGND	BIN P	BIN N	AGND	AGND	AGND	SYNCO N	SYNCO P	C
D	AH11P	AH11N	AGND	AGND	CMIREFA	AGND	AGND	AGND	VCCA	VCCA	AGND	AGND	AGND	CMIREFB	AGND	AGND	BH11N	BH11P	D
E	AH10P	AH10N	AFU1P	AFU1N	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCA	VCCA	AGND	AGND	BFU1N	BFU1P	BH10N	BH10P	E
F	AH8P	AH8N	AH9P	AH9N	GNDIO	GNDIO	AGND	AGND	VCCA	VCCA	AGND	AGND	GNDIO	GNDIO	BH9N	BH9P	BH8N	BH8P	F
G	AH6P	AH6N	AH7P	AH7N	VCCIO H2A	GNDIO	VCCIO H2A	AGND	AGND	AGND	AGND	VCCIO H2B	GNDIO	VCCIO H2B	BH7N	BH7P	BH6N	BH6P	G
H	AH4P	AH4N	AH5P	AH5N	VCCIO H1A	GNDIO	VCCIO H1A	VCCA	AGND	AGND	VCCA	VCCIO H1B	GNDIO	VCCIO H1B	BH5N	BH5P	BH4N	BH4P	H
J	AH2P	AH2N	AH3P	AH3N	GNDIO	GNDIO	VCCIO H2A	AGND	VCCA	VCCA	AGND	VCCIO H2B	GNDIO	GNDIO	BH3N	BH3P	BH2N	BH2P	J
K	AH0P	AH0N	AH1P	AH1N	GNDIO	GNDIO	VCCIO H1A	VCCA	VCCD	GNDIO	VCCA	VCCIO H1B	GNDIO	GNDIO	BH1N	BH1P	BH0N	BH0P	K
L	ADRP	ADRN	AFU2P	AFU2N	VCCIO L1A	GNDIO	VCCIO L1A	GNDIO	VCCD	GNDIO	GNDIO	VCCIO L1B	GNDIO	VCCIO L1B	BFU2N	BFU2P	BDRN	BDRP	L
M	AL0P	AL0N	AL1P	AL1N	GNDIO	VCCIO L2A	GNDIO	VCCIO L2A	VCCIO L1A	VCCIO L1B	VCCIO L2B	GNDIO	VCCIO L2B	GNDIO	BL1N	BL1P	BL0N	BL0P	M
N	AL2P	AL2N	AL3P	AL3N	GNDIO	GNDIO	VCCIO L2A	GNDIO	GNDIO	GNDIO	GNDIO	VCCIO L2B	GNDIO	GNDIO	BL3N	BL3P	BL2N	BL2P	N
P	AL4P	AL4N	AL5P	AL5N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL5N	BL5P	BL4N	BL4P	P
R	AL6P	AL6N	AL7P	AL7N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL7N	BL7P	BL6N	BL6P	R
T	AL8P	AL8N	AL9P	AL9N	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	BL9N	BL9P	BL8N	BL8P	T
U	AL10P	AL10N	AL11P	AL11N	GNDIO	TESTA	VCCFUSEC	GNDIO	GNDIO	GNDIO	GNDIO	SCLK	RSTN	GNDIO	BL11N	BL11P	BL10N	BL10P	U
V	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	SCAN	VCCFUSEB	VCCFUSEA	GNDIO	GNDIO	GNDIO	MISO	MOSI	CSN	GNDIO	GNDIO	GNDIO	GNDIO	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

FIGURE 2.1. Terminal connections(top view through lid).

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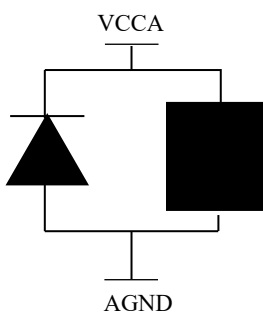
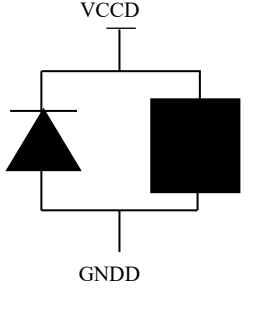
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Pinout Table CCGA323

Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
Power supplies					
AGND	A2, A4, A5, A6, A7, A8, A11, A12, A13, A14, A15, A17, A18, B1, B2, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B17, B18, C3, C4, C5, C8, C9, C10, C11, C14, C15, C16, D3, D4, D6, D7, D8, D11, D12, D13, D15, D16, E5, E6, E9, E10, E13, E14, F7, F8, F11, F12, G8, G9, G10, G11, H9, H10, J8, J11	Analog ground			
VCCA	D9, D10, E7, E8, E11, E12, F9, F10, H8, H11, J9, J10, K8, K11	Analog power supply			
GNDD	K10, L10	Digital ground			
VCCD	K9, L9	Digital power supply			
GNDIO	F5, F6, F13, F14, G6, G13, H6, H13, J5, J6, J13, J14, K5, K6, K13,	I/O ground			

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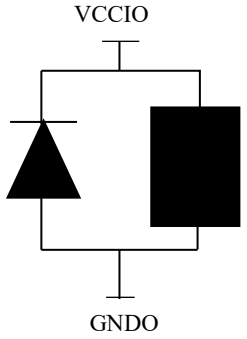
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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
	K14, L6, L8, L11, L13, M5, M7, M12, M14, N5, N6, N8, N9, N10, N11, N13, N14, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, U5, U8, U9, U10, U11, U14, V1, V2, V3, V4, V5, V9, V10, V11, V15, V16, V17, V18				
VCCIOH1	H5, H7, H12, H14, K7, K12	Output power supply for LVDS port high			
VCCIO L1	L5, L7, L12, L14, M9, M10	Output power supply for LVDS port low			
VCCIOH2	G5, G7, G12, G14, J7, J12	Output power supply for LVDS port high			
VCCIO L2	M6, M8, M11, M13, N7, N12	Output power supply for LVDS port low			
Clock					

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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
CLKP CLKN	A10, A9	Input clock signal	I		
AINP AINN	C7, C6	Analog input for ADC A	I		
BINP BINN	C12, C13	Analog input for ADC B	I		

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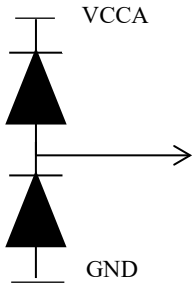
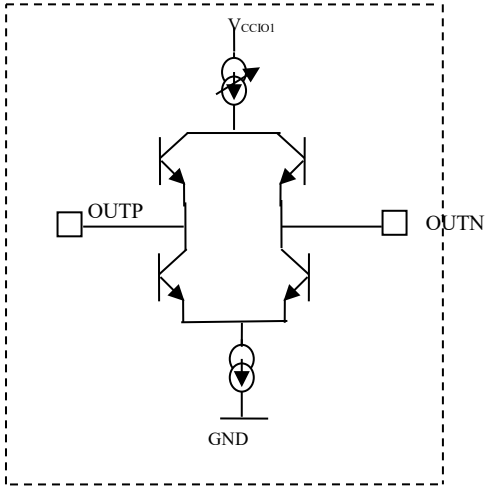
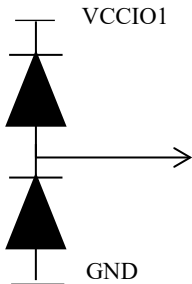
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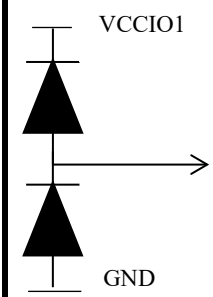
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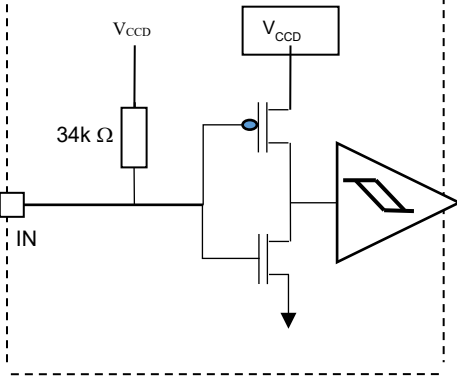
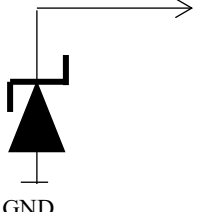
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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
CMIREFA CMIREFB	D5, D14	Input signal common mode reference for A and B cores. In AC coupling operation this output must be left floating (not used) In DC coupling operation, these pins provide an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O		
Digital output (LVDS)					
AH0P, AH0N AH1P, AH1N AH2P, AH2N AH3P, AH3N AH4P, AH4N AH5P, AH5N AH6P, AH6N AH7P, AH7N AH8P, AH8N AH9P, AH9N AH10P, AH10N AH11P, AH11N	K1, K2 K3, K4 J1, J2 J3, J4 H1, H2 H3, H4 G1, G2 G3, G4 F1, F2 F3, F4 E1, E2 D1, D2	High port channel A output data AH0 is the LSB, AH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O		
AFU1P, AFU1N	E3, E4	Channel A control bit 1	O		
AL0P, AL0N AL1P, AL1N AL2P, AL2N AL3P, AL3N AL4P, AL4N AL5P, AL5N AL6P, AL6N AL7P, AL7N AL8P, AL8N AL9P, AL9N AL10P, AL10N	M1, M2 M3, M4 N1, N2 N3, N4 P1, P2 P3, P4 R1, R2 R3, R4 T1, T2 T3, T4 U1, U2 U3, U4	Low port channel A output data AL0 is the LSB, AL11 is the MSB. (in DEMUX 1:1, this channel is disabled)	O		
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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
AL11P, AL11N					
AFU2P, AFU2N	L3, L4	Channel A control bit 2	O		
ADRP, ADRN	L1, L2	Channel A data ready	O		
BH0P, BH0N BH1P, BH1N BH2P, BH2N BH3P, BH3N BH4P, BH4N BH5P, BH5N BH6P, BH6N BH7P, BH7N BH8P, BH8N BH9P, BH9N BH10P, BH10N BH11P, BH11N	K18, K17 K16, K15 J18, J17 J16, J15 H18, H17 H16, H15 G18, G17 G16, G15 F18, F17 F16, F15 E18, E17 D18, D17	High port channel B output data BH0 is the LSB, BH11 is the MSB. (in DEMUX 1:1, this channel is enabled)	O		
BFU1P, BFU1N	E16, E15	Channel B control bit 1	O		
BL0P, BL0N BL1P, BL1N BL2P, BL2N BL3P, BL3N BL4P, BL4N BL5P, BL5N BL6P, BL6N BL7P, BL7N BL8P, BL8N BL9P, BL9N BL10P, BL10N BL11P, BL11N	M18, M17 M16, M15 N18, N17 N16, N15 P18, P17 P16, P15 R18, R17 R16, R15 T18, T17 T15, T16 U18, U17 U16, U15	Low port channel B output data BL0 is the LSB, BL11 is the MSB (in DEMUX 1:1, this channel is disabled)	O		
BFU2P, BFU2N	L16, L15	Channel B control bit 2	O		
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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
BDRP, BDRN	L18, L17	Channel B data ready	O		
SSOP, SSON	C1, C2	Slow Synchronization Output Clock	O		
SYNCO, SYNCON	C18, C17	Synchronization output signal	O		
SPI digital I/O (CMOS)					
CSN	V14	Chip Select signal (active low) Internal pull-up	I		
SCLK	U12	SPI clock Internal pull-up	I		
MOSI	V13	SPI Master Out Slave In Internal pull-up	I		
RSTN	U13	SPI asynchronous reset (active low) Internal pull-up	I		

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Pin label	Pin number	Description	I/O	Simplified electrical schematics	Input and output protection networks
MISO	V12	SPI Master In Slave Out	O		
DIGITAL INPUT (LVDS)					

SYNCTRIGP SYNCTRIGN	A3, B3	Differential input synchronization or trigger signal (LVDS) Active high signal	I		
Miscellaneous					

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scan	V6	RESERVED PIN Must be pulled-down with 10kΩ		
TESTA	U6	RESERVED PIN Should be left unconnected		
VCCFuseA, VCCFuseB VCCFuseC	V8 V7 U7	RESERVED PIN Should be left unconnected		

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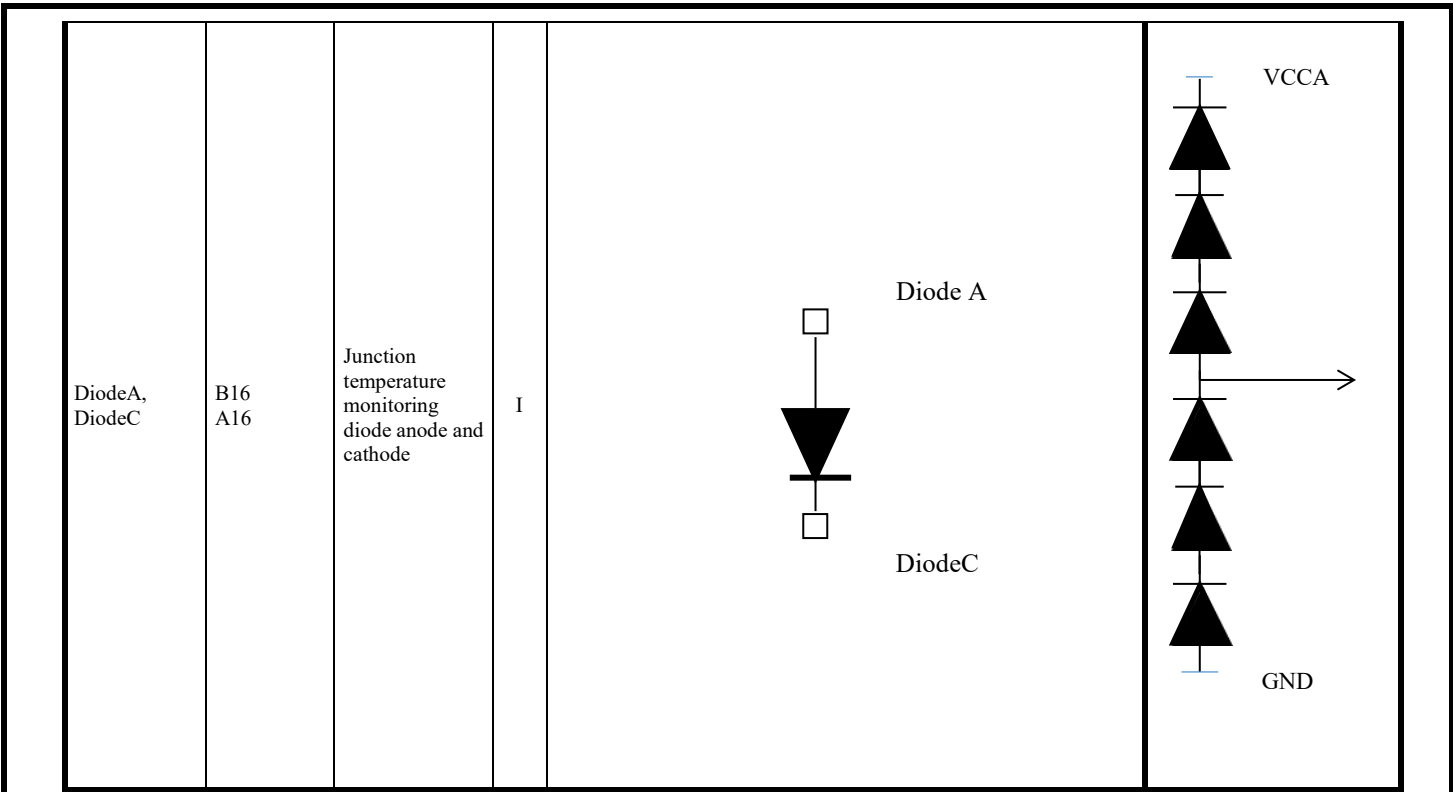


FIGURE 2.2. Pinout Functions

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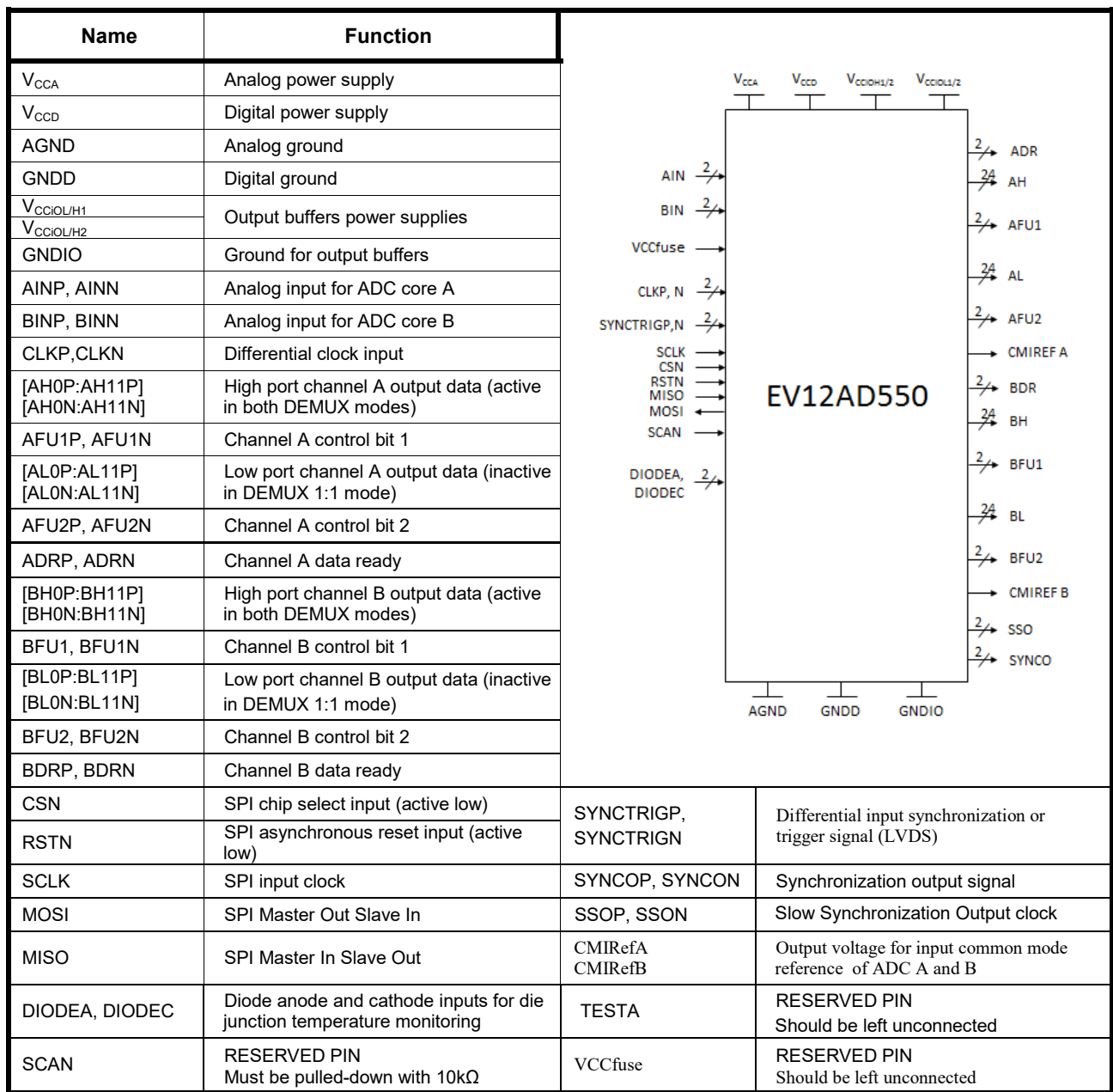


FIGURE 2.3. Functional diagram.

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Differential analog input	Voltage level	Binary MSB (bit 11).....LSB(bit 0) In-range
> + 500.125 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 500.125 mV + 500 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 0.125 mV - 0.125 mV	Mid-scale + ½ LSB Mid-scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
- 500 mV -500.125 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
< - 500.125 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0 0 0

FIGURE 3. Truth table.

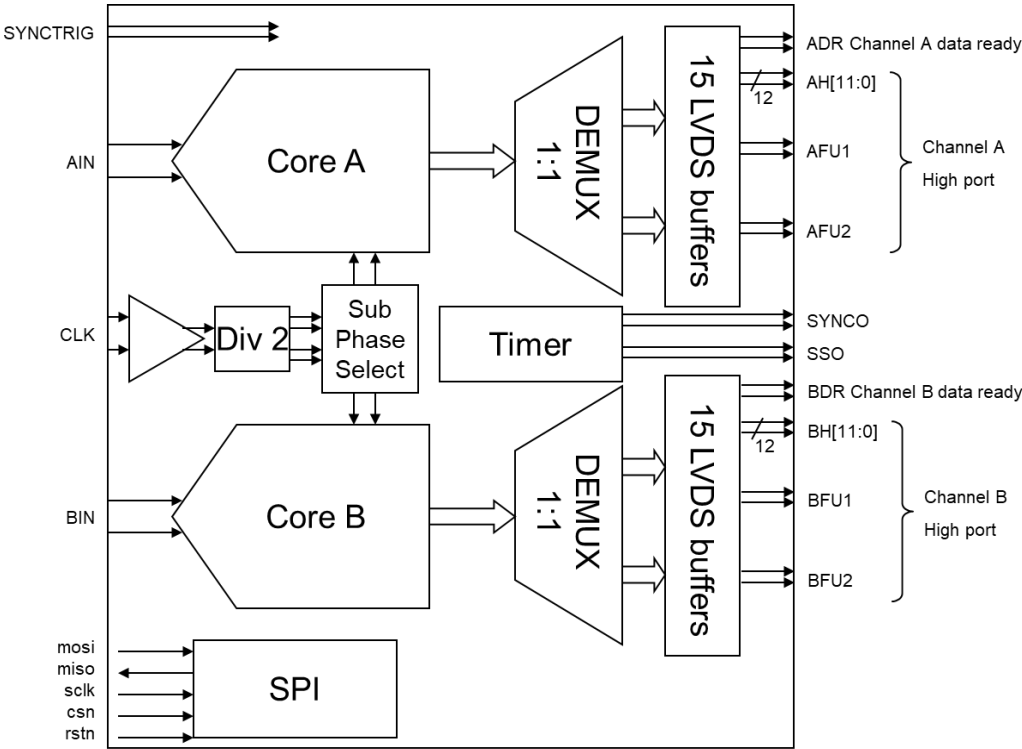


FIGURE 4. Functional diagram.(DEMUX 1:1)

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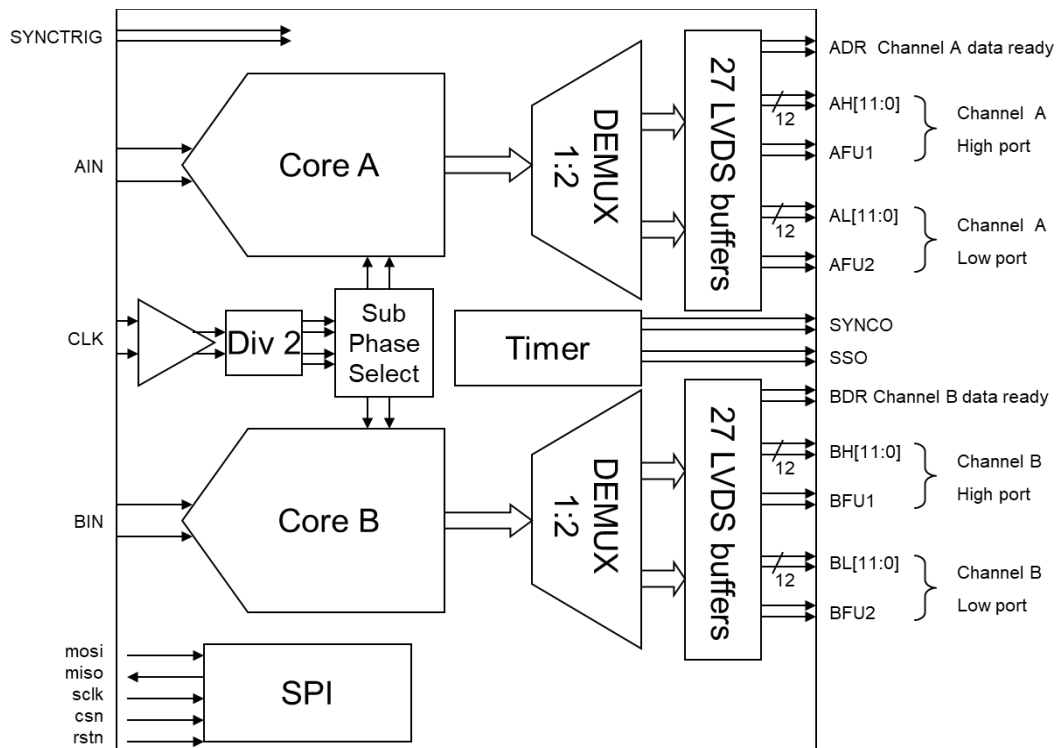


FIGURE 4. Functional diagram.(DEMUX 1:2)

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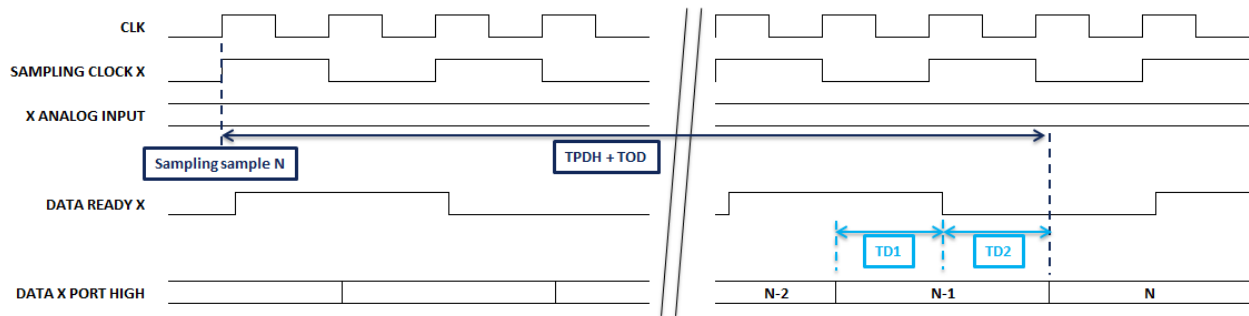
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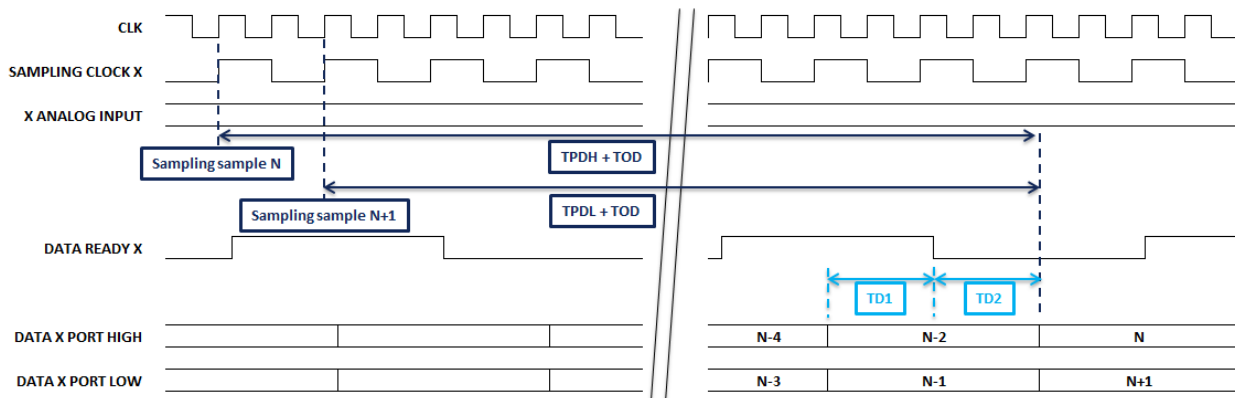
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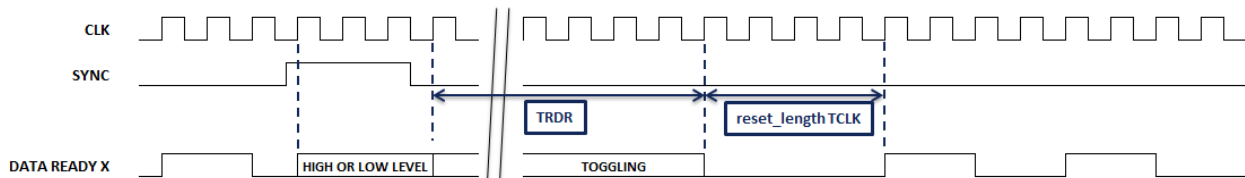
5.1. Timing Diagram in DEMUX 1:1



5.2. Timing Diagram in DEMUX 1:2



5.3. SYNC Timing Diagram in DEMUX 1 :1



Notes: In DEMUX 1:2 the only difference from the timing diagram above is the frequency of the data ready

5.4. SYNC edges forbidden zone

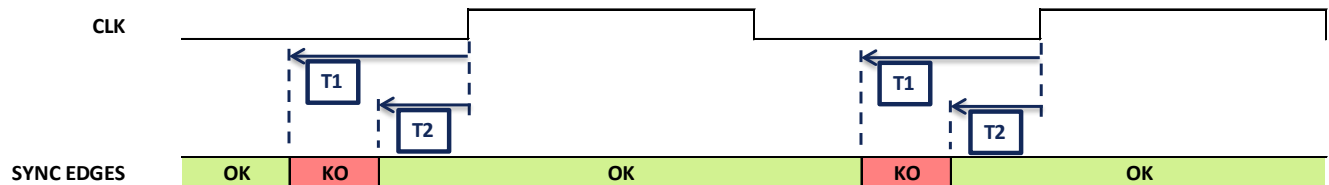


FIGURE 5. Timing waveforms.

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Parameter	Symbol	Value	Unit
Thermal Resistance	$\Theta_{\text{Junction-Bottom of columns}}$	4.7	°C/Watt
Thermal Resistance	$\Theta_{\text{Junction-top of lid}}^{(1)}$	3.9	°C/Watt
Thermal Resistance	$\Theta_{\text{Junction-Ambient}}^{(2)}$	17.5	°C/Watt
Delta Temp Hot Spot - Vdiode		+10	°C

Notes: Thermal resistances are calculated from hot spot, not from average temperature with a TIM of 310 micron thick and a thermal conductivity of 10 W/m/K

1. Infinite heat sink at top of lid. No dissipation through columns

2. Typical Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Board size 114.3 × 76.2 mm, 1.6 mm thickness

FIGURE 6. Thermal characteristics

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4. VERIFICATION

4.1 Sampling and inspection. For device class V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device class V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.2 Addition/deviation from MIL-PRF-38535.

- a. "Reverse Bias Burn-in" is not applicable on technology use for EV12AD550 product (SiGe Bipolar). However, 100% Static burn-in shall be performed in accordance with MIL-PRF-38535.
- b. Life test and dynamic burn-in test is performed at $T_A=85^{\circ}\text{C}$ and static burn-in is performed at $T_A=90^{\circ}\text{C}$ which corresponding to diode junction temperature of 134°C and hot spot junction temperature is 145°C .

4.3 Qualification inspection for device class V. Qualification inspection for device class V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device class V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 <u>1/</u>	1,2,3,7,8A, 8B,9,10,11 <u>1/</u>
2	Static burn-in I and II (method 1015)	Not required	Required
3	Dynamic burn-in (method 1015)	Required	Required
4	Final electrical parameters	1, 2, 3, 7, 8A, 8B, 9, 10, 11 <u>1/</u>	1,2,3,7,8A,8B,9, 10,11 <u>1/ 2/</u>
5	Group A test requirements <u>3/</u>	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
6	Group C end-point electrical parameters <u>3/</u>	1, 2, 3, 7, 8A, 8B, 9, 10, 11 <u>2/</u>	1,2,3,7,8A,8B, 9,10,11 <u>2/</u>
7	Group D end-point electrical parameters <u>4/</u>	1, 2, 3, 7, 8A, 8B 9,10,11	1, 2, 3, 7, 8A, 8B 9,10,11
8	Group E end-point electrical parameters <u>3/</u>	-	-
9	Column attach <u>5/</u>	1, 7, 9	1, 7, 9

1/ Indicates PDA applies to subgroup 1 and 7.

2/ For device class V, performance of delta limits shall be specified in table IIB.

3/ LGA packages only

4/ LGA package for all tests, plus CGA device for Column Pull and Salt Atmosphere.

5/ Solderability test shall be performed in accordance with TM 2003.

Table IIB. Burn-in and operating life test delta drift limits at +25°C. 1/ 2/

Test description	Test Symbol	Test limits	Units
Power dissipation (full swing) (DEMUX 1:1)	P _D	± 5 %	W
Power dissipation (Reduced swing) (DEMUX 1:2)	P _D	± 5 %	W
Power dissipation (Standby mode) (DEMUX 1:2)	P _D	± 5 %	W
Low level output voltage maximum	VOL_max	± 5 %	V
Low level output voltage minimum	VOL_min	± 5 %	V
SNR (DEMUX 1:2)	SNR	± 2 %	dBFS

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

2/ Unless otherwise specified, the measurement shall be performed at T_A = 23 ± 4°C, the characteristics, test methods, conditions and limits shall be as per the corresponding test defined in TABLE I. The drift value shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class V. Packing is not individual: Devices are packed within trays.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 General applications: The manufacturer is supplying this SMD device as a high-performance dual channel (S-band) capable 12 bit 1.6 GSps Analog to Digital Converter(ADC) . By providing full power input bandwidth(-3dB) upto 4.3GHz which allow direct digitization in S-band without frequency down-conversion. Synthetic Aperture Radar system will also be able to operate this ADC with reduced dynamic range at frequencies beyond 5GHz without frequency down-conversion. This device include multiple ADC chained synchronization features which help designing large array of synchronous ADC's to support the development of MIMO system using digital analog/digital beam forming techniques in active antennas.

This device can be used in many applications/systems but general applications are for Space application like earth observation SAR payload, Telecommunication satellite payload, Satellite datalinks, Satellite altimeter, satellite TWTA compensation system.

6.1.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device class V. Sources of supply for device class V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplying to this drawing with terminal lead finish mark "F". However, terminal lead finish F is tin (Sn) and lead (Pb) alloy with copper spiral column, and solder column material contains compositions of Sn= 15% and Pb=85% and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-18

Approved sources of supply for SMD 5962-19205 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-1920501VXC	F8385	EV12AD550AMLG-V
5962-1920501VZF	F8385	EV12AD550AMGC-V
5962-1920502VXC	F8385	EV12AD550BMLG-V
5962-1920502VZF	F8385	EV12AD550BMGC-V

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

F8385

Vendor name
and address

Teledyne e2V Semiconductors
Avenue De Rochepleine
BP 123
Saint Egreve CEDEX 38521, France

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