

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Five Year Review boilerplate update to current MIL-PRF-38535 requirements. – IIb	25-11-03	James R. Eschmeyer



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	A	A	A	A	A	A	A															
SHEET	23	24	25	26	27	28	29															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

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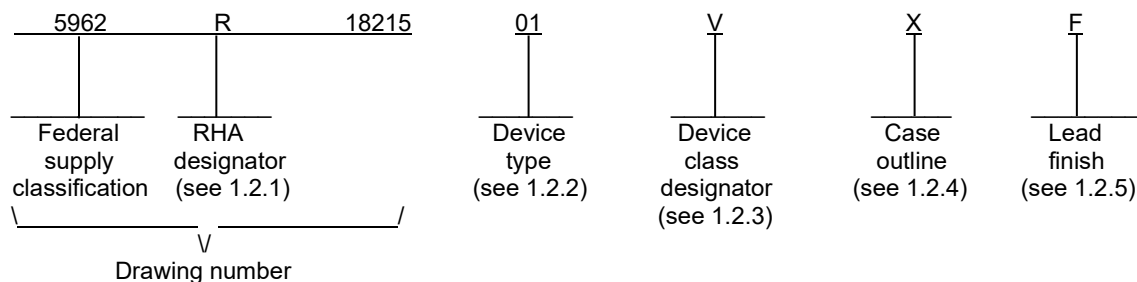
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY Gary Gross	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY Laura Leeper Branham			
	APPROVED BY James R. Eschmeyer	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, RADIATION HARDENED, 4M X 36-bit, 1.8 VOLT, 2-WORD AND 4-WORD BURST, SYNCHRONOUS STATIC RANDOM ACCESS MEMORY (SSRAM), MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 20-01-02			
AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE 67268	5962-18215

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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The devices type identify the circuit function as follows:

Device type	Generic number	Circuit function	Maximum Operating Frequency
01	2644KV18-250	4M X 36-bit rad-hard SSRAM 2-word burst w/ ODT	250 MHz
02	2645KV18-250	4M X 36-bit rad-hard SSRAM 4-word burst w/ ODT	250 MHz
03	1644KV18-250	4M X 36-bit rad-hard SSRAM 2-word burst w/o ODT	250 MHz
04	1645KV18-250	4M X 36-bit rad-hard SSRAM 4-word burst w/o ODT	250 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	165	Ceramic column grid array (CCGA) <u>1/</u>

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Terminal lead finish F is tin-lead alloy. Package case outline X solder column material is Sn = 20% and Pb = 80%.

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1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD}).....	-0.5 V dc to +2.9 V dc
Supply voltage range to outputs (V_{DDQ}).....	-0.5 V dc to V_{DD} <u>3/</u>
Reference supply voltage (V_{REF}).....	0.95 V dc <u>4/</u>
DC voltage range to any input.....	-0.5 V dc to V_{DD} +0.3 V dc <u>5/</u>
DC voltage range to any output pin in High-Z.....	-0.5 V dc to V_{DDQ} +0.3 V dc
Current into output (Low).....	20 mA
Storage temperature range.....	-65°C to +150°C
Case temperature range (T_C).....	-55°C to +125°C
Maximum junction temperature (T_J).....	150°C <u>6/</u>
Lead temperature (soldering, 10 seconds).....	+260°C
Thermal resistance, junction-to-case (θ_{JC}).....	8.6°C/W <u>7/</u>
Maximum power dissipation (P_D):	
Device 01.....	3.51 W
Device 02.....	3.44 W
Device 03.....	2.70 W
Device 04.....	2.68 W
Maximum operating supply current ($V_{DD} + V_{DDQ}$) = I_{DD} :	
Device 01.....	1850 mA
Device 02.....	1810 mA
Device 03.....	1422 mA
Device 04.....	1412 mA
Maximum operating frequency (devices 01 – 04).....	250 MHz

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}).....	1.7 V dc to 1.9 V dc
Supply voltage to outputs (V_{DDQ}).....	1.4 V dc to V_{DD} <u>3/</u>
Supply voltage (V_{SS}).....	0 V
Input high voltage range (V_{IH}).....	V_{REF} +0.1 V dc to V_{DDQ} +0.3 V dc <u>4/ 5/</u>
Input low voltage range (V_{IL}).....	-0.3 V dc to V_{REF} -0.1 V dc <u>4/ 5/</u>
Case operating temperature range (T_C).....	-55°C to +125°C <u>6/</u>

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s).....	100 krad(Si) <u>8/</u>
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.4).....	≤ 120 MeV-cm ² /mg <u>7/</u>
SEU observed at Onset LET (see 4.4.4.4).....	≤ 0.05 MeV-cm ² /mg <u>7/</u>
(saturated cross section = 7.2×10^{-8} cm ²)	
Single event upset (SEU) error rate	= 3.34×10^{-7} errors/bit-day) <u>7/ 9/</u>
Dose rate induced upset.....	= 1.0×10^9 rad(Si)/sec <u>7/</u>
Dose rate induced latch-up (survivability).....	= 3.0×10^9 rad(Si)/sec <u>7/</u>
Neutron irradiation.....	= 5.0×10^{14} n/cm ² <u>7/</u>

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ $V_{DDQ} \leq V_{DD}$ at all times.

4/ $V_{REF}(\text{Min}) = 0.68$ V or $0.46 * V_{DDQ}$, whichever is larger. $V_{REF}(\text{Max}) = 0.95$ V or $0.54 * V_{DDQ}$.

5/ Overshoot: $V_{IH(AC)} < V_{DDQ} + 0.85$ V (Pulse width $< t_{CYC}/2$), Undershoot: $V_{IL(AC)} > -1.5$ V (Pulse width $< t_{CYC}/2$).

6/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

7/ Tested initially and after any design or process changes which may affect this parameter. Contact the device manufacturer for detailed lot information.

8/ Manufacturer supplying device types 01-04 have been tested total ionizing dose (TID) test in accordance with MIL-STD-883, method 1019, condition A to a maximum total ionizing dose (TID) level of 200 krad(Si). However, device types 01-04 are marked to standard 100 krad(Si) of RHA TID level R.

9/ For single event upset error rate = 3.34×10^{-7} errors/bit-day (SEU rate 50.5 device-day/events) consider SEU error rate calculation CREME96 Geosynchronous orbit.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org>.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 95 - Book Three Registered and Standard Outlines for Solid State and Related Products

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org>.)

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - Test Access Port and Boundary-Scan Architecture

(Copies of these documents are available online at <https://standards.ieee.org/standard/index.html>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.1.1 Solderability test for CGA packages. Solderability testing for case outline X for CGA packages have been verified during the solder column attachment process in accordance with method 2003 of MIL-STD-883.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Output load and V_{OH}/V_{OL} test circuit. The output load and V_{OH}/V_{OL} test circuit shall be as specified on figure 4.

3.2.5 Block diagram. The block diagram shall be as specified on figure 5.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in Appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

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3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 IEEE 1149.1 Serial Boundary Scan (JTAG). The SRAMs described in this document incorporate a serial boundary scan Test Access Port (TAP). This feature is fully compliant with IEEE Standard 1149.1-2001. The TAP operates using standard 1.8V I/O logic levels.

3.10.1 Disabling the JTAG feature. It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied to LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively connect to V_{DD} through a pull-up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 1.7 V ≤ V _{DD} ≤ 1.9 V 1.4 V ≤ V _{DDQ} ≤ V _{DD} unless otherwise specified <u>1/</u> <u>2/</u> <u>3/</u>	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output HIGH Voltage <u>4/</u> <u>5/</u>	V _{OH1}	I _{OH} = -0.1 mA, 50 Ω impedance See figure 4	1, 2, 3	All	V _{DDQ} -0.20	V _{DDQ}	V
Output LOW Voltage <u>4/</u> <u>5/</u>	V _{OL1}	I _{OL} = 0.1 mA, 50 Ω impedance See figure 4	1, 2, 3	All	V _{SS}	0.20	V
Output HIGH Voltage <u>6/</u>	V _{OH2}	I _{OH} = -2.0 mA, 50 Ω impedance See figure 4	1, 2, 3	All	V _{DDQ} /2 -0.12	V _{DDQ} /2 +0.12	V
Output LOW Voltage <u>7/</u>	V _{OL2}	I _{OL} = 2.0 mA, 50 Ω impedance See figure 4	1, 2, 3	All	V _{DDQ} /2 -0.12	V _{DDQ} /2 +0.12	V
Input HIGH Voltage <u>8/</u>	V _{IH}		1, 2, 3	All	V _{REF} +0.1	V _{REF} +0.3	V
Input LOW Voltage <u>8/</u>	V _{IL}		1, 2, 3	All	-0.3	V _{REF} - 0.1	V
Input Reference Voltage <u>9/</u>	V _{REF}	Typical value = 0.75 V	1, 2, 3	All	0.68	0.95	V
Input Leakage Current	I _X	GND ≤ V _I ≤ V _{DDQ}	1, 2, 3	All	-20	20	μA
Output Leakage Current	I _{OZ}	GND ≤ V _I ≤ V _{DDQ} , output disabled	1, 2, 3	All	-20	20	μA
V _{DD} Operating Supply Current	I _{DD}	V _{DD} = max, I _{OUT} = 0 mA f = f _{MAX} = 1/t _{CYC}	1, 2, 3	01, 03		1080	mA
				02, 04		1040	
Automatic CE Power-Down Current	I _{SB1}	V _{DD} = max, both ports deselected, inputs static, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} f = f _{MAX} = 1/t _{CYC}	1, 2, 3	01, 03		390	mA
				02, 04		390	
Input Capacitance <u>10/</u>	C _{IN}	T _A = 25°C, f = 1 MHz, V _{DD} = 1.8 V, V _{DDQ} = 1.5 V See 4.4.1d	4	All		10	pF
Clock Input Capacitance <u>10/</u>	C _{CLK}		4	All		10	pF
Output Capacitance <u>10/</u>	C _{OUT}		4	All		10	pF
Functional Tests	F _T	T _A = 25°C, see 4.4.1b	7, 8A, 8B	All			
K Clock Cycle Time	t _{CYC}	See Figure 5 as applicable. <u>11/</u> <u>12/</u>	9, 10, 11	All	4.0	8.4	ns
Input Clock (K/ $\bar{K}$) High	t _{KH}		9, 10, 11	All	1.6	---	ns
Input Clock (K/ $\bar{K}$) Low	t _{KL}		9, 10, 11	All	1.6	---	ns
K Clock Rise to K Clock Rise (rising edge to rising edge)	t _{KH$\bar{K}$H}		9, 10, 11	All	1.8	---	ns
Address Setup to K Clock Rise	t _{SA}		9, 10, 11	All	0.5	---	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 1.7 V ≤ V _{DD} ≤ 1.9 V 1.4V ≤ V _{DDQ} ≤ V _{DD} unless otherwise specified <u>1/ 2/ 3/</u>	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Control Setup to K Clock Rise (RPS, WPS)	t _{SCDDR}	See Figure 5 as applicable. <u>11/ 12/</u>	9, 10, 11	All	0.5	---	ns
Double Data Rate Control Setup after Clock (K/ $\bar{K}$) Rise (BWS ₀ , BWS ₁ , BWS ₂ , BWS ₃)	t _{SCDDR}		9, 10, 11	All	0.5	---	ns
D _[X:0] Setup to Clock (K/ $\bar{K}$) Rise	t _{SD}		9, 10, 11	All	0.5	---	ns
Address Hold after K Clock Rise	t _{HA}		9, 10, 11	All	0.5	---	ns
Control Hold after to K Clock Rise (RPS, WPS)	t _{HC}		9, 10, 11	All	0.5	---	ns
Double Data Rate Control Hold after Clock (K/ $\bar{K}$) Rise (BWS ₀ , BWS ₁ , BWS ₂ , BWS ₃)	t _{HCDDR}		9, 10, 11	All	0.5	---	ns
D _[X:0] Hold after Clock (K/ $\bar{K}$)	t _{HD}		9, 10, 11	All	0.5	---	ns
K/ $\bar{K}$ Clock Rise to Data Valid	t _{CO}		9, 10, 11	All	---	0.85	ns
Data Output Hold after Output K/ $\bar{K}$ Clock Rise (Active to Active)	t _{DOH}		9, 10, 11	All	-0.85	---	ns
K/ $\bar{K}$ Clock Rise to Echo Clock	t _{CCQO}		9, 10, 11	All	---	0.85	ns
Echo Clock Hold after C/ $\bar{C}$ Clock Rise	t _{CQOH}		9, 10, 11	All	-0.85	---	ns
Echo Clock High to Data Valid	t _{CQD}		9, 10, 11	All	---	0.50	ns
Echo Clock High to Data Invalid	t _{CQDOH}		9, 10, 11	All	-0.30	---	ns
Output Clock (CQ/ $\bar{CQ}$) High <u>13/</u>	t _{CQH}		9, 10, 11	All	1.55	---	ns
CQ Clock High to $\bar{CQ}$ Clock Rise (rising edge to rising edge) <u>13/</u>	t _{CQH$\bar{CQ}$H}		9, 10, 11	All	1.55	---	ns
Clock (K/ $\bar{K}$) Rise to High-Z (Active to High-Z) <u>14/ 15/</u>	t _{CHZ}		9, 10, 11	All	---	0.45	ns
Clock (K/ $\bar{K}$) Rise to Low-Z <u>8/ 14/ 15/</u>	t _{CLZ}		9, 10, 11	All	-0.45	---	ns
Echo Clock High to QLVD Valid <u>16/</u>	t _{QVLD}		9, 10, 11	All	-0.5	0.5	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 1.7 V ≤ V _{DD} ≤ 1.9 V 1.4V ≤ V _{DDQ} ≤ V _{DD} unless otherwise specified <u>1/</u> <u>2/</u> <u>3/</u>	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock Phase Jitter	t _{KC Var}	See Figure 5 as applicable. <u>11/</u> <u>12/</u>	9, 10, 11	All	---	0.20	ns
DLL Lock Time (K)	t _{KC Lock}		9, 10, 11	All	20	---	μs
K static to DLL reset	t _{KC Reset}		9, 10, 11	All	30	---	ns

1/ All voltage is in reference to ground.

2/ Power up: Assumes a linear ramp from 0 V to V_{DD(min)} within 200 ms. During this time, V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

3/ RHA parts supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ Outputs are impedance controlled. I_{OH} = -(V_{DDQ}/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.

5/ Outputs are impedance controlled. I_{OL} = (V_{DDQ}/2)/(RQ/5) for values of 175 Ω ≤ RQ ≤ 350 Ω.

6/ Tested limits for V_{OH2} are MIN = 1.3 V, MAX = 1.5 V for 50 Ω termination and -2 mA output current.

7/ Tested limits for V_{OL2} are MIN = 0.0 V, MAX = 0.3 V for 50 Ω termination and 2 mA output current.

8/ Parameters guaranteed by characterization but not production tested.

9/ V_{REF(min)} = 0.68 V or 0.46 * V_{DDQ}, whichever is larger, V_{REF(max)} = 0.95 V or 0.54 * V_{DDQ}, whichever is smaller.

10/ Tested initially and after any design or process changes that may affect these parameters.

11/ Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, V_{REF} = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 4(a), AC test loads.

12/ When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timing of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.

13/ These parameters are extrapolated from the input timing parameters (t_{KHKH} - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps (t_{KC Var}) is already included in the t_{KHKH}). These parameters are only guaranteed by design and are not tested in production.

14/ t_{CHZ} and t_{CLZ} are specified with a load capacitance of 5 pF as in Figure 4(b), AC test loads. Transition is measured ±100 mV from steady-state voltage.

15/ At any voltage and temperature t_{CHZ} is < t_{CLZ} and t_{CHZ} is < t_{CO}.

16/ t_{QVLD} spec is applicable to both rising and falling edges of QVLD signal.

TABLE IB. SEP Test Limits. 1/ 2/

Device type	Single Event Upset <u>3/</u> V _{DD} = 1.7 V, V _{DD} = 1.4 V		Single Event Latch-up (SEL) test Bias V _{DD} = 1.9 V, V _{DDQ} = 1.9 V
	Single event upsets occurs at Onset LET <u>5/</u>	Maximum device Cross section (cm ²)	Effective LET No SEL occurs <u>4/</u>
All	0.13 MeV/(mg/cm ²)	7.2 x 10 ⁻⁸	120 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Test temperature T_A = +25°C ±10°C.

4/ Worst case test temperature T_A = +125°C ±10°C.

5/ For single event upset error rate = 3.34 x 10⁻⁷ errors/bit-day (SEU rate 50.5 device-day/events) consider Geosynchronous orbit CREME96.

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Case outline X

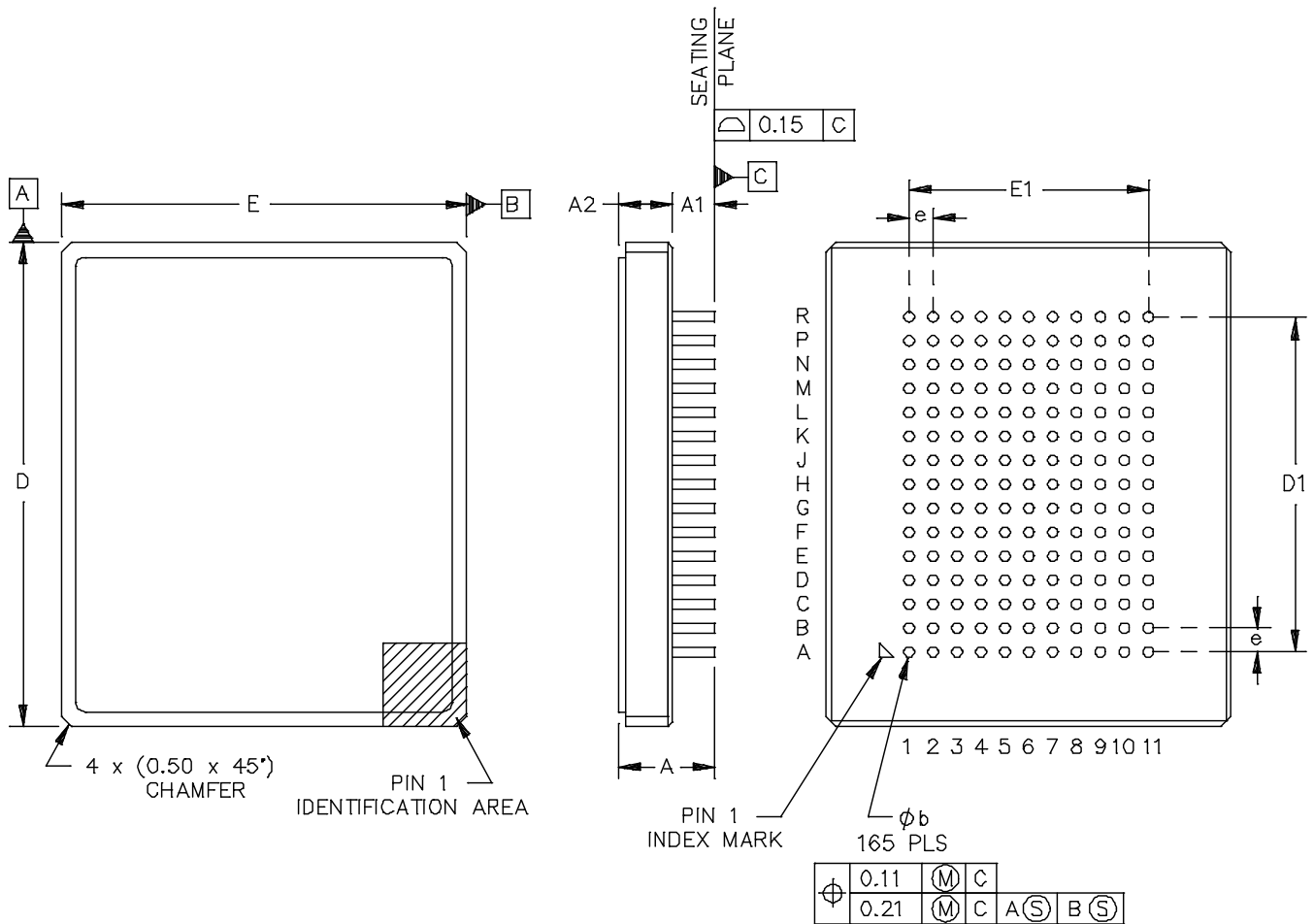


FIGURE 1. Case outline.

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Case outline X – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.38		0.212
A1	2.11	2.31	0.083	0.091
A2	2.59	3.07	0.102	0.121
b	0.43	0.59	0.017	0.023
e	1.27 BSC NOM		0.050	
D	24.75	25.25	0.974	0.994
D1	17.78 BSC NOM		0.700	
E	20.79	21.21	0.819	0.835
E1	12.70 BSC NOM		0.500	
N	165			

NOTES:

1. Index area: a notch or pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Reference Outline MO-158, Variable BE-1 in JEP 95 for lead pattern.

FIGURE 1. Case outline – Continued.

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Case outline X

Device types 01 – 04											
	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	1/	A	$\overline{\text{WPS}}$	$\overline{\text{BWS}}_2$	$\overline{\text{K}}$	$\overline{\text{BWS}}_1$	$\overline{\text{RPS}}$	A	A	CQ
B	Q27	Q18	D18	A	$\overline{\text{BWS}}_3$	K	$\overline{\text{BWS}}_0$	A	D17	Q17	Q8
C	D27	Q28	D19	V _{SS}	A	NC	A	V _{SS}	D16	Q7	D8
D	D28	D20	Q19	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q16	D15	D7
E	Q29	D29	Q20	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q13	D13	D5
H	$\overline{\text{DOFF}}$	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	D31	Q31	D23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	D10	Q1	D2
N	D34	D26	Q25	V _{SS}	A	A	A	V _{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

1/ Terminal A2 assignments by device type:

Device type	Terminal symbol
01	A
02, 03, 04	NC/288M

FIGURE 2. Terminal connections.

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Pin Definitions

Pin	Name	Function
D _[x:0]	Input-Synchronous	Data Input Signals. Sampled on the rising edge of K and $\bar{K}$ clocks during valid write operations. Device types 01 and 02: D _[35:0] .
$\overline{WPS}$	Input-Synchronous	Write Port Select – Active LOW. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores D _[x:0] .
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	Byte Write Select 0, 1, 2 and 3 – Active LOW. Sampled on the rising edge of the K and $\bar{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. Device types 01 and 02: S ₀ controls D _[8:0] , S ₁ controls D _[17:9] . All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	Address Inputs. Sampled on the rising edge of the K (Read address) and $\bar{K}$ (Write address) clocks during active read and write operations for device type 01 whereas sampled on the rising edge of the K clock during active read and write operations for device type 02. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2 M x 36 (2 arrays each of 1 M x 36) for device type 01 and 2 M x 36 (4 arrays each of 512 K x 36) for device type 02. Therefore, 20 address inputs are needed to access the entire memory array of device type 01 and 19 address inputs for device type 02. These inputs are ignored when the appropriate port is deselected.
Q _[x:0]	Output-Synchronous	Data Output Signals. These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of the K and $\bar{K}$ clocks during read operations. On deselecting the read port, Q _[x:0] are automatically tri-stated. Device types 01 and 02: Q _[35:0] .
$\overline{RPS}$	Input-Synchronous	Read Port Select – Active LOW. Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. De-asserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the K clock. Each read access consists of a burst of two sequential transfers for device type 01 whereas a burst of four sequential transfers for device type 02.
QVLD	Valid Output Indicator	Valid Output Indicator. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
ODT	On-Die Termination Input Pin	On-die Termination Input. This pin is used for On-Die termination of the input signals. ODT range selection is made during power up initialization. A low on this pin selects a low range that follows RQ /3.33 for 175 Ω $\leq$ RQ $\leq$ 350 Ω (where RQ is the resistor tied to ZQ pin). A high on this pin selects a high range that follows RQ /1.66 for 175 Ω $\leq$ RQ $\leq$ 250 Ω (where RQ is the resistor tied to ZQ pin). When left floating, a high range termination value is selected by default. On-Die Termination (ODT) feature is supported for D _[x:0] , BWS _[x:0] , and K/ $\bar{K}$ inputs.
K	Input Clock	Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through Q _[x:0] . All accesses are initiated on the rising edge of K.
$\bar{K}$	Input Clock	Negative Input Clock Input. $\bar{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through Q _[x:0] .
CQ	Echo Clock	Synchronous Echo Clock Outputs. This is a free running clock and is synchronized to the input clock (K) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics (Table IA).
$\overline{CQ}$	Echo Clock	Synchronous Echo Clock Outputs. This is a free running clock and is synchronized to the input clock ($\bar{K}$) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics (Table IA).

FIGURE 2. Terminal connections – Continued.

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Pin Definitions – Continued.

Pin	Name	Function
ZQ	Input	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. CQ , $\overline{CQ}$, and $Q_{[X:0]}$ output impedance are set to $0.2 \times RQ$, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ} , which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	DLL Turn Off- Active LOW. Connecting this pin to ground turns off the DLL inside the device. For normal operation, this pin can be connected to a pull up through a 10 K Ω or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR-I timing.
TDO	Output	Test Data Out (TDO) for JTAG.
TCK	Input	Test Clock (TCK) Pin for JTAG.
TDI	Input	Test Data In (TDI) Pin for JTAG.
TMS	Input	Test Mode Select (TMS) Pin for JTAG
NC, NC/288M	N/A	Not Connected to the Die. Can be tied to any voltage level.
V_{REF}	Input-Reference	Reference Voltage Input. Static input used to set reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	Power Supply Inputs to the Core of the Device.
V_{SS}	Ground	Ground for the Device.
V_{DDQ}	Power Supply	Power Supply Inputs for the Outputs of the Device.

FIGURE 2. Terminal connections – Continued.

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Truth Table for device types 01 and 03 1/ 2/ 3/ 4/ 5/ 6/

Operation	K	RPS	WPS	DQ	DQ
Write Cycle: Load address on the rising edge of $\bar{K}$ clock; input write data on K and $\bar{K}$ rising edges.	L - H	X	L	D(A) at K(t)↑	D(A + 1) at $\bar{K}$ (t) ↑
Read Cycle: Load address on the rising edge of K clock; wait one and a half cycle; read data on $\bar{K}$ and K rising edges.	L - H	L	X	Q(A) at K(t + 2) ↑	Q(A + 1) at $\bar{K}$ (t + 2) ↑
NOP: No Operation	L - H	H	H	D = X Q = High Z	D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

Write Cycle Descriptions for device types 01 and 03 1/ 7/

BWS ₀	BWS ₁	BWS ₂	BWS ₃	K	$\bar{K}$	Comments
L	L	L	L	L - H	-	During the data portion of a write sequence all four bytes (D _[35:0]) are written into the device.
L	L	L	L	-	L - H	During the data portion of a write sequence all four bytes (D _[35:0]) are written into the device.
L	H	H	H	L - H	-	During the data portion of a write sequence only the lower byte (D _[8:0]) is written into the device, D _[35:9] remains unaltered.
L	H	H	H	-	L - H	During the data portion of a write sequence only the lower byte (D _[8:0]) is written into the device, D _[35:9] remains unaltered.
H	L	H	H	L - H	-	During the data portion of a write sequence only the byte (D _[17:9]) is written into the device, D _[8:0] and D _[35:18] remain unaltered.
H	L	H	H	-	L - H	During the data portion of a write sequence only the byte (D _[17:9]) is written into the device, D _[8:0] and D _[35:18] remain unaltered.
H	H	L	H	L - H	-	During the data portion of a write sequence only the byte (D _[26:18]) is written into the device, D _[17:0] and D _[35:27] remain unaltered.
H	H	L	H	-	L - H	During the data portion of a write sequence only the byte (D _[26:18]) is written into the device, D _[17:0] and D _[35:27] remain unaltered.
H	H	H	L	L - H	-	During the data portion of a write sequence only the lower byte (D _[35:27]) is written into the device, D _[26:0] remains unaltered.
H	H	H	L	-	L - H	During the data portion of a write sequence only the lower byte (D _[35:27]) is written into the device, D _[26:0] remains unaltered.
H	H	H	H	L - H	-	No data is written into the devices during this portion of a write operation.
H	H	H	H	-	L - H	No data is written into the devices during this portion of a write operation.

1/ X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.

2/ Device powers up deselected with the outputs in a tri-state condition.

3/ "A" represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represents the internal address sequence in the burst.

4/ "t" represents the cycle at which a Read/Write operation is started. t + 1 and t + 2 are the first and second clock cycles respectively succeeding the "t" clock cycle.

5/ Data inputs are registered at K and $\bar{K}$ rising edges. Data outputs are delivered on K and $\bar{K}$ rising edges.

6/ It is recommended that K = $\bar{K}$ = HIGH when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.

7/ Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

FIGURE 3. Truth tables and device operations.

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Truth Table for device type 02 and 04 1/ 2/ 3/ 4/ 5/ 6/

Operation	K	RPSb	WPSb	DQ	DQ	DQ	DQ
Write Cycle: Load address on the rising edge of K; input write data on two consecutive K and Kb rising edges.	L - H	H <u>7/</u>	L <u>8/</u>	D(A) at K(t+1) ↑	D(A + 1) at Kb(t+1) ↑	D(A+2) at K(t+2) ↑	D(A+3) at Kb(t+2) ↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K; wait two cycles; read data on two consecutive K and Kb rising edges.	L - H	L <u>8/</u>	X	Q(A) at K(t+2) ↑	Q(A+1) at Kb(t+2) ↑	Q(A+2) at K(t+3) ↑	Q(A+3) at Kb(t+3) ↑
NOP: No Operation	L - H	H	H	D = X	Q = High Z		D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State			Previous State

- 1/ X = "Don't Care", H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
2/ Device powers up deselected with the outputs in a tri-state condition.
3/ "A" represents address location latched by the devices when transaction was initiated. A + 1, A + 2, and A + 3 represent the internal address sequence in the burst.
4/ "t" represents the cycle at which a Read/Write operation is started. t + 1, t + 2, and t + 3 are the first, second and third clock cycles respectively succeeding the "t" clock cycle.
5/ Data inputs are registered at K and $\bar{K}$ rising edges. Data outputs are delivered on K and $\bar{K}$ rising edges, except when in single clock mode.
6/ It is recommended that K = $\bar{K}$ = HIGH when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
7/ If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation.
8/ This signal was HIGH on previous K clock rise. Initiating consecutive read or write operations on consecutive K clock rises is not permitted. The device ignores the second read or write request.

FIGURE 3. Truth tables and device operations – Continued.

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Write cycle descriptions for device types 02 and 04 1/ 2/

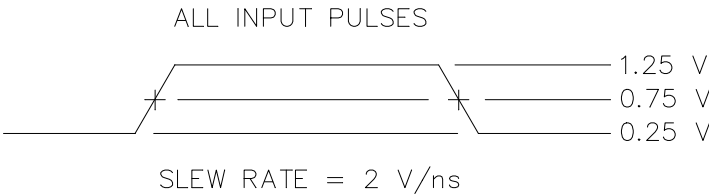
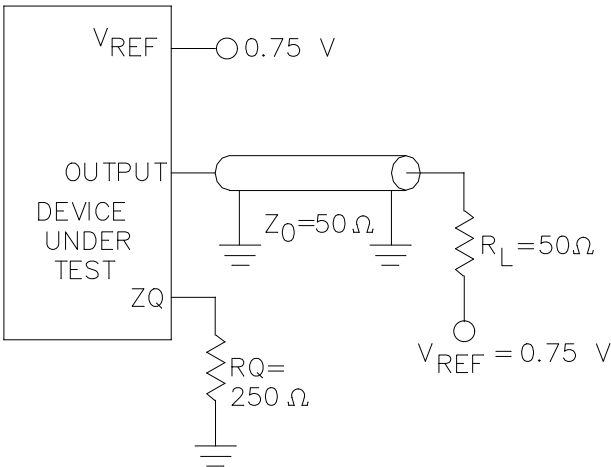
$\overline{BWS}_0$	$\overline{BWS}_1$	$\overline{BWS}_2$	$\overline{BWS}_3$	K	$\overline{K}$	Comments
L	L	L	L	L – H	-	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	-	L – H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L – H	-	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[35:9]}$ remains unaltered.
L	H	H	H	-	L – H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[35:9]}$ remains unaltered.
H	L	H	H	L – H	-	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	-	L – H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L – H	-	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device, $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	-	L-H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device, $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L – H	-	During the data portion of a write sequence, only the lower byte ($D_{[35:27]}$) is written into the device, $D_{[26:0]}$ remains unaltered.
H	H	H	L	-	L – H	During the data portion of a write sequence, only the lower byte ($D_{[35:27]}$) is written into the device, $D_{[26:0]}$ remains unaltered.
H	H	H	H	L – H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L – H	No data is written into the device during this portion of a write operation.

1. X = "Don't Care," H = Logic HIGH, L= Logic LOW.
2. This is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, and $\overline{BWS}_3$ can be altered on different portions of a write cycle, as long the setup and hold requirements are achieved.

FIGURE 3. Truth tables and device operations – Continued.

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OUTPUT LOAD CIRCUIT



NOTE: 50 Ω uniform transmission line terminated with a 50 Ω load to V_{REF} .

V_{OH}/V_{OL} TEST CIRCUIT

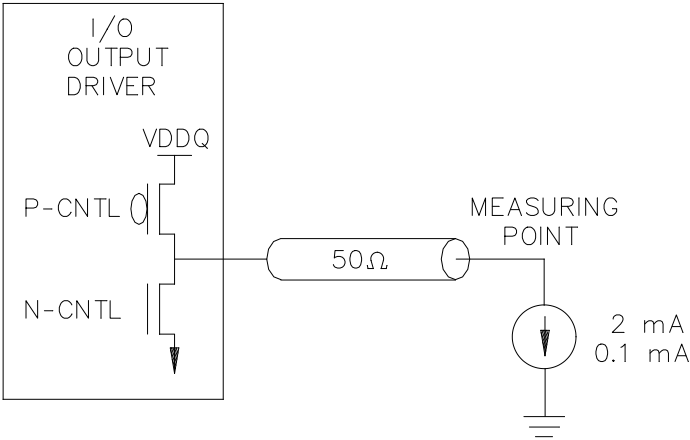
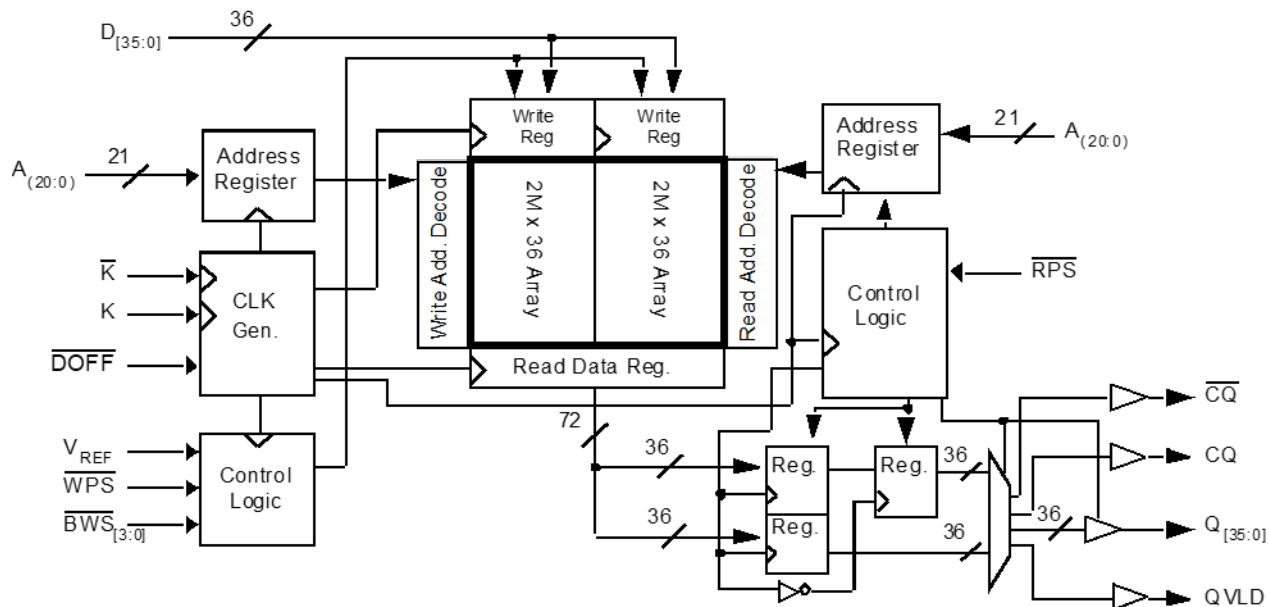


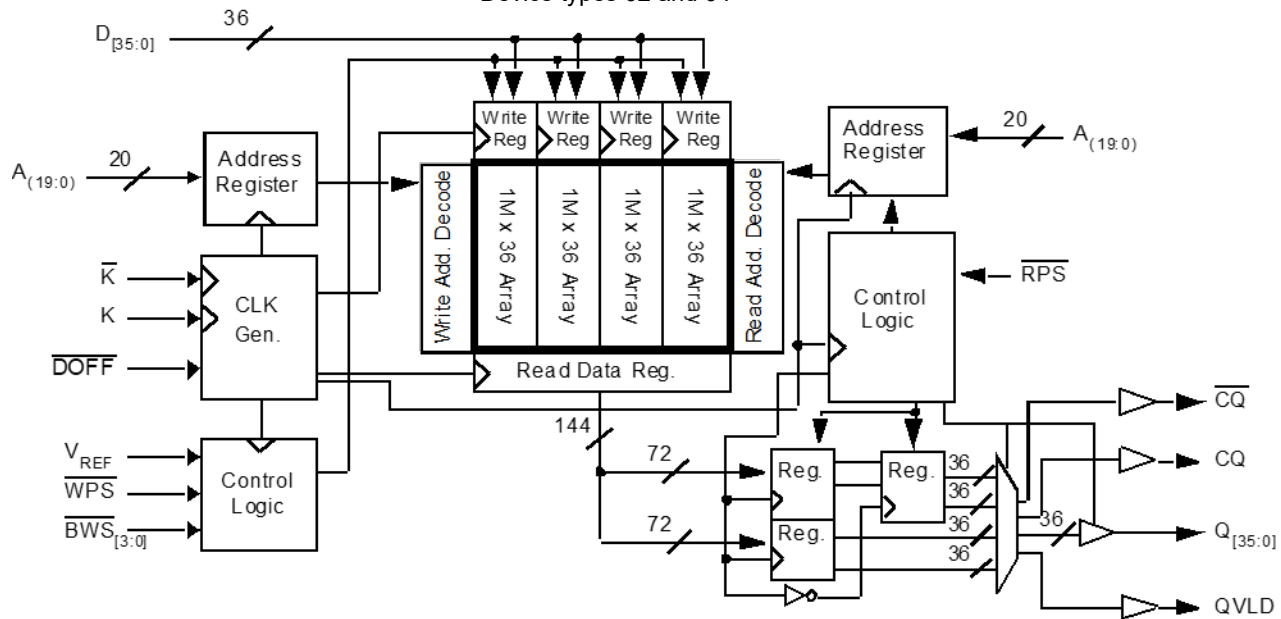
FIGURE 4. Output load circuit and V_{OH}/V_{OL} test circuit.

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Device types 01 and 03



Device types 02 and 04

FIGURE 5. Block diagrams

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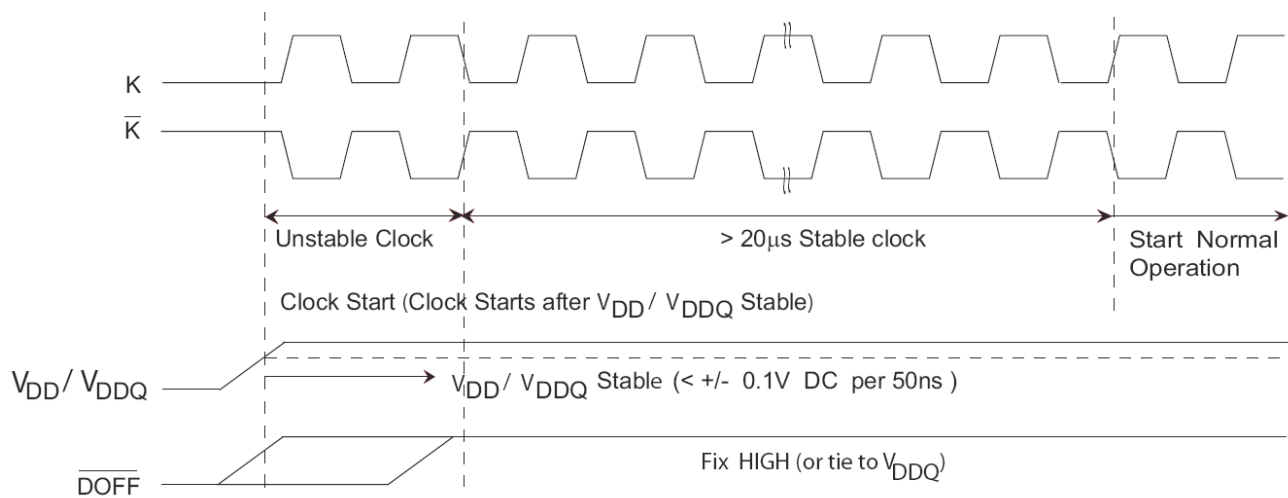


FIGURE 6. Timing waveforms.

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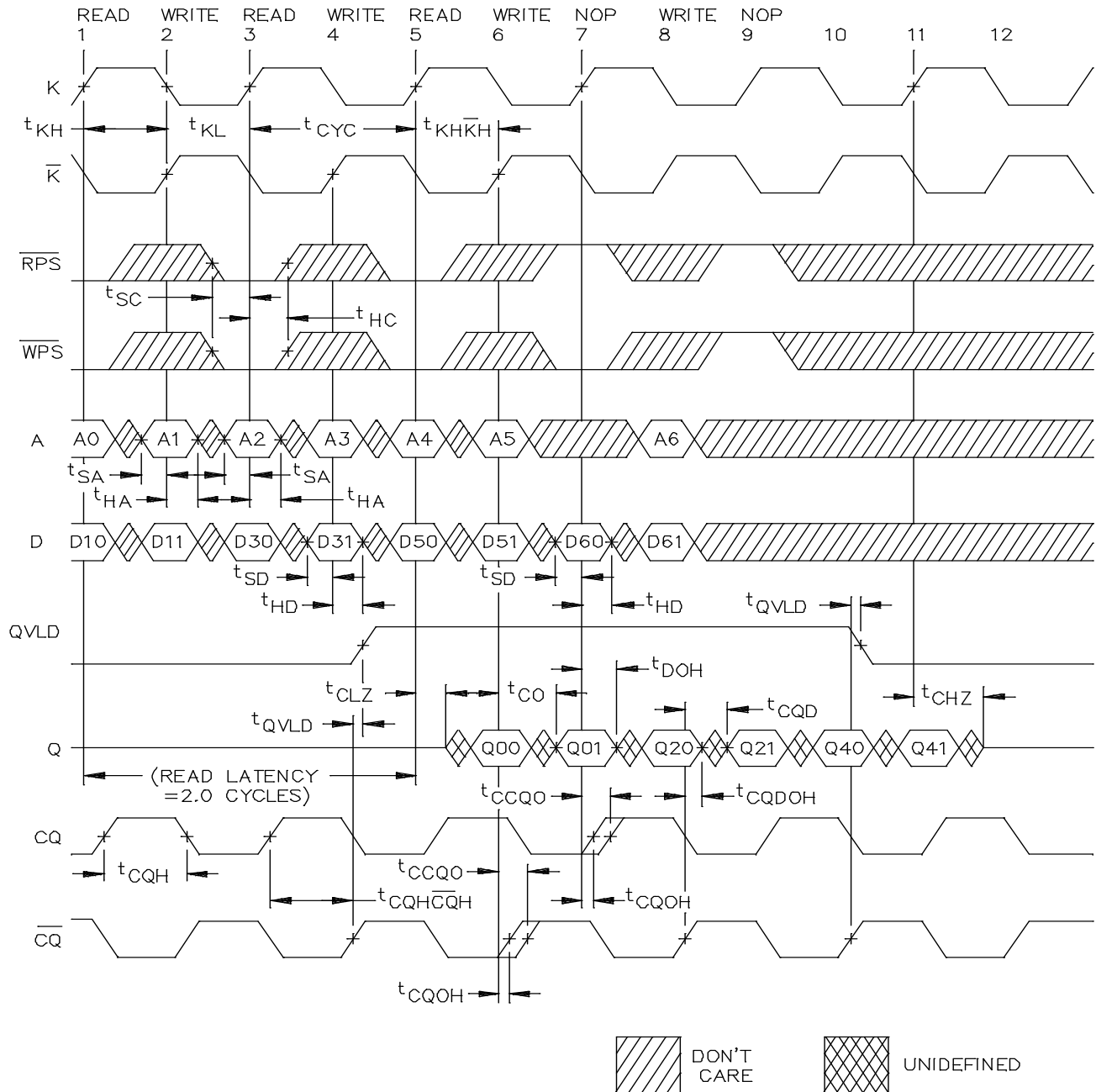
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READ/WRITE/DESELECT SEQUENCE for device types 01 and 03 1/ 2/ 3/



1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
2. Outputs are disabled (High Z) one clock cycle after a NOP.
3. In this example, if the address A0 = A1, then data Q00 = D10 and Q01 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

FIGURE 6. Timing waveforms – Continued.

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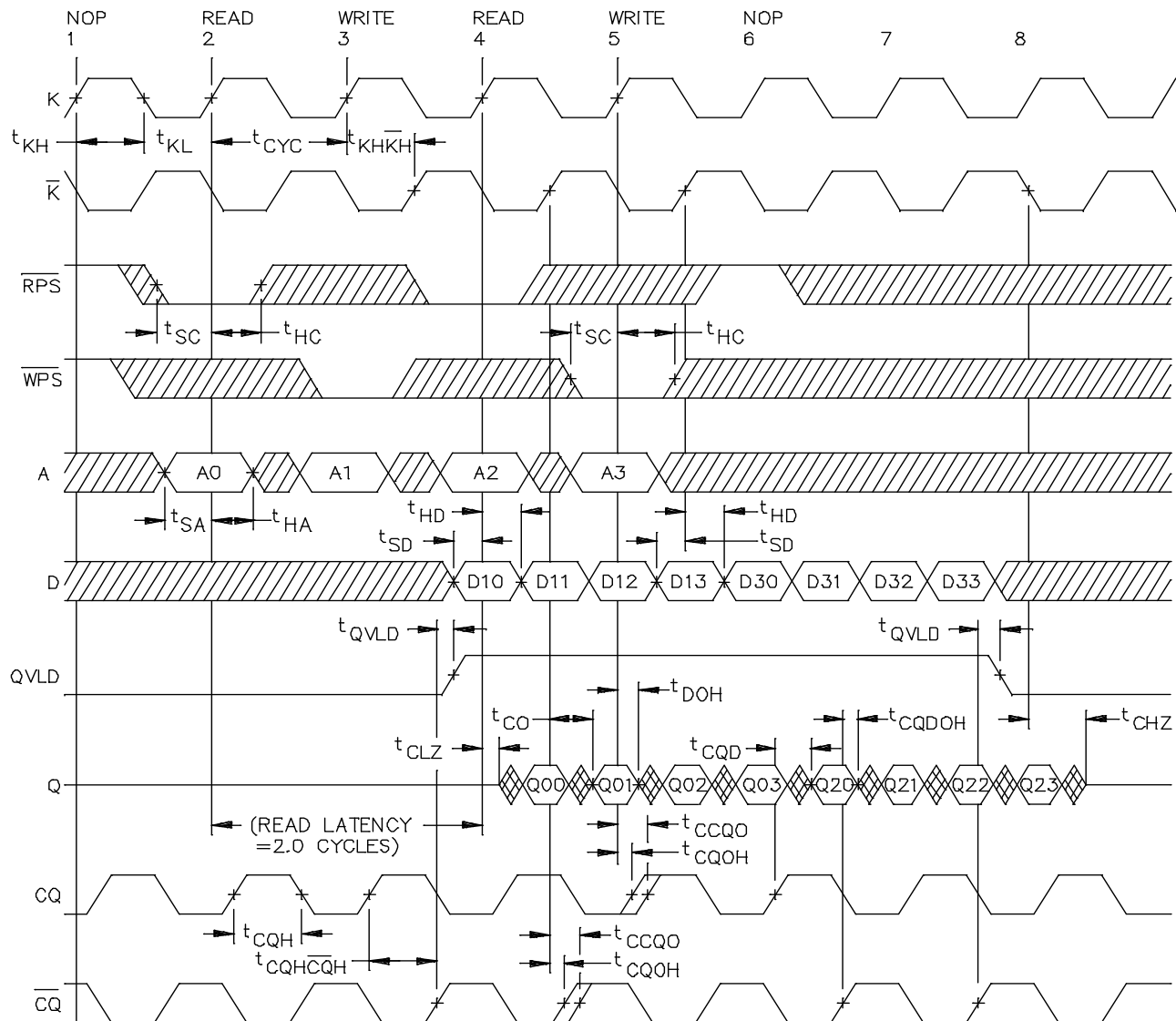
SIZE
A

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1/ 2/ 3/



1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, $A0 + 1$.
2. Outputs are disabled (High Z) one clock cycle after a NOP.
3. In this example, if the address $A2 = A1$, then data $Q20 = D10$ and $Q21 = D11$, $Q22 = D12$, and $Q23 = D13$. Write data is forwarded immediately as read results. This note applies to the whole diagram.

FIGURE 6. Timing waveforms Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(1) For class V devices, the burn-in and Group C life test operating frequency shall be greater than or equal to 5.0 MHz.

- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five (5) devices with no failures, and all input and output terminals tested.

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TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 <u>1/</u>	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 <u>1/</u>
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	---	1*, 7*, 9 Δ <u>1/</u> <u>2/</u>
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1*, 7*, 9 Δ <u>1/</u> <u>2/</u>	1*, 7*, 9 Δ <u>1/</u> <u>2/</u>
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 <u>1/</u>	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 <u>1/</u>
7	Group A test requirements (see 4.4) <u>3/</u>	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 <u>4/</u> <u>5/</u>	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 <u>4/</u> <u>5/</u>
8	Group C end-point electrical parameters (see 4.4) <u>3/</u>	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ <u>2/</u>	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ <u>2/</u>
9	Group D end-point electrical parameters (see 4.4) <u>6/</u>	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4) <u>3/</u>	1, 7, 9	1, 7, 9
11	Column attach	1, 7, 9	1, 7, 9

1/ * Indicates PDA applies to subgroup 1 and 7.

2/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta limits shall be computed with reference to previous interim electrical parameters (see Line number 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.

3/ LGA packages only

4/ ** See 4.4.1d for subgroup 4.

5/ See 3.2.8 and 4.4.1b.

6/ LGA package for all tests, plus CGA device for Column Pull and Salt Atmosphere.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein

4.4.3.1 Subgroup 5 Salt Atmosphere testing. Testing is conducted on 12 devices with no failures before solder column attach and 3 devices with no failures after solder column attach.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end point electrical parameters shall be as specified in Table IIA herein.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

- a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices.
- b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects are allowed.
- b. The fluence shall be $\geq$ than 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ion/cm²-s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$. The latch-up test temperature shall be at the maximum rated operating temperature $\pm 10^{\circ}\text{C}$ for single event upset testing.
- f. Bias conditions shall be defined by the manufacturer for latch-up measurements.
- g. Test four devices with zero failures.

4.4.4.5 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$.

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Table IIB. Burn-in and operating life test delta limits at +25°C.

Parameter <u>1/</u>	Limit	Unit
I _{DD} , I _{SB1}	± 10% of the last measured value	mA
I _X , I _{OZ}	± 2 µA	µA
I _{X_ODT} <u>2/</u>	± 2 mA	mA
V _{OH2} , V _{OL2}	± 10% of the last measured value	mV

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

2/ I_{X_ODT} is the I/O current with the On Die Termination (ODT) circuit enabled; because it depends on the selected ODT resistance, no single absolute limit applies, and it is not specified in Table I. It is monitored in Table IIB as a delta to verify ODT circuitry stability; conventional I/O leakage is covered by I_X.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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6.7 CGA packages lead finish. Microcircuits devices for column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark "F". Terminal lead finish F for devices listed on this drawing are a tin (Sn) and lead (Pb) alloy. The solder column material contains compositions of Sn = 20% and Pb = 80%.

6.8 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Number of transients (SEP).
- e. Occurrence of latch-up (SEP).

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APPENDIX A
Appendix A forms a part of SMD 5962-18215
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 25-11-03

Approved sources of supply for SMD 5962-18215 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u> <u>2/</u>	Vendor CAGE number	Vendor similar PIN <u>3/</u>
5962R1821501VXF	65786	CYRS2644KV18-250GCMB
5962R1821502VXF	65786	CYRS2645KV18-250GCMB
5962R1821503VXF	65786	CYRS1644KV18-250GCMB
5962R1821504VXF	65786	CYRS1645KV18-250GCMB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ See 1.2.4 for description of the actual case outline lead finish.
- 3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.