

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update to current MIL-PRF-38535 requirements. - rep	25-09-02	James R. Eschmeyer



Revision Status of Sheets

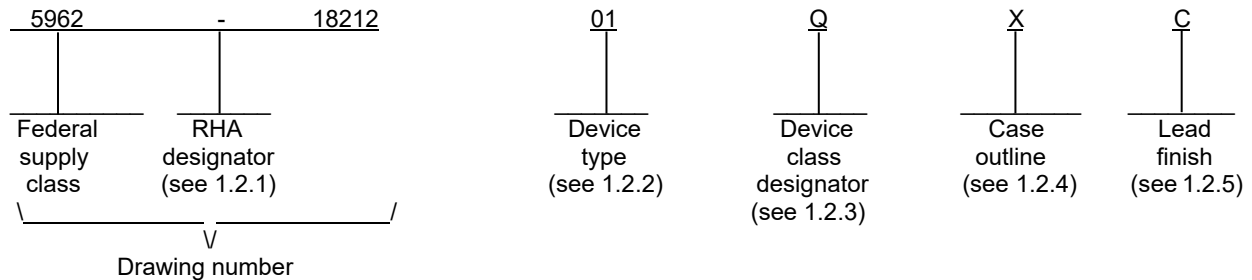
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SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A		PREPARED BY Gary L. Gross		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE		CHECKED BY Laura Leeper Branham				
		APPROVED BY Charles Saffle				
		DRAWING APPROVAL DATE 19-07-22				
AMSC N/A		REVISION LEVEL A		SIZE A	CAGE CODE 67268	5962-18212
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access Time</u>	<u>Store Cycle</u>	<u>Recall Cycle</u>	<u>Endurance</u>
01	14CA8C	128K X 8 NVSRAM	35 ns	8 ms	20 ms	100,000 cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	32	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V _{CC})	-0.5 V dc to 7.0 V dc
Voltage on DQ ₍₀₋₇₎ with outputs in high Z state	-0.5 V to (V _{CC} + 0.5 V)
Input voltage operating range (V _{IH} , V _{IL})	-0.5 V to (V _{CC} + 0.5 V)
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D)	1.0 W
Maximum output current	15 mA
Lead temperature (soldering)	260°C
Junction temperature (T _J) 3/	150°C
Thermal resistance, junction to case (θ _{JC})	see MIL-STD-1835
Data retention	10 years to nonvolatile array (minimum)
Endurance (as store cycles to non-volatile array)	100,000 store cycles (minimum)

1.4 Recommended operating conditions. 1/ 2/

Supply voltage range (V _{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T _C)	-55°C to +125°C
Input voltage, low range (V _{IL})	V _{SS} - 0.5 V dc to 0.8 V dc, all inputs
Input voltage, high range (V _{IH})	2.2 V dc to V _{CC} + 0.5 V dc, all inputs

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JESD 78 - IC Latch-Up Test.

(Copies of this document are available online at <https://www.jedec.org>).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ All voltages are referenced to V_{SS} (ground).
- 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional tests. Various functional tests used to test this device are contained in Appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 AC output loading. The AC output loading shall be as specified on figure 3.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.9 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V _{CC} current	I _{CC1}	Addresses cycling at t _{RC}	1, 2, 3	All		85	mA
V _{CC} current during store cycle	I _{CC2}	All inputs = don't care, V _{CC} = max, average current for duration t _{STORE}	1, 2, 3	All		15	mA
V _{CC} current at t _{RC} = 200 ns, V _{CC} = 25°C	I _{CC3}	All inputs cycling at CMOS levels	1, 2, 3	All		35	mA
V _{CAP} current during automatic store on power loss	I _{CC4}	All inputs = don't care, average current for duration t _{STORE}	1, 2, 3	All		8	mA
V _{CC} standby current	I _{SB}	$\overline{CE} > (V_{CC} - 0.2 \text{ V})$, $V_{IN} < 0.2 \text{ V}$ or $> (V_{CC} - 0.2 \text{ V})$, Standby current level after non-volatile cycle is complete, Inputs are static, f = 0 MHz	1, 2, 3	All		10	mA
Input leakage current, (except $\overline{HSB}$) <u>1/</u>	I _{ILK1}	V _{CC} = 5.5 V, V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All		+5	μA
Input leakage current for $\overline{HSB}$ <u>1/</u>	I _{ILK2}	V _{CC} = 5.5 V, V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All	-100	±5	μA
Off state output leakage current	I _{OLK}	V _{CC} = 5.5 V V _{IN} = V _{SS} to V _{CC}	1, 2, 3	All		±5	μA
Input logic "1" voltage	V _{IH}	All Inputs	1, 2, 3	All	2.2	V _{CC} + 0.5	V
Input logic "0" voltage	V _{IL}	All Inputs	1, 2, 3	All	V _{SS} - 0.5	0.8	V
Output Logic "1" voltage	V _{OH}	I _{OH} = -4 mA	1, 2, 3	All	2.4		V
Output Logic "0" voltage	V _{OL}	I _{OL} = 8 mA	1, 2, 3	All		0.4	V
Low voltage trigger level	V _{SWITCH}		1, 2, 3	All		4.4	V
$\overline{HSB}$ output disable voltage inactive <u>4/</u>	V _{HDIS}		1, 2, 3	All		1.9	V
Storage capacitor <u>2/</u>	V _{CAP}	Between V _{CAP} pin and V _{SS}	1, 2, 3	All	61	180	μF
Maximum voltage driven on V _{CAP} pin by the device <u>3/ 4/</u>	V _{VCAP}	V _{CC} = Max	1, 2, 3	All	2.4		V
Input capacitance	C _{IN}	ΔV = 0 to 3 V T _A = 25°C, f = 1.0 MHz See 4.4.1e	4	All		8	pF
Output capacitance	C _{OUT}	ΔV = 0 to 3 V T _A = 25°C, f = 1.0 MHz See 4.4.1e	4	All		8	pF
Functional tests		See 4.4.1c	7, 8A, 8B			V _{CC} - 0.5	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Sym bol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLES #1 & #2							
Chip enable access time	t _{ACE}	See figures 3 and 4	9, 10, 11	All		35	ns
Read cycle time <u>5/</u>	t _{RC}		9, 10, 11	All	35		ns
Address access time <u>6/</u>	t _{AA}		9, 10, 11	All		35	ns
Output enable to data valid	t _{DOE}		9, 10, 11	All		15	ns
Output hold after address change <u>6/</u>	t _{OHA}		9, 10, 11	All	3		ns
Chip enable to output active <u>7/ 8/</u>	t _{LZCE}		9, 10, 11	All	3		ns
Chip disable to output inactive <u>7/ 8/</u>	t _{HZCE}		9, 10, 11	All		13	ns
Output enable to output active <u>7/ 8/</u>	t _{LZOE}		9, 10, 11	All	0		ns
Output disable to output inactive <u>7/ 8/</u>	t _{HZOE}		9, 10, 11	All		13	ns
Chip enable to power active <u>4/</u>	t _{PU}		9, 10, 11	All	0		ns
Chip disable to power standby <u>4/</u>	t _{PD}		9, 10, 11	All		35	ns
WRITE CYCLE #1 & #2							
Write cycle time	t _{WC}	See figures 3 and 4	9, 10, 11	All	35		ns
Write pulse width	t _{PWE}		9, 10, 11	All	25		ns
Chip enable to end of write	t _{SCE}		9, 10, 11	All	25		ns
Data set-up to end of write	t _{SD}		9, 10, 11	All	12		ns
Data hold after end of write	t _{HD}		9, 10, 11	All	0		ns
Address set-up to end of write	t _{AW}		9, 10, 11	All	25		ns
Address set-up to start of write	t _{SA}		9, 10, 11	All	0		ns
Address hold after end of write	t _{HA}		9, 10, 11	All	0		ns
Write enable to output disable <u>4/ 7/ 8/</u>	t _{HZWE}		9, 10, 11	All		13	ns
Output active after end of write <u>4/ 7/</u>	t _{LZWE}		9, 10, 11	All	3		ns
See footnotes at end of table.							
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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V V _{SS} = 0 V, I _{OUT} = 0 mA unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HARDWARE STORE/RECALL							
RECALL cycle duration <u>9/</u>	t _{HRECALL}	See figures 3 and 4	9, 10, 11	All		20	ms
STORE cycle duration <u>10/</u>	t _{STORE}	V _{CC} ≥ 4.5 V. See figures 3 and 4	9, 10, 11	All		8	ms
Time allowed to complete SRAM write cycle <u>11/</u>	t _{DELAY}	See figures 3 and 4	9, 10, 11	All	25		ns
V _{CC} rise time <u>4/</u>	t _{VCCRISE}		9, 10, 11	All	150		μs
HSB to output active time enable <u>4/</u>	t _{LZHSB}		9, 10, 11	All		5	ns
HSB high active time <u>4/</u>	t _{HHD}		9, 10, 11	All		500	μs
SOFTWARE STORE/RECALL							
STORE/RECALL initiation cycle time <u>12/ 13/</u>	t _{RC}	See figures 3 and 4	9, 10, 11	All	35		ns
Address setup time <u>12/ 13/</u>	t _{SA}		9, 10, 11	All	0		ns
Clock pulse width <u>12/ 13/</u>	t _{CW}		9, 10, 11	All	25		ns
Address hold time <u>12/ 13/</u>	t _{HA}		9, 10, 11	All	0		ns
RECALL duration <u>12/ 13/</u>	t _{RECALL}		9, 10, 11	All		200	μs

- 1/ The $\overline{\text{HSB}}$ pin has I_{OUT} = -2 μA for V_{OH} of 2.4 V when both active high and low drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
- 2/ Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits. Contact the manufacturer for more details on V_{CAP} options.
- 3/ Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
- 4/ These parameters are guaranteed by design and are not tested.
- 5/ $\overline{\text{WE}}$ must be HIGH during SRAM read cycles.
- 6/ Device is continuously selected with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ low.
- 7/ Measured ±200 mV from steady state output voltage.
- 8/ If $\overline{\text{WE}}$ is low when $\overline{\text{CE}}$ goes low, the outputs remain in the high impedance state.
- 9/ t_{HRECALL} starts from the time V_{CC} rises above V_{SWITCH}.
- 10/ If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
- 11/ On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
- 12/ The software sequence is clocked with $\overline{\text{CE}}$ controlled or $\overline{\text{OE}}$ controlled reads.
- 13/ The six consecutive addresses must be read in the order listed in Figure 2. $\overline{\text{WE}}$ must be HIGH during all six consecutive cycles.

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Device types	ALL
Case outlines	X
Terminal number	Terminal symbol
1	V _{CAP}
2	A ₁₄
3	A ₁₂
4	A ₇
5	A ₆
6	A ₅
7	A ₄
8	A ₃
9	A ₁₆
10	A ₂
11	A ₁
12	A ₀
13	DQ ₀
14	DQ ₁
15	DQ ₂
16	V _{SS}
17	DQ ₃
18	DQ ₄
19	DQ ₅
20	DQ ₆
21	DQ ₇
22	$\overline{\text{CE}}$
23	A ₁₀
24	A ₁₅
25	$\overline{\text{OE}}$
26	A ₁₁
27	A ₉
28	A ₈
29	A ₁₃
30	$\overline{\text{WE}}$
31	HSB
32	V _{CC}

FIGURE 1. Terminal connections.

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$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A ₁₆ -A ₀ ^{1/} (HEX)	MODE	I/O	POWER	NOTES
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read RAM	Output Data	Active	
L	L	X	X	Write RAM	Input Data	Active	
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	^{2/}
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	^{2/}
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I _{cc2}	^{2/}
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	^{2/}

^{1/} While there are 17 address lines on the device, only the lower 14 are used to control software modes.

^{2/} The six consecutive address locations must be in the order listed. $\overline{\text{WE}}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

FIGURE 2. Truth table.

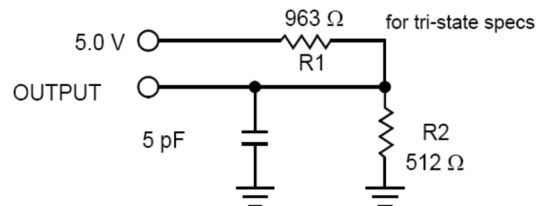
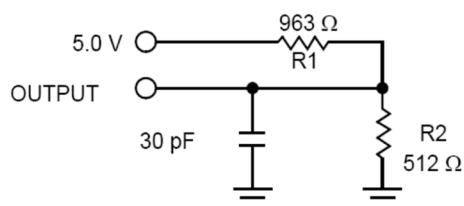
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AC TEST CONDITIONS 1/

TEST CONDITION	VALUES
Input pulse levels	V_{SS} to 3 V
Input rise & fall time	≤ 3 ns
Input and output timing reference levels	1.5 V
Output load	Per Figure 3

1/ All voltages are referenced to V_{SS} (ground).

FIGURE 3. AC output loading.

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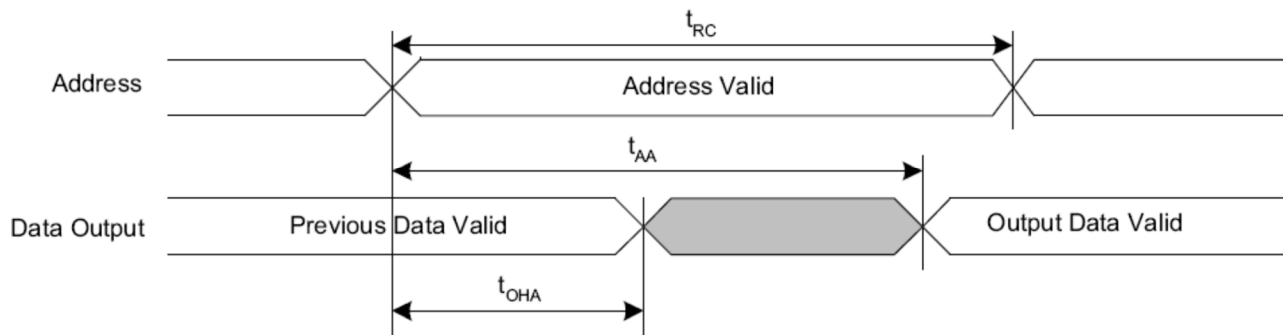
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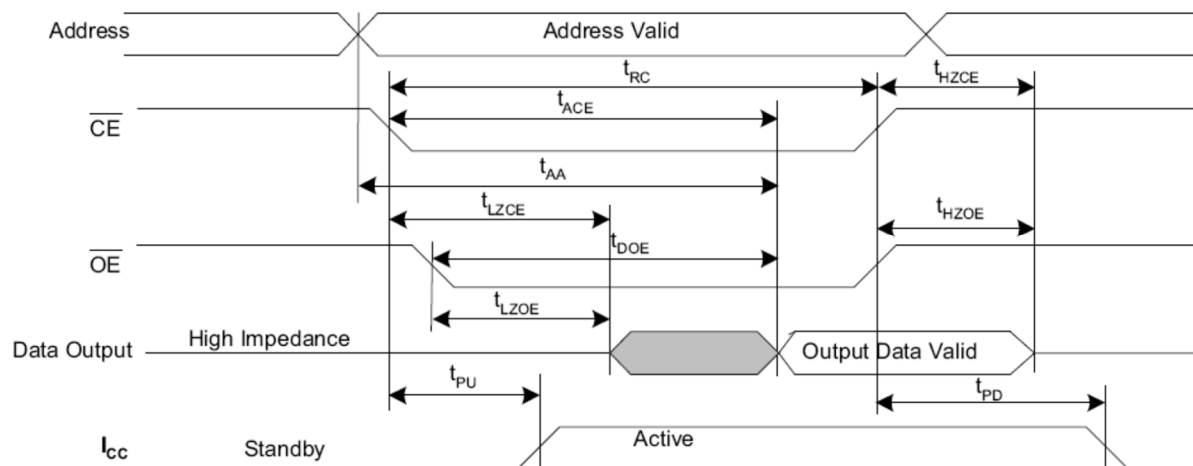
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SRAM READ CYCLE #1 (Address Controlled) 1/ 2/ 3/



SRAM READ CYCLE #1 ($\overline{CE}$ and $\overline{OE}$ Controlled) 1/ 3/



- 1/ $\overline{WE}$ must be HIGH during SRAM read cycles.
- 2/ Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ LOW.
- 3/ $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

FIGURE 4. Timing waveforms.

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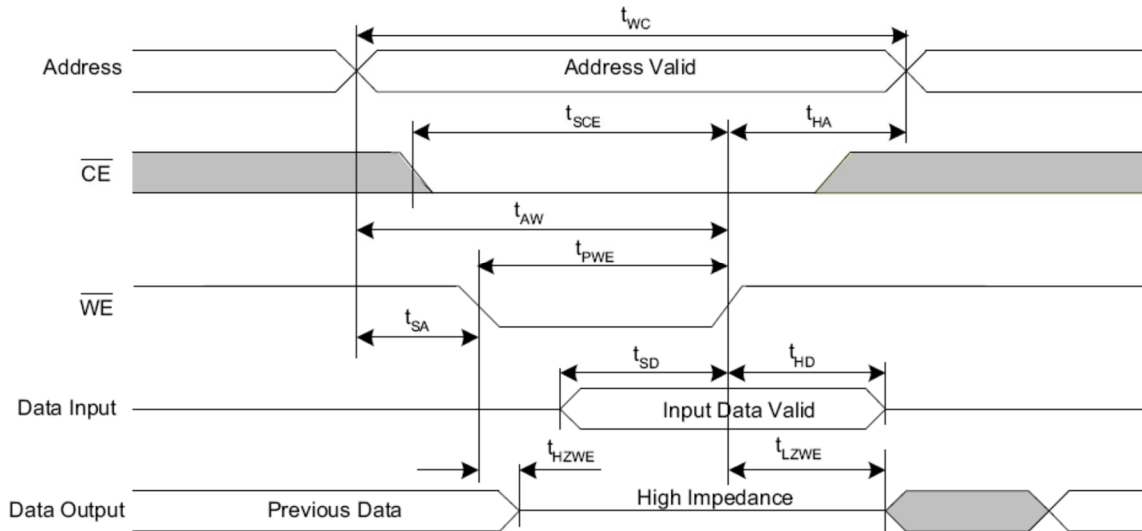
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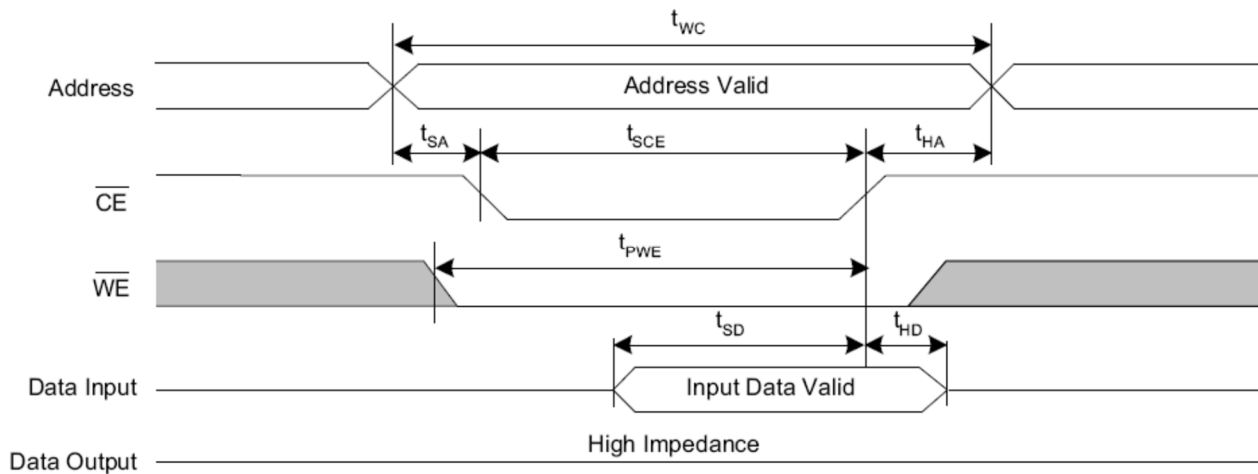
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SRAM WRITE CYCLE #1 ($\overline{\text{WE}}$ Controlled) 1/ 2/ 3/



SRAM WRITE CYCLE #2 ($\overline{\text{CE}}$ Controlled) 1/ 2/ 3/



- 1/ $\overline{\text{HSB}}$ must remain HIGH during READ and WRITE cycles.
- 2/ If $\overline{\text{WE}}$ is low when $\overline{\text{CE}}$ goes low, the outputs remain in the high impedance state.
- 3/ $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be $> V_{\text{IH}}$ during address transitions.

FIGURE 4. Timing waveforms - continued.

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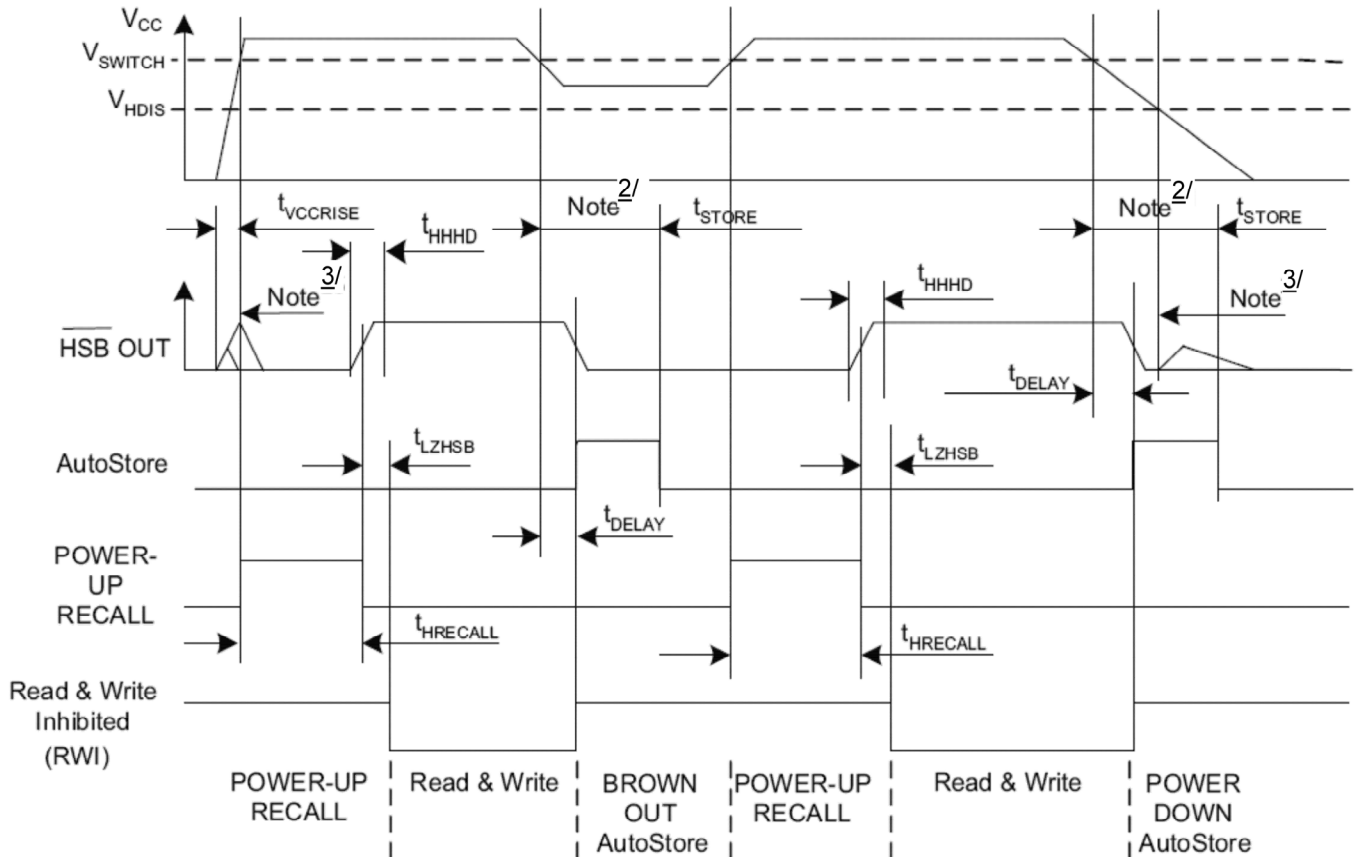
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AUTOSTORE or Power-Up RECALL ^{1/}



^{1/} Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is less than V_{SWITCH}.

^{2/} If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

^{3/} During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

FIGURE 4. Timing waveforms - continued.

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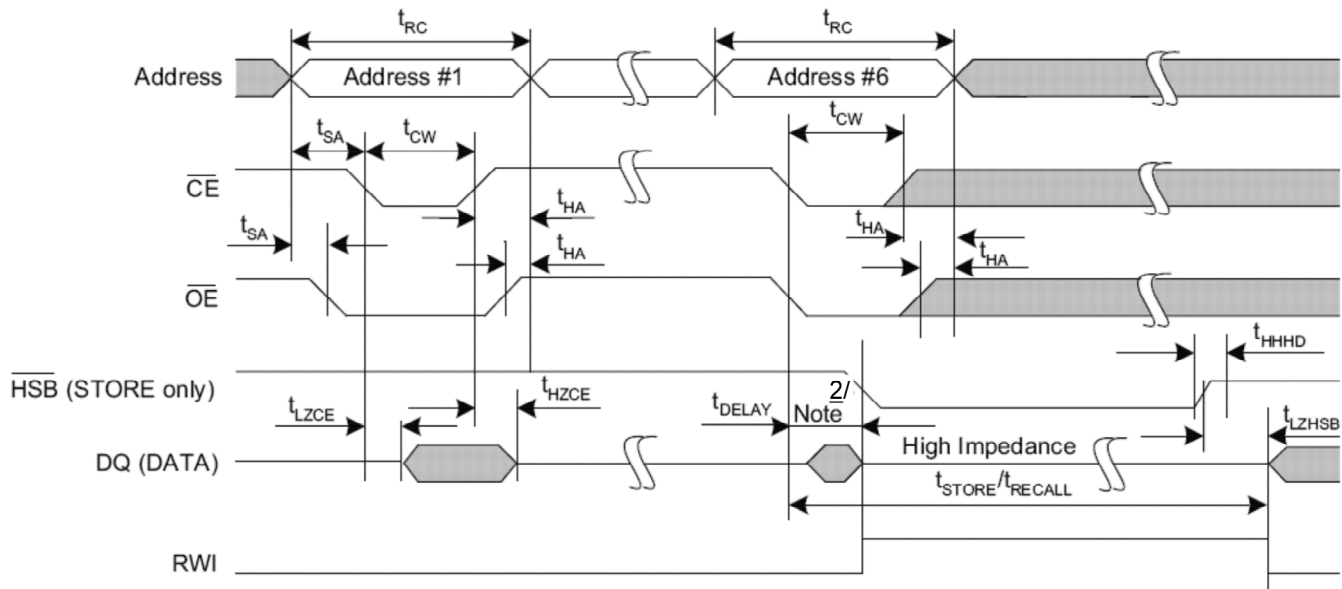
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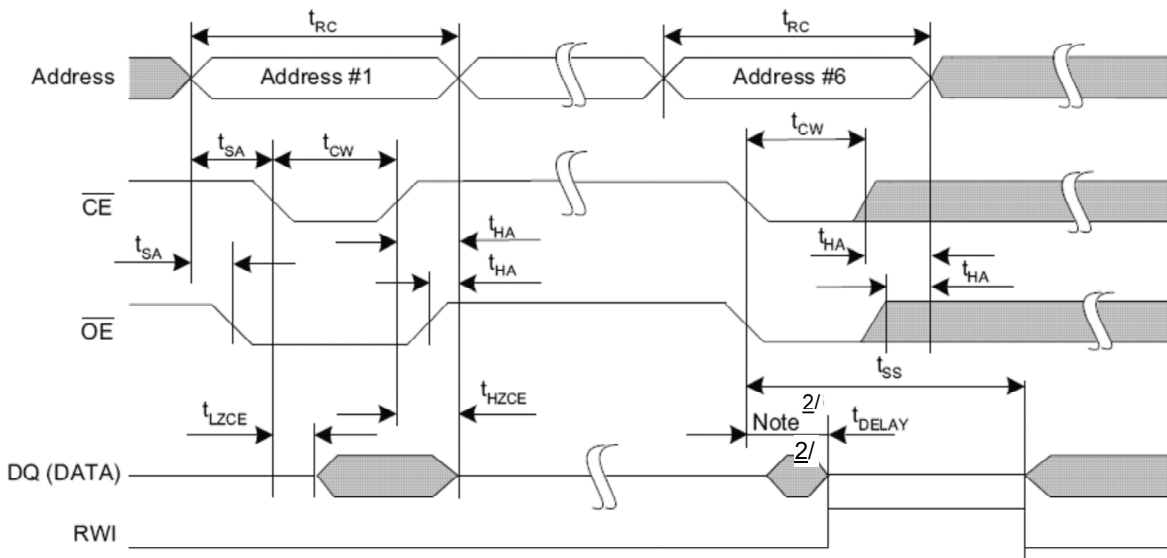
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$\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled Software STORE/RECALL 1/



Autostore Enable/Disable Cycle 1/



1/ The six consecutive addresses must be read in the order listed in Figure 2. $\overline{\text{WE}}$ must be HIGH during all six consecutive cycles.

2/ DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

FIGURE 4. Timing waveforms - continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V subgroups 7, 8A, and 8B shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	---	1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	---	1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.

4/ * indicates PDA applies to subgroups 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.

7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Limit	Unit
	All Devices	
I _{CC1} , I _{SB}	± 10% of the measured value	mA
I _{ILK1} , I _{ILK2} , I _{OLK}	± 2 μA	μA
V _{OH} , V _{OL}	± 10% of the measured value	V

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device classes Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits, are listed in table IIB.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

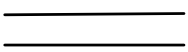
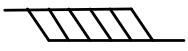
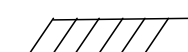
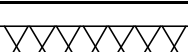
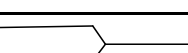
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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

C _{IN}	Input terminal capacitance.
C _{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I _{CC}	Supply current.
I _{IH}	Input high current.
I _{IL}	Input low current.
T _C	Case temperature.
T _A	Ambient temperature
V _{CC}	Ground zero voltage potential.
O/V	Latch-up over-voltage
HSB	Hardware store/busy
V _{CAP}	Capacitor voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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APPENDIX A

APPENDIX A forms a part of SMD 5962-18212

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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APPENDIX A – continued.

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A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 25-09-02

Approved sources of supply for SMD 5962-18212 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-1821201QXC	65786	STK14CA8C-5C35M

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.