

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to meet current MIL-PRF-38535 requirements. – glg	15-12-16	Charles Saffle
B	Update drawing to meet current MIL-PRF-38535 and Accessibility/508 Compliance requirements. – rp	22-09-26	James R. Eschmeyer



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

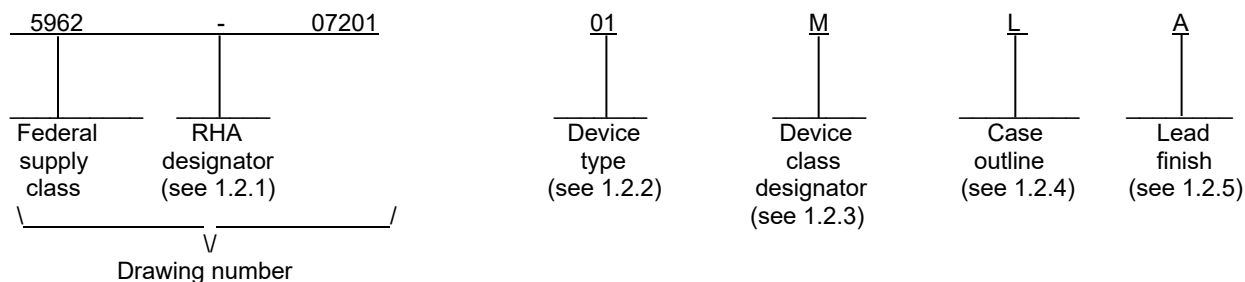
REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A				
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY Kenneth Rice	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY Rajesh Pithadia			
	APPROVED BY Robert M. Heber	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ERASEABLE (EE) PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 07-08-17			
AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE 67268	5962-07201
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Address access time</u>
01	F750C	22-input 10-output and-or-logic array	10 ns
02	F750C	22-input 10-output and-or-logic array	15 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
L	GDIP3-T24	24	dual-in-line package
3	CQCC1-N28	28	square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc 2/
Input voltage range	-0.5 V dc to V _{CC} +1.0 V dc 2/
Output voltage applied	-0.5 V dc to V _{CC} +1.0 V dc 2/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 3/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds)	+240°C
Data Retention	10 Years (Minimum)
Endurance	100 Erase/Write Cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V _{IH})	2.0 V dc minimum
Low level input voltage (V _{IL})	0.8 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

1/ All voltages referenced to V_{SS}.

2/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.

3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or quality conformance inspection group A, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices shall be as specified by an attached item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Processing EEPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

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3.6.1 Erasure of EEPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.6.2 Programmability of EEPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7.

3.6.3 Verification of erasure or programmed EEPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.7.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.9 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.11 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendor's procedure shall be under document control and shall be made available upon request.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors' procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$I_O = -4.0\text{ mA}$	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	$I_O = 12\text{ mA}$	1, 2, 3	All		0.5	V
High impedance output leakage current <u>2/</u>	I_{OZ}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, $V_O = \text{GND}$	1, 2, 3	All	-10	10	μA
High level input current	I_{IH}	$V_{IH} = 5.5\text{ V}$, $V_{CC} = 5.5\text{ V}$ <u>3/</u>	1, 2, 3	All		10	μA
Low level input current	I_{IL}	$V_{IH} = \text{GND}$, $V_{CC} = 5.5\text{ V}$ <u>3/</u>	1, 2, 3	All		-10	μA
Standby supply current	I_{CC2}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = \text{GND}$, outputs open	1, 2, 3	All		190	mA
Input capacitance	C_I <u>4/</u>	$V_I = 0\text{ V}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$, $f = 1\text{ Mhz}$ (see 4.4.1e)	4	All		8	pF
Output capacitance	C_O <u>4/</u>	$V_O = 0\text{ V}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$, $f = 1\text{ Mhz}$ (see 4.4.1e)	4	All		8	pF
Functional tests		See section 4.4.1c.	7, 8A, 8B				
Input or feedback to nonregistered output	t_{PD}	$V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$, see figures 4 and 5	9, 10, 11	01		10	ns
				02		15	
Clock to output	t_{CO}	$V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$, see figures 4 and 5	9, 10, 11	01		10	ns
				02		14	
Input to output enable	t_{EA}	$V_{CC} = 4.5\text{ V}$, $C_L = 5\text{ pF}$, see figures 4 and 5	9, 10, 11	01		10	ns
				02		15	
Input to output disable	t_{ER}		9, 10, 11	01		10	ns
				02		15	
Clock period	t_P	$V_{CC} = 4.5\text{ V}$, $C_L = 5\text{ pF}$, see figures 4 and 5	9, 10, 11	01	11		ns
				02	14		
Clock pulse width <u>5/</u>	t_{CL}	$V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$, see figures 4 and 5	9, 10, 11	01	5.5		ns
				02	7		
Clock to feedback	t_{CF}	$V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$, see figures 4 and 5	9, 10, 11	01	7.5		ns
				02	9		
Input setup time <u>5/</u>	t_S		9, 10, 11	01	4		ns
				02	8		
Hold time <u>5/</u>	t_H		9, 10, 11	01	2		ns
				02	5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Maximum clock frequency 1/(t _{ts} + t _{co}) <u>4/ 5/</u>	f _{MAX}	V _{CC} = 4.5 V, C _L = 50 pF, see figures 4 and 5	9, 10, 11	01	71		MHz
				02	45		
Internal Maximum clock frequency 1/(t _{sf} + t _{cf}) <u>4/ 5/</u>	f _{MAX}		9, 10, 11	01	87		MHz
				02	62.5		
Asynchronous reset pulse width <u>4/</u>	t _{AW}		9, 10, 11	01	10		ns
				02	15		
Asynchronous reset recovery time	t _{AR}		9, 10, 11	01	10		ns
				02	15		
Feedback setup time <u>4/</u>	t _{sf}		9, 10, 11	01	4		ns
				02	7		
Asynchronous reset to registered output reset	t _{AP}		9, 10, 11	01		12	ns
				02		15	
Clock period, input pin clock	t _{ps}		9, 10, 11	01	10		ns
				02	12		
Clock pulse width, input pin clock	t _{ws}		9, 10, 11	01	5		ns
				02	6		
Clock to feedback, input pin clock <u>4/</u>	t _{cfs}		9, 10, 11	01		5	ns
				02		5.5	
Input setup time, input pin clock	t _{ss}		9, 10, 11	01	6.5		ns
				02	8		
Hold time, input pin clock	t _{hs}		9, 10, 11	All	0		ns
External Maximum clock frequency, input pin clock 1/(t _{ss} + t _{cos}) <u>4/ 5/</u>	f _{MAXS}		9, 10, 11	01		74	MHz
				02		55	
Internal Maximum clock frequency, input pin clock 1/(t _{sfs} + t _{cfs}) <u>4/ 5/</u>	f _{MAXS}		9, 10, 11	01		87	MHz
				02		80	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous reset recovery time, input pin clock	t_{ARS}	$V_{CC} = 4.5\text{ V}$, $C_L = 50\text{ pF}$, see figures 4 and 5	9, 10, 11	01	10		ns
				02	15		
Clock to output, input pin clock	t_{COS}		9, 10, 11	01	0	7	ns
				02	0	10	
Setup time, synchronous preset product term clock	t_{SP}		9, 10, 11	01	7		ns
				02	8		
Feedback setup time, input pin clock <u>4/</u>	t_{SFS}		9, 10, 11	01	6.5		ns
				02	7		
Power up reset time <u>6/</u>	t_{PR}		9, 10, 11	All		1.0	μs
Setup time, synchronous preset, input pin clock	t_{SPS}		9, 10, 11	01	5		ns
				02	11		

1/ All voltages are referenced to ground.2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ} .3/ See figure 7 for I/V Curve for ppk (bus friendly pin-keeper option).4/ Tested only initially and after any major design changes.5/ Test applies only to register outputs.6/ See figure 6 t_{PR} waveform.

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Device types	01-02	
Case outlines	L	3
Terminal number	Terminal symbol	
1	CK/I	NC/V _{CC}
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC/GND
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC/GND
23	I/O	I/O
24	V _{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V _{CC}

NOTE:

For case outline 3, pins 1, 8, 15, and 22 can be left unconnected; however, for superior performance connect V_{CC} to pin 1, GND to pins 8, 15, and 22.

FIGURE 1. Terminal connections

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Truth table																					
Input pins												Output pins									
I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H

NOTES:

1. H = three-state.
2. X = don't care

FIGURE 2. Truth table (unprogrammed).

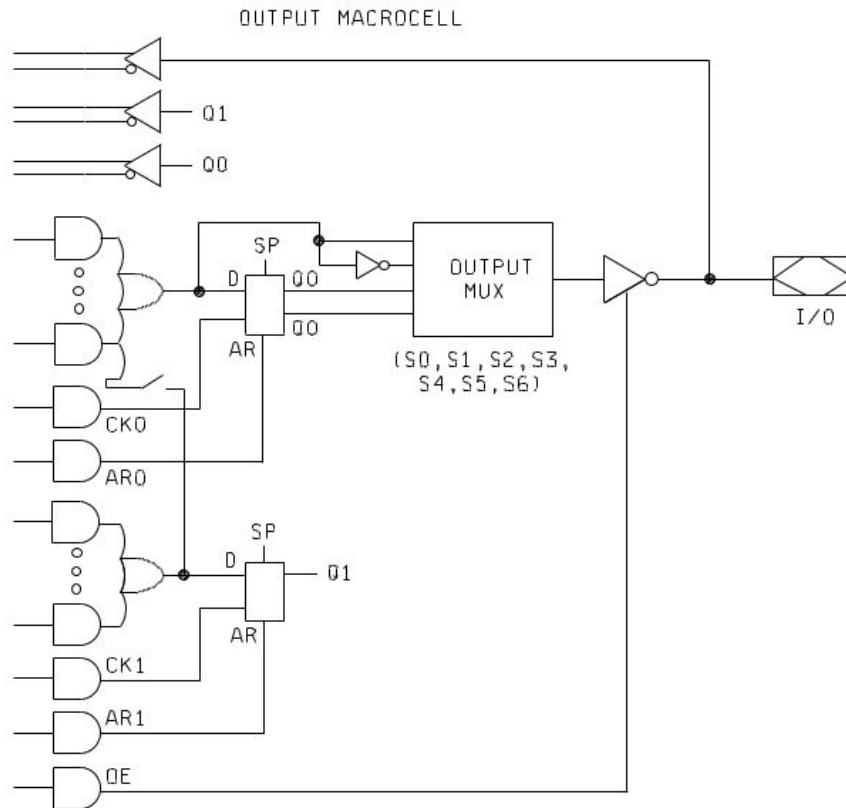
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	ERASED (1)	PROGRAM (0)
S0	COMMUTORIAL	SYNC / REG
S1	AL0 / 1 SEPERATE	MERGED
S2	ACTIVE HIGH	ACTIVE LOW
S3	PIN CLK REG. 0	PRODUCT TERM CLK / REG. 0
S4	PIN CLK REG. 1	PRODUCT TERM CLK / REG. 1
S5	T- TYPE REG. 0	D-TYPE REG REG. 0
S6	T- TYPE REG. 1	D-TYPE REG REG. 1

FIGURE 3. Logic diagram (unprogrammed).

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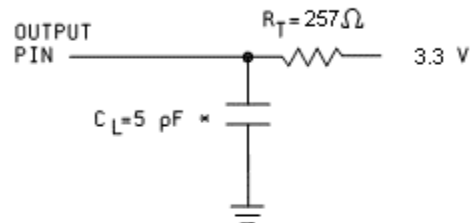
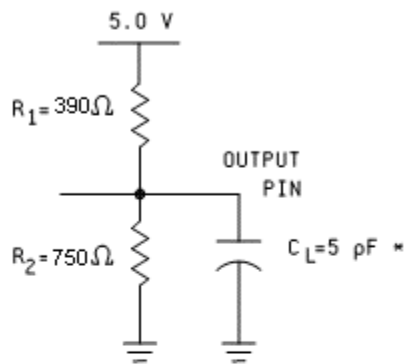
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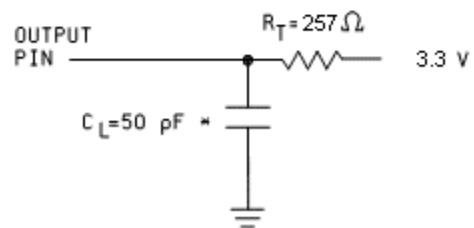
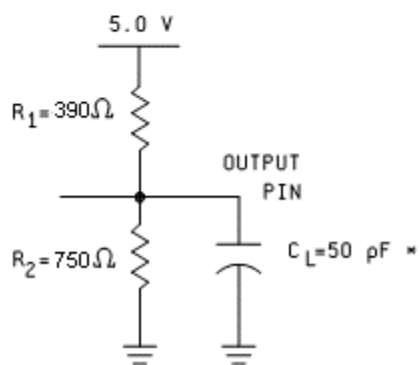
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OUTPUT TEST LOAD



CIRCUIT A OR EQUIVALENT

OUTPUT TEST LOAD



CIRCUIT B OR EQUIVALENT

*Including jig and scope
(minimum value)

FIGURE 4. Output test circuit.

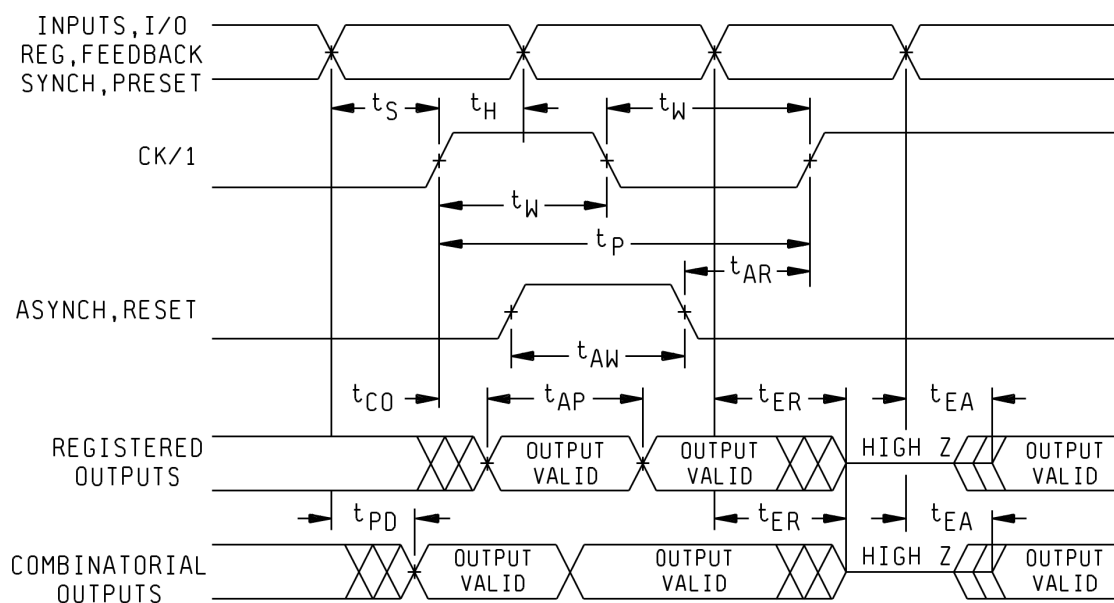
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NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V, unless otherwise specified.

FIGURE 5. Switching waveforms

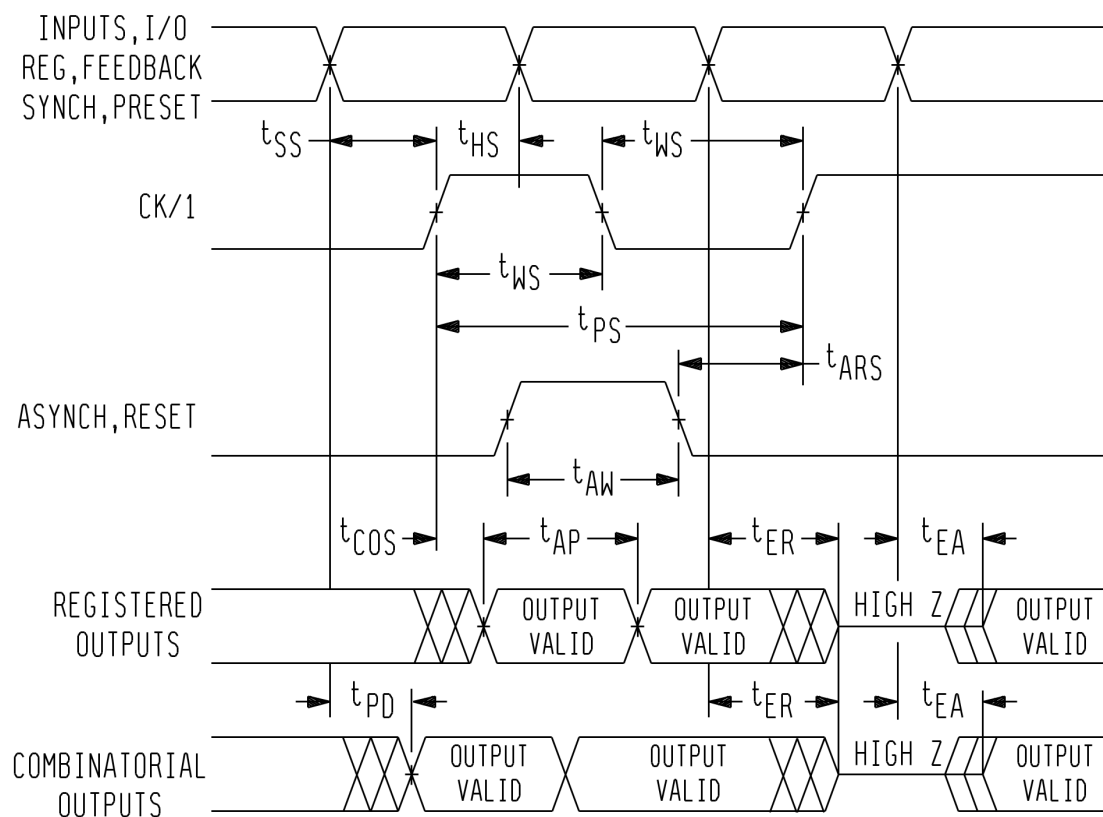
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NOTE: Timing measurement reference is 1.5 V. Input ac driving levels are 0.0 V and 3.0 V, unless otherwise specified.

FIGURE 5. Switching waveforms - Continued.

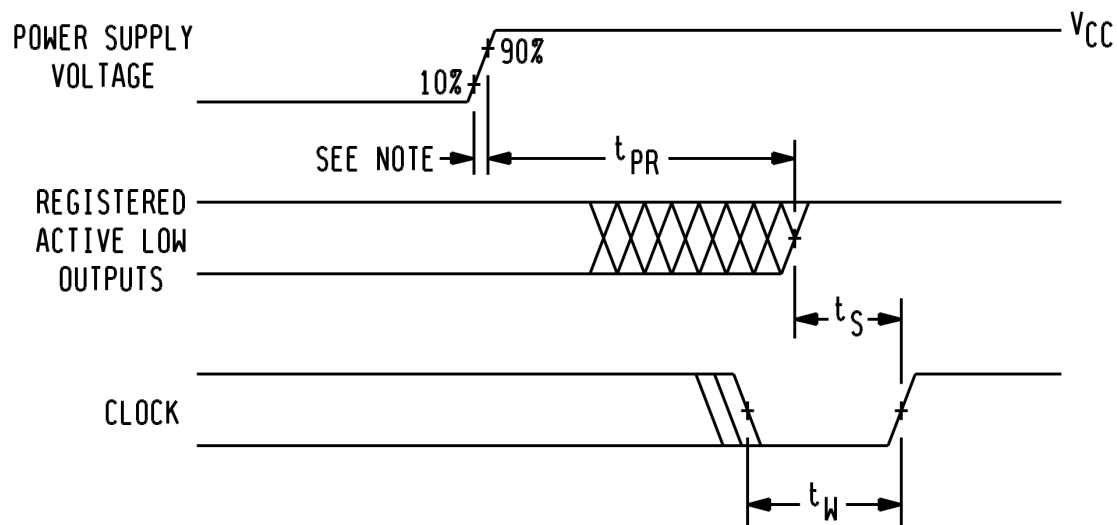
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Note: The power-up reset feature ensures that all flip-flops will be reset to low after the device has been powered up. The following conditions are required:

- The V_{CC} rise must be monotonic.
- After reset occurs, all applicable input and feedback setup times must be met before driving the clock pin high.
- The clock signal must remain stable beginning prior to the occurrence of the 10% level and continuing until the end of t_{PR} .
- $t_{PR} = 600 - 1000$ ns, Typical power-up reset voltage is 2.0 V.

FIGURE 6. Power-up Reset waveform. (Device types 01 - 02)

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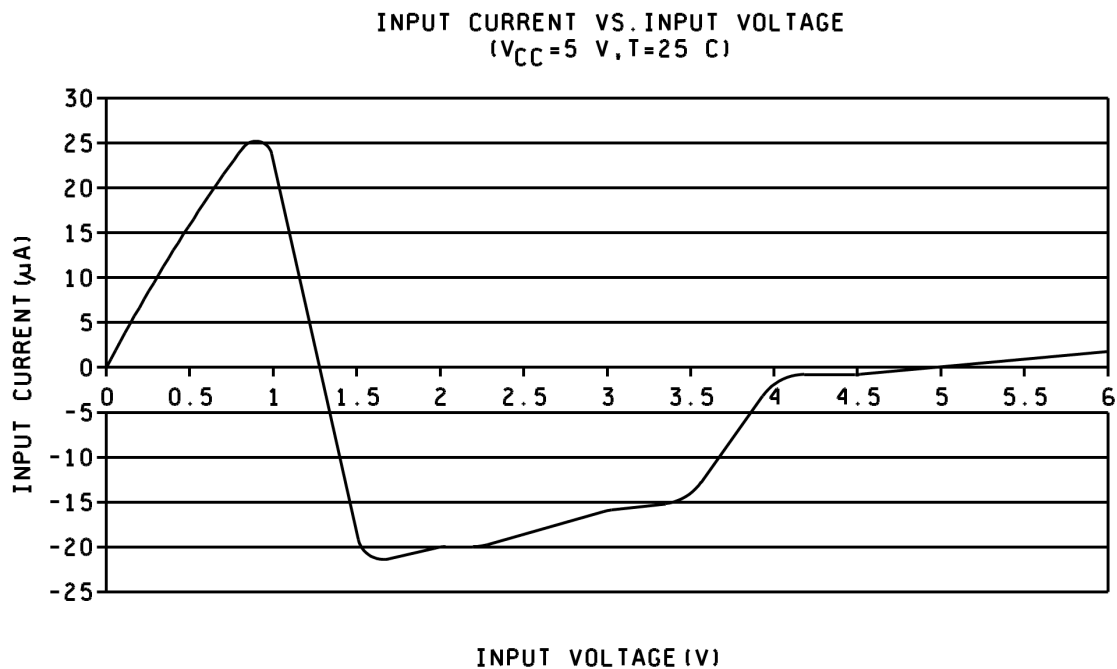


FIGURE 7. I/V Curve.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883 and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. Prior to burn-in, the devices shall be programmed (see 4.7 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.
- c. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- d. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_i and C_o measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- f. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
 - (1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
 - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d and also 4.4.1f.

Table IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I _{IH}	±10% of specified value in Table I herein
I _{IL}	±10% of specified value in Table I herein

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-09-26

Approved sources of supply for SMD 5962-07201 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-0720101MLA	0HSW3	ATF750C-10GM/883
5962-0720101M3A	0HSW3	ATF750C-10NM/883
5962-0720102MLA	0HSW3	ATF750C-15GM/883
5962-0720102M3A	0HSW3	ATF750C-15NM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

0HSW3

Vendor name
and address

Microchip Technology, Inc.
1150 East Cheyenne Mountain Blvd.
Colorado Springs, CO 80906

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.