

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to the latest requirements. Made correction to paragraph 1.3. -sld	07-04-13	Robert M. Heber
B	Added footnote 1 to table II, under group C end-point electricals. Updated drawing paragraphs. -sld	12-12-10	Charles F. Saffle
C	Updated drawing to the latest requirements of MIL-PRF-38534. -sld	19-02-19	Charles F. Saffle
D	Update drawing to the latest requirements of MIL-PRF-38534. -gc	23-09-05	James R. Eschmeyer



Revision Status of Sheets

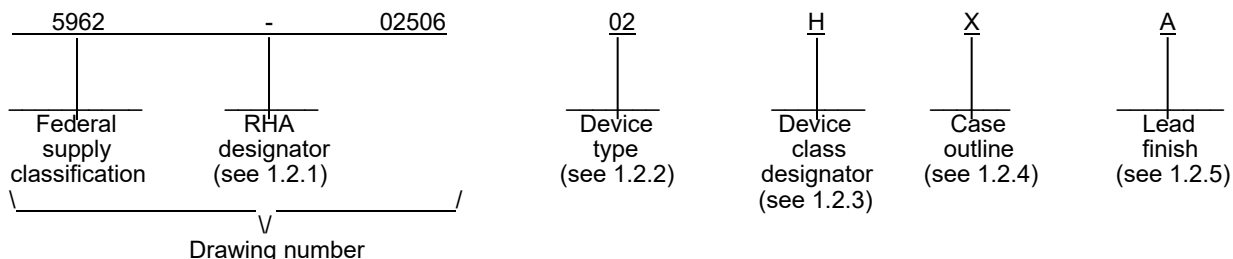
REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A		PREPARED BY Gary Zahn		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE		CHECKED BY Michael C. Jones				
		APPROVED BY Raymond Monnin				
		DRAWING APPROVAL DATE 02-01-31				
AMSC N/A		REVISION LEVEL D		SIZE A	CAGE CODE 67268	5962-02506
				SHEET	1 OF 16	

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices meet the MIL-PRF-38534 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type 1/</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>UVLO Turn-on</u>	<u>UVLO Turn-off</u>
01	52447	Phase shift resonant controller	10.75 V	9.25 V

1.2.3 Device class designator. This device class designator is a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

<u>Device class</u>	<u>Device performance documentation</u>
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1/ Device type may be similar to the device type on Standard Microcircuit Drawing (SMD) 5962-94555.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506

SHEET **2**

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CQCC1-N28B	28	Square leadless chip carrier with thermal pads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. ^{1/}

Supply voltage (V_C , V_{IN})	20 V
Output current, source or sink:	
DC	0.5 A
Pulse (0.5 μ s)	3 A
Analog I/O pins	-0.3 V to 5.3 V
Operating junction temperature (T_J)	150°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	65°C/W

1.4 Recommended operating conditions.

Supply voltage (V_C , V_{IN})	12 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-02506
		REVISION LEVEL D	SHEET 3

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 2.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime -VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime -VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-02506
		REVISION LEVEL D	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current section							
Input current startup	I _{IS}	V _{IN} = 8 V, V _C = 20 V, R _{SLOPE} = open, I _{DELAY} = 0 mA	1,2,3	01		600	μA
Output switch supply current startup	I _{IS}	V _{IN} = 8 V, V _C = 20 V, R _{SLOPE} = open, I _{DELAY} = 0 mA	1,2,3	01		100	μA
Input supply current	I _{IN}		1,2,3	01		40	mA
Output switch supply current	I _C		1,2,3	01		30	mA
Voltage reference section							
Output voltage	V _{OUT}	T _A = +25°C	1	01	4.92	5.08	V
Load regulation	V _{LD}	V _{REF} = -10 mA	1,2,3	01		20	mV
Line regulation	V _{LN}	+V _{IN} = 11 V to 20 V	1,2,3	01		10	mV
Total variation	V _T	Line, load, temperature	1,2,3	01		5.1	V
Error amplifier section							
Offset voltage	V _{IO}		1,2,3	01		15	mV
Input bias current	I _{IB}		1,2,3	01		3	μA
Open loop voltage gain	A _{VOL}	V _{COMP} = 1 V to 4 V	4,5,6	01	60		dB
Common mode rejection ratio	CMRR	V _{CM} = 1.5 V to 5.5 V	4,5,6	01	75		dB
Power supply rejection ratio	PSRR	V _{IN} = 11 V to 20 V	4,5,6	01	85		dB
Output sink current	I _{SI}	V _{COMP} = 1 V	1,2,3	01	1		mA

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506SHEET **5**

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section - Continued.							
Output source current	ISO	VCOMP = 4 V	1,2,3	01		-0.5	mA
Output voltage, high	VOH	ICOMP = -0.5 mA	1,2,3	01	4	5	V
Output voltage, low	VOL	ICOMP = 1 mA	1,2,3	01	0	1	V
Unity gain bandwidth <u>3/</u>	UGBW		4,5,6	01	5		MHz
Slew rate <u>3/</u>	SR		4,5,6	01	6		V/μs
Pulse width modulator section							
Zero phase shift voltage	VZPS	<u>4/</u>	1,2,3	01	0.55		V
Pulse width modulator <u>5/</u> phase shift	PS	VCOMP > (ramp peak + ramp offset)	4,5,6	01	98	102	%
		VCOMP < (zero phase shift voltage)			0	2	
Output skew <u>5/</u>	tOS	VCOMP < 1 V	9,10,11	01		±20	ns
Ramp to output delay	tOD		9,10,11	01		125	ns
Oscillator section							
Initial accuracy	IA	TA = +25°C	4	01	0.85	1.15	MHz
Voltage stability	VS	VIN = 11 V to 20 V	4,5,6	01		2	%
Total variation	VT	Line, temperature	1,2,3	01	0.80	1.20	MHz
Clock output pulse width	tCLKO	RCLK/SYNC = 3.9 kΩ	4,5,6	01		100	ns
Maximum frequency	fMAX	RFSET = 5 kΩ	4,5,6	01	2		MHz
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990		SIZE A	REVISION LEVEL D		5962-02506		
					SHEET 6		

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Ramp generator / slope compensation section							
Minimum ramp current	IRMIN	ISLOPE = 10 μA, VFSET = VREF	1,2,3	01		-14	μA
Maximum ramp current	IRMAX	ISLOPE = 1 mA, VFSET = VREF	1,2,3	01	-0.8		mA
Ramp peak, clamping level voltage	VCL	RFSET = 100 kΩ	1,2,3	01	3.8		V
Current limit section							
Input bias current	IIB	C+C/S = 3 V	1,2,3	01		5	μA
Threshold voltage	VTH		1,2,3	01	2.4	2.6	V
Delay to output	tDO		9,10,11	01		150	ns
SOFT-START / reset delay section							
Charge current	ICH	VS-S = 0.5 V	1,2,3	01	-20	-3	μA
Discharge current	IDCH	VS-S = 1 V	1,2,3	01	120		μA
Restart threshold voltage	VRTH		1,2,3	01	4.3		V
OUTPUT drivers section							
Output low level voltage	VOL	IOUT = 50 mA	1,2,3	01		0.4	V
Output high level voltage	VOH	IOUT = -50 mA	1,2,3	01		2.5	V
DELAY SET section							
DELAY SET voltage	VDS	IDELAY = -500 μA	1,2,3	01	2.3	2.6	V
DELAY time	tD	IDELAY = -250 μA	9,10,11	01	150	600	ns
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990		SIZE A			5962-02506		
			REVISION LEVEL D		SHEET 7		

TABLE I. Electrical performance characteristics - Continued.

- 1/ Unless otherwise specified, $V_S = +V_{IN} = 12\text{ V}$, frequency set resistance $R_{FSET} = 12\text{ k}\Omega$, frequency set capacitance $C_{FSET} = 330\text{ pF}$, slope resistance $R_{SLOPE} = 12\text{ k}\Omega$, ramp capacitance $C_{RAMP} = 200\text{ pF}$, DELAY SET capacitance $C_{DS\ A-B} = C_{DS\ C-D} = 0.01\text{ }\mu\text{F}$, DELAY SET current $I_{DS\ A-B} = I_{DS\ C-D} = -500\text{ }\mu\text{A}$.
- 2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ Not production tested.
- 4/ Zero phase shift voltage has a temperature coefficient of about $-2\text{ mV}/^\circ\text{C}$.
- 5/ Phase shift percentage ($0\% = 0^\circ$, $100\% = 180^\circ$) is defined as: $\theta = (200/T)\phi\%$. θ is the phase shift, and ϕ and T are defined in figure 3. At 0% phase shift, ϕ is the output skew.
- 6/ Delay time can be programmed via resistors from the delay set pins to ground. Delay time = $(62.5 \times 10^{-12})\text{ seconds}/I_{DELAY}$. $I_{DELAY} = \text{delay set voltage}/R_{DELAY}$. The recommended range for I_{DELAY} is $25\text{ }\mu\text{A} \leq I_{DELAY} \leq 1\text{ mA}$.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-02506

REVISION LEVEL
D

SHEET **8**

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	V _{IN}
2	PWR GND
3	OUTPUT B (OUT B)
4	OUTPUT A (OUT A)
5	NC
6	NC
7	DELAY SET A/B
8	FREQ SET
9	CLOCK/SYNC
10	SLOPE
11	RAMP
12	NC
13	NC
14	GND
15	NC
16	V _{REF}
17	E/A OUT
18	NC
19	NC
20	E/A (-)
21	E/A (+)
22	C/S (+)
23	SOFTSTART
24	DELAY SET C/D
25	NC
26	OUTPUT D (OUT D)
27	OUTPUT C (OUT C)
28	V _C

NC = No connection

FIGURE 1. Terminal connections.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-02506

REVISION LEVEL
D

SHEET **9**

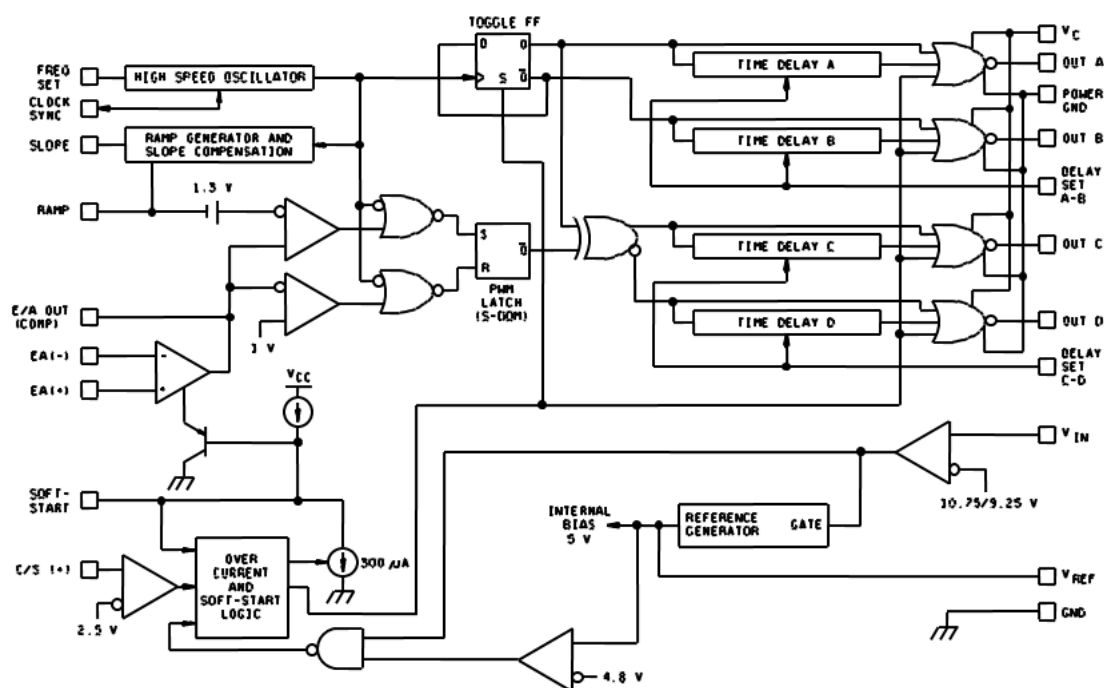


FIGURE 2. Logic diagram.

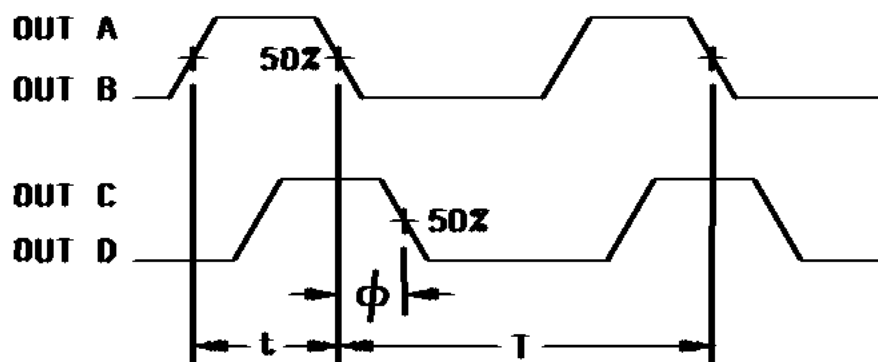
**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506

SHEET **10**



Phase shift, output skew and delay time definitions.

Duty cycle = t/T . Period = T . $T_{DHL} (A \text{ to } C) = T_{DHL} (B \text{ to } D) = \phi$

FIGURE 3. Timing diagram.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506

SHEET **11**

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	---
Final electrical parameters	1*,2,3,4,5,6,9,10,11
Group A test requirements	1,2,3,4,5,6,9,10,11
Group C end-point electrical <u>1/</u> parameters	1,2,3,4
Group D end-point electrical parameters	1,4
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

1/ As a minimum, for all Group C testing performed after (12-12-10) manufacturers shall perform subgroups 1, 2, and 3 from the Group A electrical test table (Table C-Xa of MIL-PRF-38534).

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) TA as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506

SHEET **12**

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Sample size shall be 116(0) for all tests.
- b. Tests shall be as specified in table II herein.
- c. Subgroups 7, and 8 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Sample size for bond strength is 22(0), resistance to solvents and die sheer is 3(0) for each test.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883. Sample size is 45(0).
 - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime -VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) TA as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- c. Subgroup 1 shall consist of the following:
 - (1) Temperature cycle and thermal shock.
 - (2) Mechanical shock, constant acceleration, and PIND.
 - (3) Physical dimensions 15(0).

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534. Sample size is 15(0).

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-02506
		REVISION LEVEL D	SHEET 13

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors, listed in MIL-HDBK-103 and QML-38534, have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-02506
		REVISION LEVEL D	SHEET 14

6.7 Abbreviations, symbols, and definitions.

GND	Signal ground. All voltages are measured with respect to ground (GND). The timing capacitor, on the FREQ SET pin, and bypass capacitor on the V _{REF} pin, bypass capacitors on V _{IN} and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.
PWR GND	Power ground. V _C should be bypassed with a ceramic capacitor from the V _C pin to the section of the ground plane that is connected to PWR GND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a signal point to optimize noise rejection and minimize DC drops.
V _C	Output switch supply voltage. This pin supplies power to the drivers and their associated bias circuitry. Connect V _C to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWR GND pin with low ESR, low ESL capacitors.
V _{IN}	Primary chip supply voltage. This pin supplies power to the logic and analog circuitry on the integrated circuitry that is not directly associated with driving the output stages.
FREQ SET	Oscillator frequency set pin. A resistor and a capacitor from FREQ SET to GND will set oscillator frequency according to the following relationship: $f = 4/(R_{SET} \times C_{RAMP})$.
CLK/SYNC	Bi-directional clock and synchronization pin. Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point.
SLOPE	Set ramp slope. Slope compensation. A resistor from this pin to V _{CC} will set the current used to generate the ramp. Connecting this resistor to the DC input line will provide voltage feed forward.
RAMP	Voltage ramp. This pin is the input to the pulse width modulator comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope: $(dV/dT) = (\text{sense voltage}/R_{SLOPE} \times C_{RAMP})$.
E/A OUT (COMP)	Error amplifier output. This is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.
E/A(+)	This pin is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A(-) pin.
E/A(-)	This pin is normally connected to the voltage divider resistors which sense the power supply output level.
SOFT START	SOFT START will remain at GND as long as V _{IN} is below the UVLO threshold. SOFT START will be pulled up to about 4.8 V by an internal 9 μA current source when V _{IN} becomes valid (assuming a non-fault condition). In the event of a current-fault (C/S (+) voltage exceeding 2.5 V), SOFT START will be pulled to GND and then ramp to 4.8 V. If a fault occurs during the SOFT START cycle, the outputs will be immediately disabled and SOFT START must charge fully prior to resetting the fault latch. For paralleled controllers, the SOFT START pins may be paralleled to a single capacitor, but the change currents will be additive.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
D

5962-02506

SHEET **15**

CURRENT SENSE (+)	The positive input to the current-fault comparator whose reference is set internally to fixed 2.5 V (separate from V _{REF}). When the voltage at this pin exceeds 2.5 V, the current-fault latch is set, the outputs are forced off and a SOFT START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the C/S (+) pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFT START pin begins to rise, this condition will not prematurely deliver power to the load.
OUTPUTS A, B, C, D	The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level shifting transformers. The outputs operate as pair with a nominal 50% duty cycle. The A-B pair is intended to drive one half bridge in the external power stage and is synchronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.
DELAY SET A-B, DELAY SET C-D	Output delay control. The users programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half bridges to accommodate differences in the resonant capacitor charging currents.
V _{REF}	This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-02506

REVISION LEVEL
D

SHEET **16**

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-09-05

Approved sources of supply for SMD 5962-02506 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revision. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u> <u>2/</u>	Vendor CAGE number	Vendor similar PIN <u>3/</u>
5962-0250601HXA	31757	52447
5962-0250601HXC	31757	52447

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Device types may be similar to the device types on Standard Microcircuit Drawing (SMD) 5962-94555.
- 3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

31757

Vendor name
and address

Micropac Industries Incorporated
905 East Walnut Street
Garland, TX 75040

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.