

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED



Revision Status of Sheets

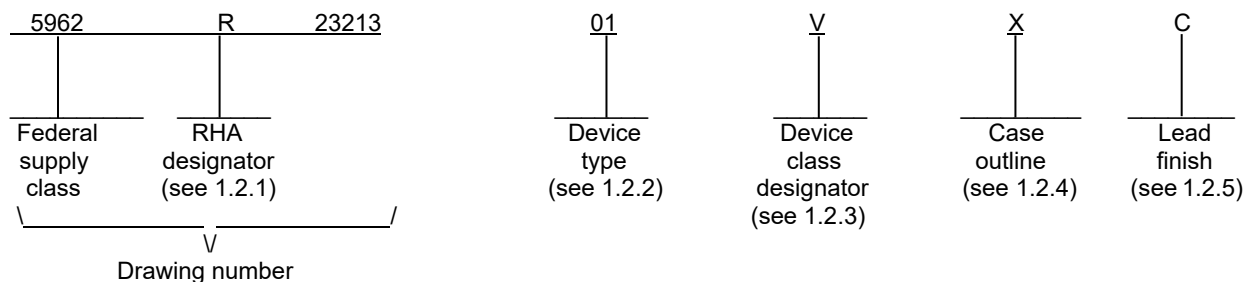
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PMIC N/A				
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY Ron E Pompey	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
	CHECKED BY Rajesh Pithadia			
	APPROVED BY James R. Eschmeyer	MICROCIRCUIT, DIGITAL, CMOS, FERROELECTRIC RANDOM ACCESS MEMORY (FRAM), MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 24-09-16			
AMSC N/A	REVISION LEVEL	SIZE A	CAGE CODE 67268	5962-23213
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Access Time	Endurance
01	CYRS15B102N	Parallel FRAM with ECC, 2.0-3.6 Volt, Radiation Hardened, (128k x16)	9 MHz	1 x 10 ¹³ cycles
02	CYRS15B101N	Parallel FRAM with ECC, 2.0-3.6 Volt, Radiation Hardened, (64k x16)/(128k x8)	9 MHz	1 x 10 ¹³ cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	44	Ceramic Thin Small Outline Package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-1.0 V dc to +4.5 V dc
DC input voltage range (V_{IN})	-1.0 V dc to +4.5 V dc and $V_{IN} < V_{DD}$ +1.0 V dc <u>2/</u>
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{DD} + 0.5$ V dc <u>2/</u>
Storage temperature range	-65°C to +150°C
Case operating free-air temperature range, (T_C)	-55°C to +125°C
Lead temperature (soldering 3 seconds)	+260°C
Thermal resistance, junction to case (θ_{JC})	25°C/W
Maximum power dissipation	0.036 W @ 25 MHz
Maximum junction temperature (T_J)	130°C
Data retention:	
$T_C = 125^\circ\text{C}$	11k hours
$T_C = 105^\circ\text{C}$	11 years
$T_C = 85^\circ\text{C}$	121 years
Write cycle endurance	1×10^{13} cycles <u>3/</u>

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V_{DD})	2.0 V dc to 3.6 V dc
Supply voltage reference (GND)	0.0 V dc
High level input voltage range (V_{IH})	1.4 V to V_{DD}
Low level input voltage range (V_{IL})	0.0 V dc to 1.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features.

Maximum total ionizing dose available (High dose rate = 50 - 300 rad(Si)/s)	= 100 krad(Si) <u>5/</u>
Maximum total ionizing dose available (Reduced dose rate = 10 rad(Si)/s)	= 100 krad(Si) <u>5/</u>
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.4) at 115°C	≤ 96 MeV-cm ² /mg) <u>6/</u>
Single event upset (SEU) error rate at in-situ LET 2.5 MeV-cm ² /mg	= 5.3×10^{-5} error /dev-day <u>6/</u>
No dose rate induced upset – static	≤ 1.1×10^{11} rad(Si)/sec <u>7/</u>
Dose rate induced functional upset – R/W	= 1.1×10^8 rad(Si)/sec <u>7/</u>
Dose rate survivability (RS)	= 1.1×10^{11} rad(Si)/sec <u>7/</u>
Neutron irradiation (1 MeV equivalent)	= 2×10^{14} neutrons/cm ²

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum or minimum levels may degrade performance and affect reliability.
- 2/ All voltages are reference to GND and maximum applied voltage shall not exceed +4.5 V.
- 3/ Endurance assumes a 50% write 1's and 50% write 0's.
- 4/ Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents.
Power-up sequence: GND, V_{DD} , Inputs. Power-down sequence: Inputs, V_{DD} , GND.
- 5/ Manufacturer supplying device type 01 has been tested total ionizing dose (TID) test in accordance with MIL-STD-883, method 1019, condition A to a maximum TID level of 150 krad(Si) and condition C to a maximum TID level of 200 krad(Si). However, devices marked to standard 100 krad(Si) of RHA TID level R. For details TID test report, please contact manufacturer.
- 6/ Heavy ion single event effects (SEE) test was performed at the Berkely NL Cyclotron facility. No SEL was observed at fluence 10^7 ions/cm² and $T_A=115^\circ\text{C}$ with an effective LET 96 MeV-cm²/mg. For Single Event Functional Interrupt (SEFI) error rate = 5.3×10^{-5} errors/dev-day consider CREME96 Geosynchronous orbit. For details SEE test report contact the device manufacturer.
- 7/ Flash X-ray (FXR) test and detailed test reports can be requested by the customer through the purchase order.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org/>.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 22-A117 - Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test.

JESD 47 - Stress-Test-Driven Qualification of Integrated Circuits.

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at <https://www.jedec.org/>.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Write cycle endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific but shall guarantee the number of program/erase endurance cycles listed in section 1.3 here in over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data. Testing may be done per JESD 22-A117 and JESD 47.

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TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 2.0 V ≤ V _{DD} ≤ 3.6 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply Current	I _{DD}	F _{SCK} = 25 MHz SCK toggling between V _{DD} − 0.2 V and V _{SS} , other inputs V _{SS} or V _{DD} − 0.2 V.		1, 2, 3	All		10	mA
Supply Current (Standby)	I _{SB}	V _{DD} = 3.6 V, $\overline{CE}$ at V _{DD} , All other pins are static and at CMOS levels (0.2 V or V _{DD} − 0.2 V), $\overline{ZZ}$ is HIGH	TID = 0 krad	1, 2, 3	All	--	700	μA
			TID = 150 krad	1, 2, 3	All	--	6	mA
Supply Current (Sleep)	I _{ZZ}	V _{DD} = 3.6 V, $\overline{ZZ}$ is LOW, All other pins V _{SS} or V _{DD}	TID = 0 krad	1, 2, 3	All	--	20	μA
			TID = 150 krad	1, 2, 3	All	--	8	mA
High level output voltage	V _{OH1}	I _{OH} = -1 mA, V _{DD} > 2.7V		1, 2, 3	All	2.4	--	V
	V _{OH2}	I _{OH} = -100μA		1, 2, 3	All	V _{DD} − 0.2	--	V
Low level output voltage	V _{OL1}	I _{OH} = 2 mA, V _{DD} > 2.7V		1, 2, 3	All	--	0.4	V
	V _{OL2}	I _{OH} = 150μA		1, 2, 3	All	--	0.2	V
High level input voltage	V _{IH1}	V _{DD} = 2.7V to 3.6V		1, 2, 3	All	2.2	V _{DD} + 0.3	V
	V _{IH2}	V _{DD} = 2.0V to 2.7V		1, 2, 3	All	0.7 × V _{DD}	--	V
Low level input voltage	V _{IL1}	V _{DD} = 2.7V to 3.6V		1, 2, 3	All	-0.3	0.8	V
	V _{IL2}	V _{DD} = 2.0V to 2.7V		1, 2, 3	All	-0.3	0.3 × V _{DD}	V
Input leakage current	I _{ILK}	V _{SS} < V _{IN} < V _{DD}		1, 2, 3	All	-10	10	μA
Output leakage current	I _{OLK}	V _{SS} < V _{OUT} < V _{DD}		1, 2, 3	All	-10	10	μA
Input Capacitance	C _{IN}	See 4.4.1e		4	All	--	6	pF
Output Capacitance	C _{OUT}			4	All	--	8	pF
Functional tests		See 4.4.1c		7, 8A, 8B	All			
Chip enable access time	t _{CE}	V _{DD} = 2.0V to 2.7V		9, 10, 11	All	--	70	ns
		V _{DD} = 2.7V to 3.6V		9, 10, 11	All	--	60	ns
Read cycle time	t _{RC}	V _{DD} = 2.0V to 2.7V		9, 10, 11	All	105	--	ns
		V _{DD} = 2.7V to 3.6V		9, 10, 11	All	90	--	ns
Address access time, A ₁₆₋₂	t _{AA}	V _{DD} = 2.0V to 2.7V		9, 10, 11	All	--	105	ns
		V _{DD} = 2.7V to 3.6V		9, 10, 11	All	--	90	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output hold time, A ₁₆₋₂	t _{OH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	20	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	20	--	ns
Page mode access time, A ₁₋₀	t _{AAP}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	40	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	30	ns
Page mode output hold time, A ₁₋₀	t _{OHP}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	3	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	3	--	ns
Chip enable active time	t _{CA}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	70	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	60	--	ns
Precharge time	t _{PC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	35	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	30	--	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ access time	t _{BA}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	25	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	15	ns
Address setup time (to CE LOW)	t _{AS}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	0	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	0	--	ns
Address hold time (CE Controlled)	t _{AH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	70	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	60	--	ns
Output enable access time	t _{OE}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	25	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	15	ns
Chip enable to output HI-Z <u>3/ 4/</u>	t _{HZ}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	15	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	10	ns
Output enable HIGH to output HI-Z <u>3/ 4/</u>	t _{OHZ}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	15	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	10	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ HIGH to output HI-Z <u>3/ 4/</u>	t _{BHZ}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	15	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	10	ns
Write cycle time	t _{WC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	105	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	90	--	ns
Chip enable active time	t _{CA}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	70	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	70	--	ns
Chip enable to write enable HIGH	t _{CW}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	70	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	70	--	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Precharge time	t _{PC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	35	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	30	--	ns
Page mode write enable cycle time	t _{PWC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	40	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	40	--	ns
Write enable pulse width	t _{WP}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	22	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	18	--	ns
UB, LB pulse width	t _{WP2}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	22	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	18	--	ns
WE LOW to UB, LB HIGH	t _{WP3}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	22	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	18	--	ns
Address setup time (to CE LOW)	t _{AS}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	0	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	0	--	ns
Address hold time (CE Controlled)	t _{AH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	70	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	60	--	ns
Page mode address setup time (to WE LOW)	t _{ASP}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	8	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	5	--	ns
Page mode address hold time (to WE LOW)	t _{AHP}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	20	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	15	--	ns
Write enable LOW to chip disabled	t _{WLC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	30	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	25	--	ns
UB, LB LOW to chip disable	t _{BLC}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	30	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	25	--	ns
Write enable LOW to address change, A ₁₆₋₂	t _{WLA}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	30	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	25	--	ns
Address change to write enable HIGH, A ₁₆₋₂	t _{AWH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	105	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	90	--	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data input setup time	t _{DS}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	105	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	90	--	ns
Data input hold time	t _{DH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	0	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	0	--	ns
Write enable LOW to output HI-Z <u>4/</u> <u>5/</u>	t _{WZ}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	--	10	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	--	10	ns
Write enable HIGH to output driven <u>4/</u> <u>5/</u>	t _{WX}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	10	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	8	--	ns
Byte disable setup time (to $\overline{WE}$ LOW)	t _{BDS}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	8	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	5	--	ns
Byte disable hold time (to $\overline{WE}$ LOW)	t _{BDH}	V _{DD} = 2.0V to 2.7V	9, 10, 11	All	8	--	ns
		V _{DD} = 2.7V to 3.6V	9, 10, 11	All	5	--	ns

1/ RHA devices supplied to this drawing have been characterized through all level M, D, P, L and R of irradiation. However, this device is only tested at the "R" level at the dose rate condition A and C. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Test conditions are defined at inception of test. The device is first stabilized at the desired temperature in an unpowered state to ensure that the module is at the desired case temperature (T_C) before parameters are measured. The case temperature (T_C) is maintained during testing at the specified temperature by a forced air test environment.

Test conditions for AC measurements are listed below.

Input Levels: 0 V to 3 V

Input rise and fall time: < 3.0 ns

Input and output timing reference levels: 1.5 V

Output load capacitance: 30 pF

3/ t_{HZ}, t_{OHZ} and t_{BHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.

4/ This parameter is characterized but not 100% tested.

5/ t_{WZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high-impedance state.

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Table IB. SEP test limits 1/ 2/

Device type	Single Event Functional Interrupt (SEFI) error rate $V_{DD} = 2.0 \text{ V}$ and $T_A = +25^\circ\text{C}$,	Single Event Latch-up (SEL) test Bias $V_{DD} = 3.6 \text{ V}$
	SEFI error rate at Onset LET $\approx 2.5 \text{ MeV}/(\text{mg}/\text{cm}^2)$ 3/	Effective LET No SEL occurs 3/
All	5.3×10^{-5} error/dev-day	$\text{LET} \leq 96 \text{ MeV}/(\text{mg}/\text{cm}^2)$

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Heavy ion single event effects (SEE) test was performed at the Berkely NL Cyclotron facility. No SEL was observed at fluence 10^7 ions/ cm^2 and $T_A = 115^\circ\text{C}$ with an effective LET $96 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. For Single Event Functional Interrupt (SEFI) error rate $= 5.3 \times 10^{-5}$ errors/dev-day consider CREME96 Geosynchronous orbit. For details SEE test report contact the device manufacturer.

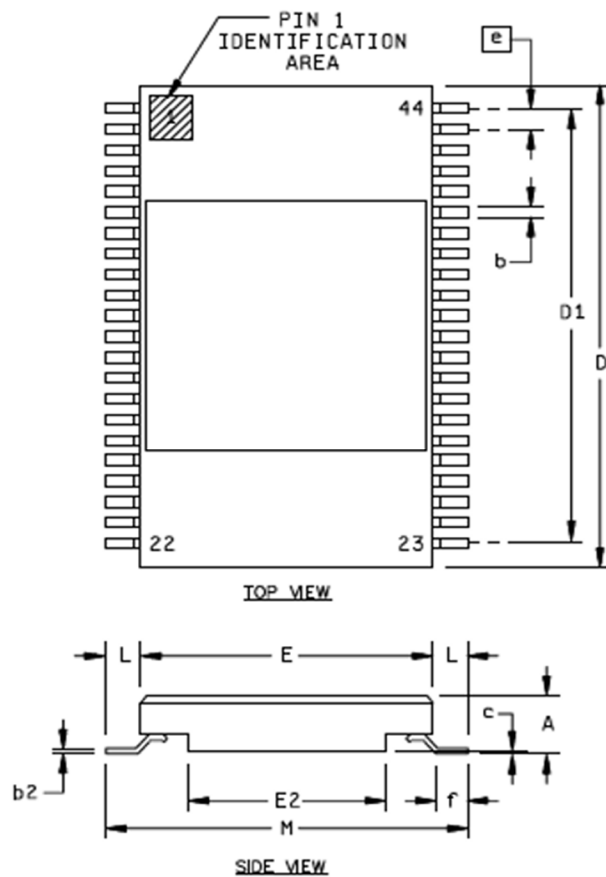
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Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Min		Min	Max	Min	Min
A	2.986	3.842	0.117	0.151	E	9.96	10.36	0.392	0.408
b	0.300	0.400	0.012	0.016	E2	5.280	5.680	0.208	0.224
b2	0.150	0.250	0.006	0.010	e	0.80 BSC		0.03 BSC	
c	0.05	---	0.002	---	f	0.406	0.597	0.016	0.024
D	18.215	18.615	0.717	0.733	L	0.839 NOM (ref)		0.033 NOM (ref)	
D1	16.60	17.00	0.654	0.669	M	11.735	11.938	0.462	0.470
N	44		---						

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Controlling dimensions are millimeters, inch dimensions are given for reference only.

FIGURE 1. Case outline.

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Device types	01	02	
Case outlines	X		
Device configuration	128k x 16	64k x 16	128k x 8
Terminal number	Terminal symbol		
1	A ₄	A ₄	A ₄
2	A ₃	A ₃	A ₃
3	A ₂	A ₂	A ₂
4	A ₁	A ₁	A ₁
5	A ₀	A ₀	A ₀
6	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
7	DQ ₀	DQ ₀	DQ ₀
8	DQ ₁	DQ ₁	DQ ₁
9	DQ ₂	DQ ₂	DQ ₂
10	DQ ₃	DQ ₃	DQ ₃
11	V _{DD}	V _{DD}	V _{DD}
12	V _{SS}	V _{SS}	V _{SS}
13	DQ ₄	DQ ₄	DQ ₄
14	DQ ₅	DQ ₅	DQ ₅
15	DQ ₆	DQ ₆	DQ ₆
16	DQ ₇	DQ ₇	DQ ₇
17	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
18	A ₁₆	V _{SS}	A ₁₆
19	A ₁₅	A ₁₅	A ₁₅
20	A ₁₄	A ₁₄	A ₁₄
21	A ₁₃	A ₁₃	A ₁₃
22	A ₁₂	A ₁₂	A ₁₂

FIGURE 2. Terminal connections.

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Device types	01	02	
Case outlines	X		
Device configuration	128k x 16	64k x 16	128k x 8
Terminal number	Terminal symbol		
23	NC	NC	NC
24	A ₁₁	A ₁₁	A ₁₁
25	A ₁₀	A ₁₀	A ₁₀
26	A ₉	A ₉	A ₉
27	A ₈	A ₈	A ₈
28	$\overline{ZZ}$	$\overline{ZZ}$	$\overline{ZZ}$
29	DQ ₈	DQ ₈	V _{SS}
30	DQ ₉	DQ ₉	V _{SS}
31	DQ ₁₀	DQ ₁₀	V _{SS}
32	DQ ₁₁	DQ ₁₁	V _{SS}
33	V _{DD}	V _{DD}	V _{DD}
34	V _{SS}	V _{SS}	V _{SS}
35	DQ ₁₂	DQ ₁₂	V _{SS}
36	DQ ₁₃	DQ ₁₃	V _{SS}
37	DQ ₁₄	DQ ₁₄	V _{SS}
38	DQ ₁₅	DQ ₁₅	V _{SS}
39	$\overline{LB}$	$\overline{LB}$	V _{SS}
40	$\overline{UB}$	$\overline{UB}$	V _{DD}
41	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
42	A ₇	A ₇	A ₇
43	A ₆	A ₆	A ₆
44	A ₅	A ₅	A ₅

Note: NC labeled connections are not internally connected to the die and floating.

FIGURE 2. Terminal connections - Continued.

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Functional

$\overline{CE}$	$\overline{WE}$	A_{16-2} / A_{15-2}	A_{1-0}	$\overline{ZZ}$	Operation <u>1/</u> <u>2/</u>
X	X	X	X	L	Sleep Mode
H	X	X	X	H	Standby/Idle
↓ L	H H	V V	V V	H H	Read
L	H	No Change	Change	H	Page Mode Read
L	H	Change	V	H	Random Read
↓ L	L L	V V	V V	H H	$\overline{CE}$ – Controlled Write <u>2/</u>
L	↓	V	V	H	$\overline{WE}$ – Controlled Write <u>2/</u> <u>3/</u>
L	↓	No Change	V	H	Page Mode Write <u>4/</u>
↑ L	X X	X X	X X	H H	Starts precharge

1/ H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.

2/ For write cycles, data-in is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever comes first.

3/ $\overline{WE}$ -controlled write cycle begins as a Read cycle and then A_{16-2} (for device type 01 and 02 – configuration 128k x 8) or A_{15-2} (for device type 02 – configuration 64k x 16) is latched.

4/ Addresses A_{1-0} must remain stable for at least 15 ns during page mode operation.

Byte Select

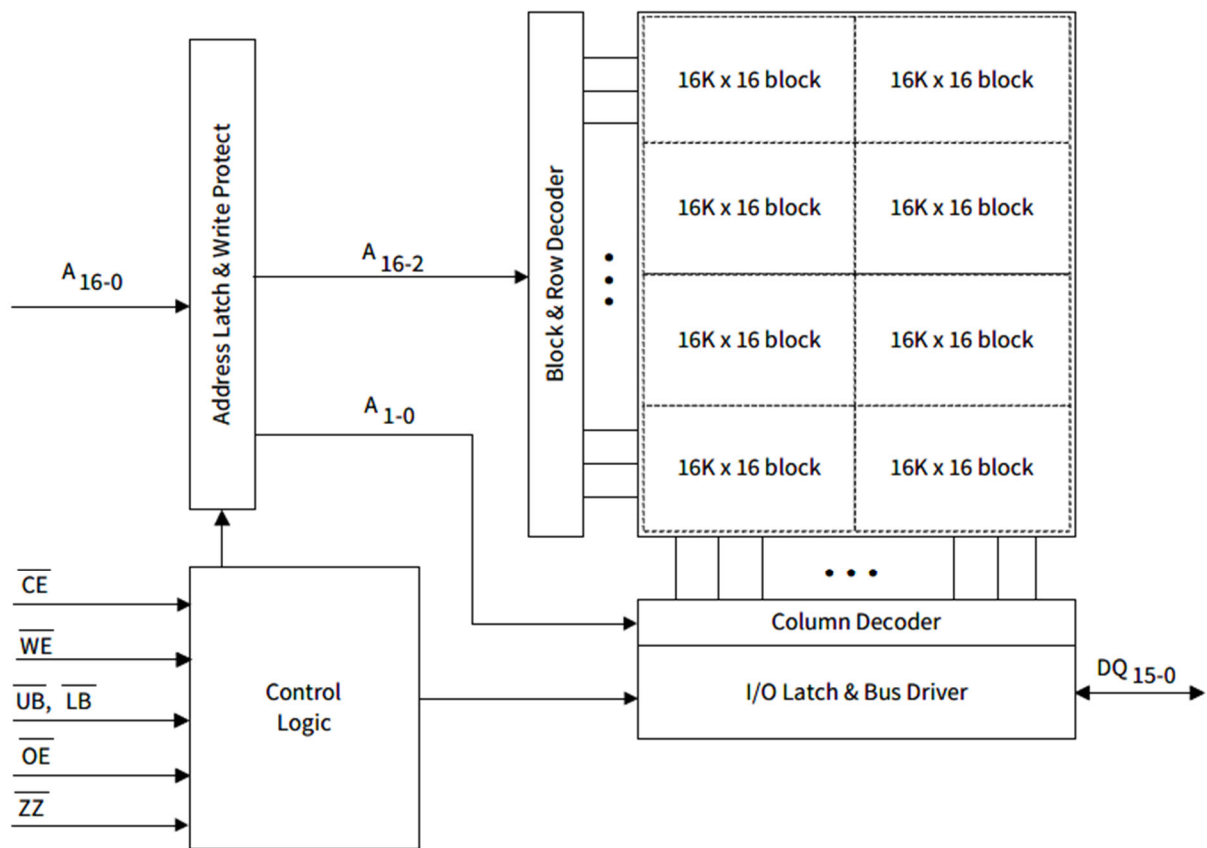
$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Operation <u>1/</u>
H	H	X	X	Read; Outputs disabled
	X	H	H	
H	L	H	L	Read upper byte; HI-Z lower byte
		L	H	Read upper byte; HI-Z upper byte
		L	L	Read both bytes
L	X	H	L	Write upper byte; HI-Z lower byte
		L	H	Write upper byte; HI-Z upper byte
		L	L	Write both bytes

1/ The $\overline{UB}$ and $\overline{LB}$ pins may be grounded if the system does not perform byte writes and the device is not configured as a 128k x 8 (device type 02).

FIGURE 3. Truth tables.

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Device Type 01 (128k x 16 Configuration)

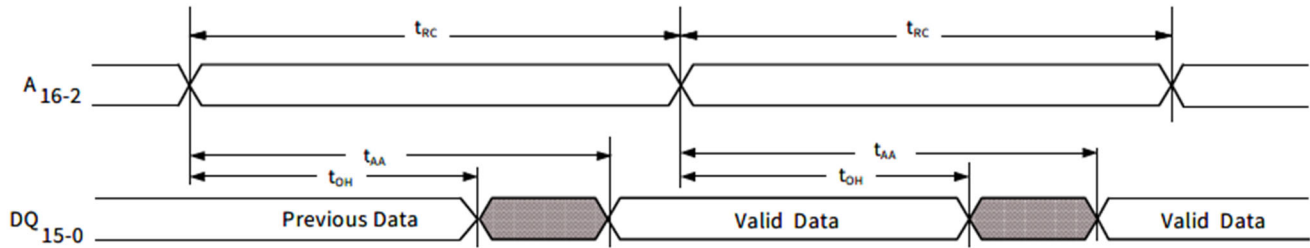


Note: For Device type 02: 64k x 16 configuration A_{16-x} is replaced with A_{15-x} and 128k x 8 configuration DQ_{15-x} is replaced with DQ_{7-x}

FIGURE 4. Block diagram.

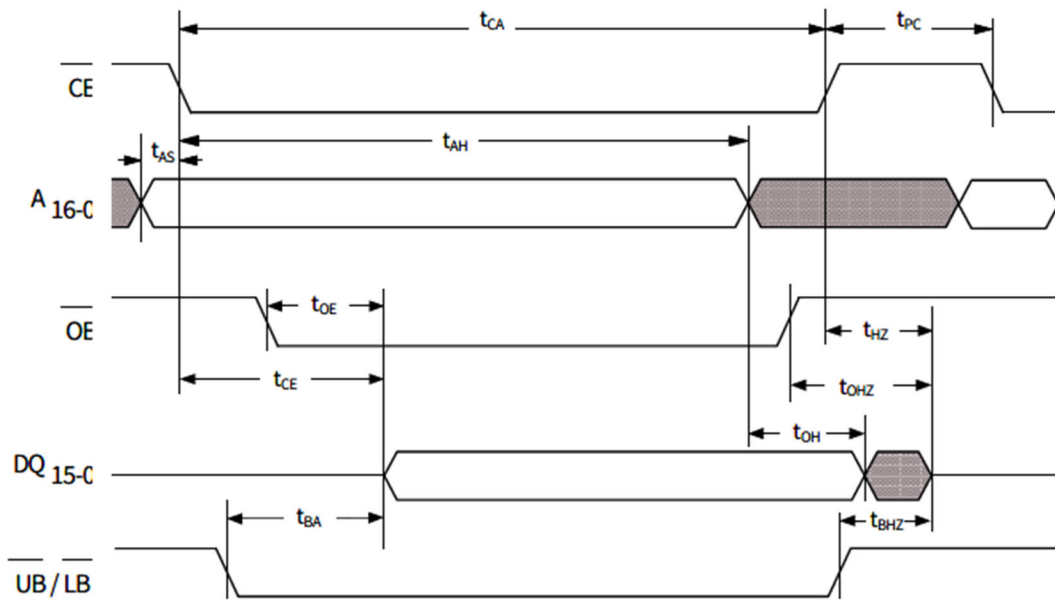
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Read Cycle No.1 ($\overline{CE}$ LOW, $\overline{OE}$ LOW)



Note: For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

Read Cycle No.2 ($\overline{CE}$ controlled)



Note: For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

FIGURE 5. Timing waveforms.

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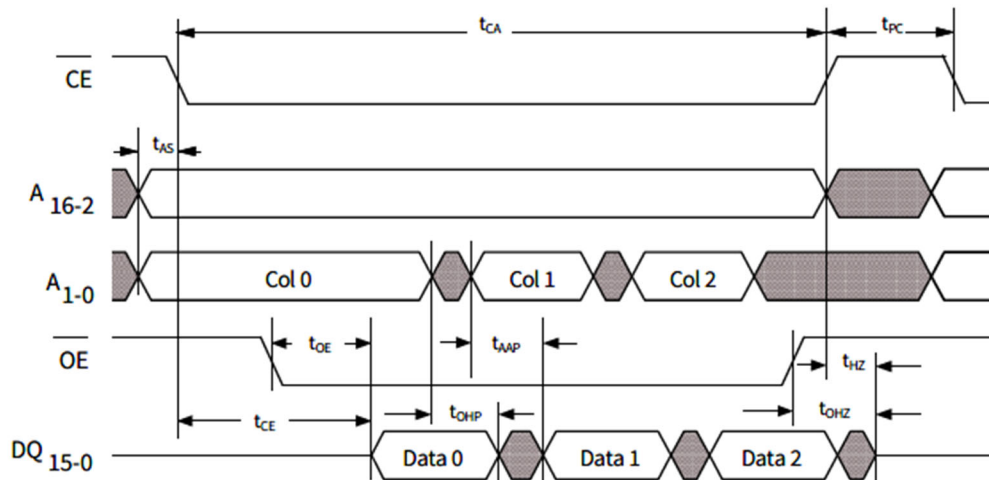
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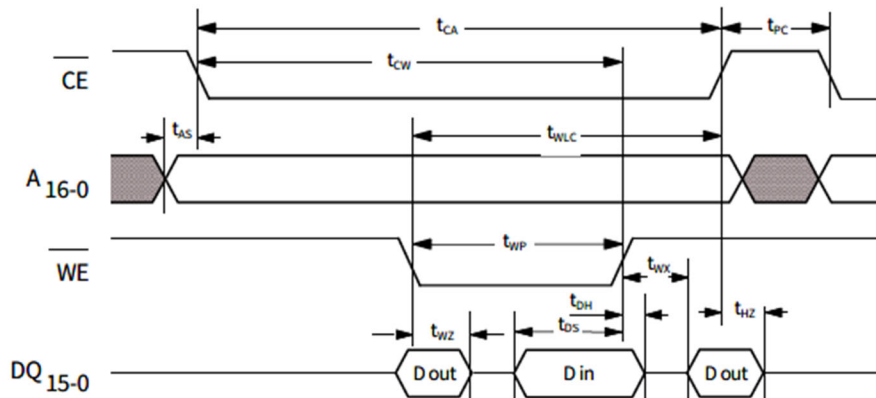
Page Mode Read Cycle



Note:

1. Although sequential column addressing is shown, it is not required.
2. For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

Write Cycle No.1 ($\overline{WE}$ controlled)



Note:

1. $\overline{OE}$ (not shown) is LOW only to show the effect of $\overline{WE}$ on DQ pins.
2. For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

FIGURE 5. Timing waveforms - Continued.

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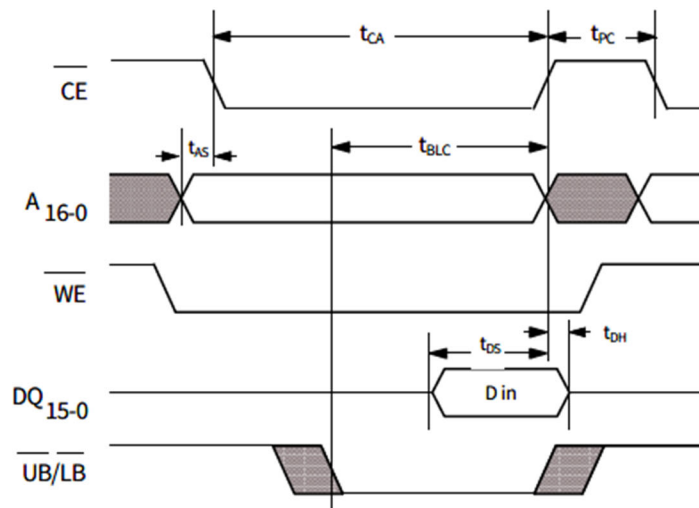
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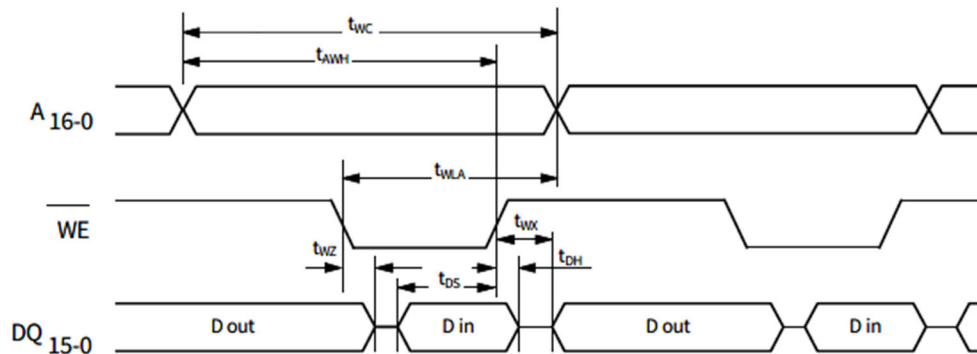
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Write Cycle No.2 ($\overline{CE}$ controlled)



Note: For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

Write Cycle No.3 ($\overline{CE}$ LOW)



Note:

1. $\overline{OE}$ (not shown) is LOW only to show the effect of $\overline{WE}$ on DQ pins.
2. For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

FIGURE 5. Timing waveforms - Continued.

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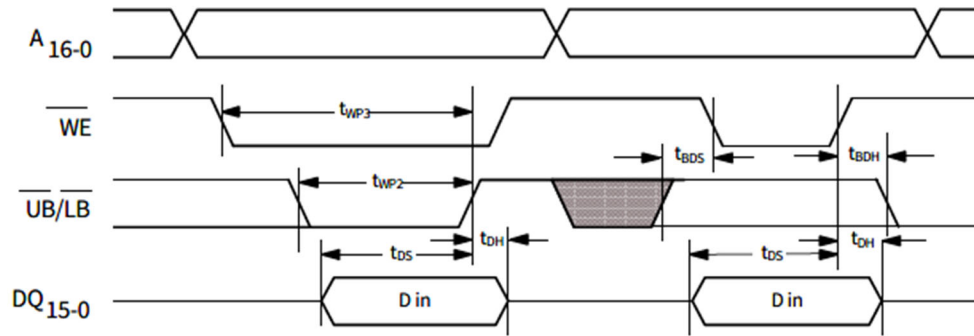
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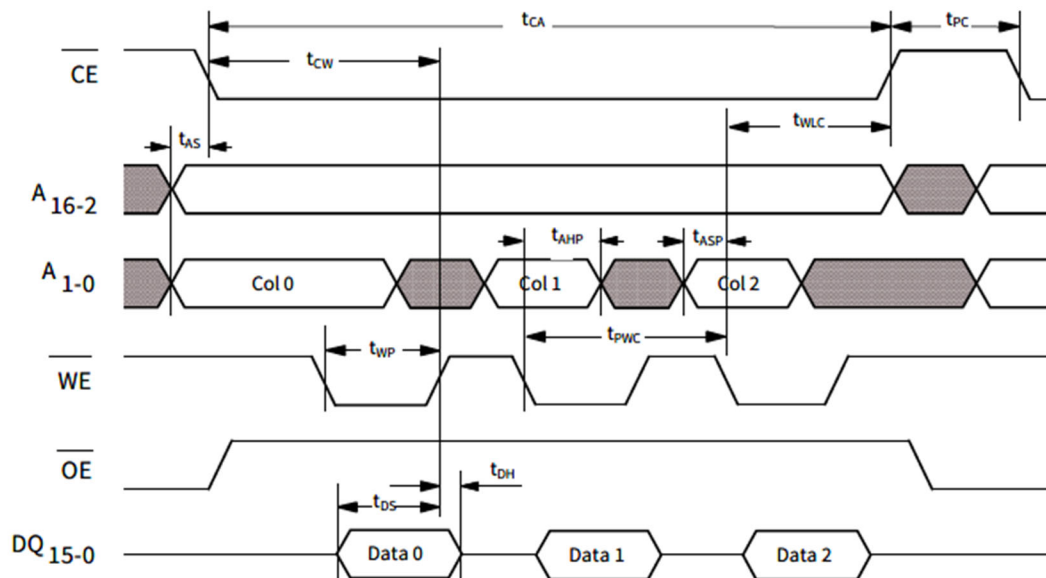
Write Cycle No.4 ($\overline{CE}$ LOW)



Note:

1. $\overline{UB}$ and $\overline{LB}$ to show byte enable and byte masking cases.
2. For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

Page Mode Write Cycle



Note: For Device type 02: 64k x 16 configuration A_{16-X} is replaced with A_{15-X} and 128k x 8 configuration DQ_{15-X} is replaced with DQ_{7-X}

FIGURE 5. Timing waveforms - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. In addition, special test structures may be used for latch-up characterization in place of using product. If test structures are used, testing shall be on five wafers. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1*, 7*, 9
Static burn-in (method 1015)	Not Required	Required
Same as line 1		1*, 7*, 9 Δ
Dynamic burn-in (method 1015)	Required	Required
Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limits	Units
I _{DD}	± 10% of the measured value	mA
I _{SB} , I _{ZZ}	± 10% of the measured value	μA
I _{ILK} , I _{OLK}	± 1	μA
V _{OH} , V _{OL}	± 10% of the measured value	mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and condition C as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} + 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$. The latch-up test temperature shall be at 115°C .
- f. Bias conditions shall be V_{DD} maximum = 2.0 V dc for the upset measurements and V_{DD} max = 3.6 V dc for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

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4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at $T_A = +25\text{ }^{\circ}\text{C} \pm 5\text{ }^{\circ}\text{C}$ after an exposure of 2×10^{12} neutrons/cm² (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Occurrence of latch-up (SEL).

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APPENDIX A
Appendix A forms a part of SMD 5962-23213
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 1.4 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.

- Step 1. Increment address from minimum to maximum writing each address with solid data pattern (xFF).
- Step 2. Increment address from minimum to maximum while performing 2a and 2b.
- Step 2a. Read and verify an address.
- Step 2b. Write the address with complement data.
- Step 3. Increment address from minimum to maximum while performing 3a, 3b, 3c, 3d.
- Step 3a. Read and verify an address.
- Step 3b. Write the address with complement data.
- Step 3c. Read and verify the address.
- Step 3d. Write the address with complement data.

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APPENDIX A – Continued.
Appendix A forms a part of SMD 5962-23213
FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solid.

- Step 1. Write x55 data pattern to all addresses from minimum to maximum.
- Step 2. Read and verify x55 data pattern at all addresses.
- Step 3. Write xAA data pattern to all addresses from minimum to maximum.
- Step 4. Read and verify xAA data pattern at all addresses.
- Step 5. Write xFF data pattern to all addresses from minimum to maximum.
- Step 6. Read and verify xFF data pattern at all addresses.
- Step 7. Write x00 data pattern to all addresses from minimum to maximum.
- Step 8. Read and verify x00 data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verification.

Each test performed independently.

Write Protect Functional test: Write data with Software Write Protect set for given array block, read data and confirm no data change.

Sleep Mode Functional test: Measure IZZ (sleep current) with $V_{ZZ} = V_{IL}$ confirm sleep current meets spec.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-09-16

Approved sources of supply for SMD 5962-23213 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962R2321301VXC	65786	CYRS15B102N-GGMB
5962R2321302VXC	65786	CYRS15B101N-GGMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.