

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update lead finish paragraph to clarify prohibition of pure tin, update format	16 August 2007	Thomas M. Hess

Devices on this drawing may be used as a substitute for MIL-S-19500/493 which has been inactivated for new design.

Prepared in accordance with ASME-14.100

Selected item drawing

REV																							
PAGE																							
REV STATUS OF PAGES	REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
	PAGES		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16					
PMIC N/A			PREPARED BY Roger Kissel						DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OH http://www.dscc.dla.mil/programs/milspec/docsearch.asp														
Original date of drawing 5 December 2001			CHECKED BY Alan Barone						TITLE SEMICONDUCTOR DEVICE, PNP, THYRISTOR, SILICON, (PROGRAMMABLE UNIJUNCTION TRANSISTOR), TYPES 2N6116, 2N6117, 2N6118, 2N6137, 2N6138														
			APPROVED BY Thomas M. Hess																				
			SIZE A	CODE IDENT. NO. 037Z3					DWG NO. 01039														
			REV A						PAGE 1 OF 16														

1. SCOPE

1.1 Scope. This drawing describes the detail requirements for PNP, thyristor silicon, programmable unijunction transistors. Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as follows:

<u>01039</u>	-	<u>2N6116</u>	<u>NON-TX, TX, TXV</u>
Drawing number		Device type	Quality Level

1.2.1 Device types. The device type shall identify the polarity and voltage of the devices as follows:

<u>Device type</u>	<u>Figure number</u>
01039 - 2N6116, TX, TXV	1
01039 - 2N6117, TX, TXV	1
01039 - 2N6118, TX, TXV	1
01039 - 2N6137, TX, TXV	1
01039 - 2N6138, TX, TXV	1

1.2.2 Physical dimensions. See figure 1 (TO-18). The graphic symbol for the programmable unijunction transistor shall be as shown on figure 2.

1.3 Maximum ratings.

Device Types	P_T $T_A = 25^\circ\text{C}$ (1)	I_T	I_{TSM} Peak (2)	V_{GKS} (3)	V_{GKR}	V_{GAR}	V_{AKR}	V_{AKF}	T_{STG}	T_{OP}
	<u>W</u>	<u>mA (rms)</u>	<u>A dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>°C</u>	<u>°C</u>
2N6116	.300	300	5	40	5	40	40	40	-65	-55
2N6117	.300	300	5	40	5	40	40	40	to	to
2N6118	.300	300	5	40	5	40	40	40	+150	+125
2N6137	.300	300	5	40	5	40	40	40		
2N6138	.300	300	5	100	5	100	100	100		

(1) Derate linearly 2.5 mW/°C for T_A above +25° C.

(2) 10 μs , square wave, 1 percent duty cycle.

(3) Anode shorted to gate.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 2

1.4 Primary electrical characteristics.

Device Types	I _p V _S = 10 V dc		I _y V _S = 10 V dc			V _F V _S = 10 V dc I _F = 50 mA dc	V _O	I _{GAO}	
	R _G 10 kΩ	R _G 1 MΩ	R _G 200Ω	R _G 10 kΩ	R _G 1 MΩ			V _{GAO} = 40 V dc	V _{GAO} = 100 V dc
	Max μA dc	Max μA dc	Min mA dc	Min μA dc	Max μA dc	Min V dc	Min V (pk)	Max nA dc	Max nA dc
2N6116	5.0	2.0		70	50	1.5	6.0	5	
2N6117	2.0	0.3		50	50	1.5	6.0	5	
2N6118	1.0	0.15		50	25	1.5	6.0	5	
2N6137	5.0	2.0	1.5	70	50	1.0	9.0	10	
2N6138	5.0	2.0	1.5	70	50	1.0	9.0		10

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Interface and physical dimensions. Interface and physical dimensions shall be as specified on figure 1.

3.2 Marking. Marking of the (part name) is not required; however, each unit package shall be marked in accordance with MIL-STD-1285 and include the PIN as specified herein (see 1.2), the manufacturer's name or Commercial and Government Entity (CAGE) code, and date lot codes.

3.3 Lead material and finish. Lead material shall be Kovar or Alloy 52; a copper core is permitted. Lead finish shall be gold, solder, or tin-lead in accordance with MIL-PRF-19500. Where a choice of lead material or finish is desired, it shall be specified in the contract or purchase order. Tin content of components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass.

3.4 Manufacturer eligibility. To be eligible to supply devices to this drawing, the manufacturer shall perform conformance inspection in accordance with procuring activity's requested first article testing requirements in accordance with 4.4 herein. Devices specified herein shall meet traceability and lot formation requirements of MIL-PRF-19500 except as modified by the procuring activity.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 3

3.5 Certificate of compliance. A certificate of compliance shall be required from manufacturers for listing as an approved source of supply in 6.6 herein. The certificate of compliance submitted to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, prior to listing as a source of supply in 6.6, shall state that the manufacturer's product meets all the requirements of MIL-PRF-19500, and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance shall be provided with each lot of devices delivered in accordance with this drawing.

3.7 Quality levels. Three quality levels are NON-TX, TX and TXV.

- a. NON -TX devices are subjected to groups A and B herein.
- b. TX devices are subjected to the screening and burn-in requirements as specified in 4.3, and groups A and B herein.
- c. TXV devices are subjected to the internal visual 100 percent inspection in accordance with Method 2072 of MIL-STD-750 and table E-IV of MIL-PRF-19500, and then the screening and burn-in requirements as specified in 4.3 and groups A and B herein.

3.8 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.9 Workmanship. The semiconductor shall be uniform in quality and free from any defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Sampling and inspection. Unless otherwise specified, sampling and inspection procedures shall be performed in accordance with MIL-PRF-19500, and as specified herein.

4.2 Conformance Inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.3 Screening. Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	TX and TXV levels
9	Not applicable
10	Not applicable
11	I _{GAO} , I _{P2} and I _{V2}
12	See 4.3.1
13	Δ I _{GAO} = 50% of initial value or 5 nA dc, whichever is greater. Δ I _{P2} = ± 100% of initial value or 25% of maximum I _{P2} , whichever is greater. Δ I _{V2} = ±25% of the initial reading.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_A = +125°C; I_A = 0; see figure 3; 2N6116, 2N6117, 2N6118, 2N6137 = V_{GK} = 40 V dc, 2N6138 = V_{GK} = 100 V dc. Note: No heatsink or forced air cooling on the device shall be permitted.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 4

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIb of MIL-PRF-19500, and table II herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables.

4.5.1 Forward on-state voltage. The test circuit on figure 4 may be used to measure this parameter. The specified values (see table I) of V_S , R_G , and anode current are applied. The anode to cathode voltage is measured as the on-state forward voltage.

4.5.2 Peak point anode current. This parameter shall be measured in the circuit of figure 5 or a suitable equivalent. The variable supply is adjusted to a point just prior to oscillation as detected by the absence of an output voltage pulse. Peak point anode current is the maximum value is I_A just prior to oscillation.

4.5.3 Peak point offset voltage. This parameter shall be measured in the circuit of figure 6. The peak point offset voltage is equal to the peak point anode voltage minus the gate source voltage (V_S), immediately prior to triggering.

4.5.4 Valley point anode current. For the specified gate supply voltage (V_S) (see table I) and gate source resistance (R_G), the anode current corresponding to the valley point operating condition is measured. The test circuit on figure 4 or suitable equivalent, shall be used for this measurement. The specified gate supply voltage (V_S) and gate source resistance (R_G) shall be applied. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{AK} . The I_A corresponding to this minimum value of V_{AK} is the I_V of the device under test.

4.5.5 Gate anode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750 except that the words and symbols, collector (C), base (B), and emitter (E) shall be replaced with gate (G), anode, and cathode, respectively.

4.5.6 Gate cathode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750, except that the words and symbols, collector (C), base (B) and emitter (E) shall be replaced with gate (G), anode, and cathode respectively.

4.5.7 Cathode peak pulse voltage. This test shall be conducted in the circuit of figure 8. The peak pulse voltage (V_O) is observed by an oscilloscope across the 20 Ω resistor. The rise time of the pulse is defined as the time for the waveform to rise from 0.6 V to 6 V.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 5

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Gate anode blocking current	3036	Bias condition D, (see 4.5.5)	I _{GAO}			
2N6116, 2N6117, 2N6118		V _{GAO} = 40 V dc			5	nA dc
2N6137		V _{GAO} = 40 V dc			10	nA dc
2N6138		V _{AOS} = 100 V dc			10	nA dc
Gate cathode blocking current	3036	Bias condition C, (see 4.5.6)	I _{GKS}			
2N6116, 2N6117, 2N6118		V _{GKS} = 40 V dc			50	nA dc
2N6137		V _{GKS} = 40 V dc			100	nA dc
2N6138		V _{GKS} = 100 V dc			100	nA dc
Peak point anode current		V _S = 10 V dc, R _G = 1 MΩ See figure 5, (see 4.5.2)	I _{P1}			
2N6116, 2N6137, 2N6138					2.0	μA dc
2N6117					0.3	μA dc
2N6118					0.15	μA dc
Peak point anode current		V _S = 10 V dc, R _G = 10 kΩ See figure 5, (see 4.5.2)	I _{P2}			
2N6116, 2N6137, 2N6138					5	μA dc
2N6117					2	μA dc
2N6118					1	μA dc
Peak point offset voltage		V _S = 10 V dc, R _G = 1 MΩ See figure 6, (see 4.5.3)	V _{T1}			
2N6116				0.2	1.6	V dc
2N6117, 2N6118, 2N6137, 2N6138				0.2	0.6	V dc
Peak point offset voltage		V _S = 10 V dc, R _G = 10 kΩ See figure 6, (see 4.5.3)	V _{T2}	0.2	0.6	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - continued						
Valley point anode current		$V_S = 10 \text{ V dc}$, $R_G = 1 \text{ M}\Omega$, See figure 4, (see 4.5.4)	I_{V1}		50	$\mu\text{A dc}$
2N6116, 2N6117, 2N6137, 2N6138						
2N6118					25	$\mu\text{A dc}$
Valley point anode current		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ k}\Omega$ See figure 4, (see 4.5.4)	I_{V2}			
2N6116, 2N6137, 2N6138				70		$\mu\text{A dc}$
2N6117, 2N6118				50		$\mu\text{A dc}$
Valley point anode current		$V_S = 10 \text{ V dc}$, $R_G = 200 \text{ }\Omega$ See figure 4, (see 4.5.4)	I_{V3}			
2N6137, 2N6138 (only)				1.5		mA dc
Forward on-state voltage		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ k}\Omega$ $I_F = 50 \text{ mA dc}$, See figure 4 (see 4.5.1)	V_F			
2N6116, 2N6117, 2N6118					1.5	V dc
2N6137, 2N6138					1.0	V dc
<u>Subgroup 3</u>						
Low temperature operation		$T_A = -55^\circ\text{C}$				
Peak point anode current		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ k}\Omega$ See figure 5, (see 4.5.2)	I_{P3}	0.001	10	$\mu\text{A dc}$
High temperature operation		$T_A = +125^\circ\text{C}$				
Gate anode blocking current	3036	Bias condition D, (see 4.5.5)	I_{GAO2}			
2N6116, 2N6117, 2N6118, 2N6137		$V_{GAO} = 40 \text{ V dc}$			0.5	$\mu\text{A dc}$
2N6138		$V_{GAO} = 100 \text{ V dc}$			0.5	$\mu\text{A dc}$

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - continued						
Valley point anode current		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ k}\Omega$ See figure 4, (see 4.5.4)	I_{V2}			
2N6116, 2N6137, 2N6138					40	$\mu\text{A dc}$
2N6117, 2N6118					10	$\mu\text{A dc}$
<u>Subgroup 4</u>						
Peak pulse voltage		See figure 8, (see 4.5.7)	V_O			
2N6116, 2N6117, 2N6118				6.0		V dc
2N6137, 2N6138				9.0		V dc
Peak pulse voltage rise time		See figure 8, (see 4.5.7)	t_r		80	ns
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO

SIZE
A

CODE IDENT NO.
037Z3

DWG NO.
01039

REV A

PAGE 8

TABLE II. Group B inspection.

Inspection 1/ <u>Subgroup 1</u> 2/	MIL-STD-750	
	Method	Conditions
Solderability	2026	
Resistance to solvents	1022	
<u>Subgroup 2</u>		
Thermal shock (temperature cycling)	1051	
Hermetic seal Fine leak Gross leak	1071	
Electrical measurements		See table III steps 1, 3, and 5
<u>Subgroup 3</u>		
Steady-state operation	1027	$T_A = +125^{\circ}\text{C}$; $I_A = 0$; see figure 10
2N6116, 2N6117, 2N6118, 2N6137		$V_{GK} = 40 \text{ V dc}$
2N6138		$V_{GK} = 100 \text{ V dc}$, no heatsink or forced air cooling on the device shall be permitted
Electrical measurements		See table III steps 2, 4, and 6
<u>Subgroup 4</u>		
Decap internal visual (design verification)	2075	
Bond strength	2037	Test condition A; all internal leads for each device shall be pulled separately
<u>Subgroup 5</u>		
Not applicable		
<u>Subgroup 6</u>		
High-temperature life (nonoperating)	1032	$T_{STG} = +150^{\circ}\text{C}$
Electrical measurements		See table III steps 2, 4, and 6
<u>Subgroup 7</u>		
Not applicable		

1/ For sample plan, see MIL-PRF-19500.

2/ Separate samples may be used for each test.

DEFENSE SUPPLY CENTER, COLUMBUS
COLUMBUS, OHIO

SIZE
A

CODE IDENT NO.
037Z3

DWG NO.
01039

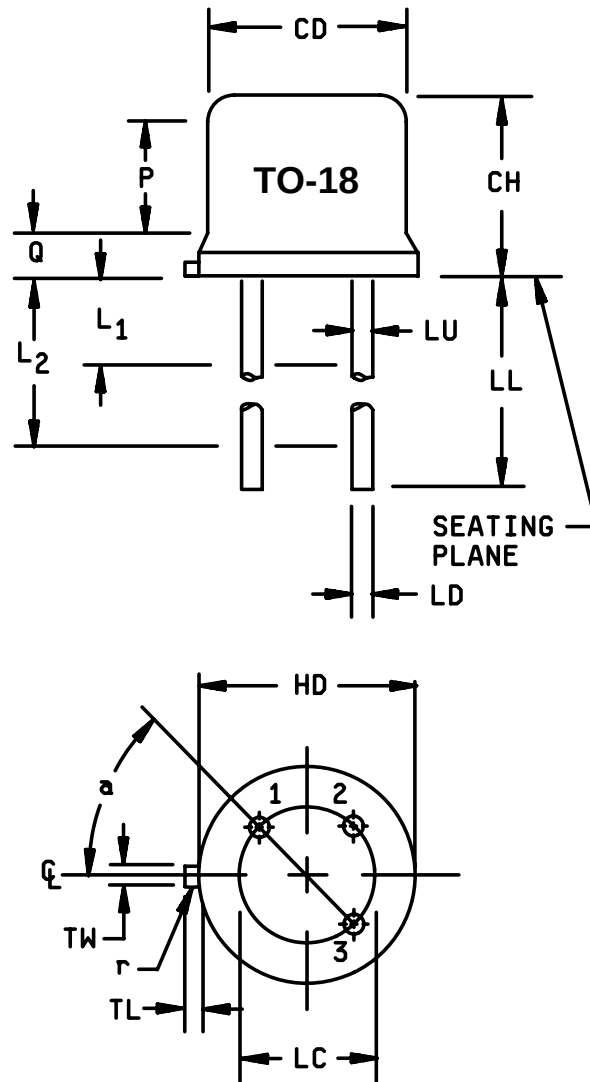
REV A

PAGE 9

TABLE III. Groups A and B electrical measurements.

Step	Inspection	MIL-STD- 750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Gate, anode blocking current 2N6116, 2N6117, 2N6118 2N6137 2N6138	3036	Bias condition D (see 4.5.5) $V_{GAO} = 40 \text{ V dc}$ $V_{GAO} = 40 \text{ V dc}$ $V_{GAO} = 100 \text{ V dc}$	I_{GAO}		5 10 10	nA dc
2.	Gate, anode blocking current 2N6116, 2N6137, 2N6138 2N6117 2N6118	3036	Bias condition D (see 4.5.5) $V_{GAO} = 40 \text{ V dc}$ $V_{GAO} = 40 \text{ V dc}$ $V_{GAO} = 100 \text{ V dc}$	I_{GAO}		1 1 1	$\mu\text{A dc}$ $\mu\text{A dc}$ $\mu\text{A dc}$
3.	Peak point anode current 2N6116, 2N6137, 2N6138 2N6117 2N6118		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ K}\Omega$ See figure 5, (see 4.5.2)	I_p		5.0 2.0 1.0	$\mu\text{A dc}$ $\mu\text{A dc}$ $\mu\text{A dc}$
4.	Peak point anode current 2N6116, 2N6137, 2N6138 2N6117 2N6118		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ K}\Omega$ See figure 5, (see 4.5.2)	I_p	.001	6.0 3.0 2.0	$\mu\text{A dc}$ $\mu\text{A dc}$ $\mu\text{A dc}$
5.	Valley point anode current 2N6116, 2N6137, 2N6138 2N6117, 2N6118		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ K}\Omega$ See figure 4, (see 4.5.4)	I_v		70 50	$\mu\text{A dc}$ $\mu\text{A dc}$
6.	Valley point anode current 2N6116, 2N6137, 2N6138 2N6117, 2N6118		$V_S = 10 \text{ V dc}$, $R_G = 10 \text{ K}\Omega$ See figure 4, (see 4.5.4)	I_v		55 35	$\mu\text{A dc}$ $\mu\text{A dc}$

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	6,7
LL	.500	.750	12.70	19.05	6,7
LU	.016	.019	0.41	0.48	6,7
L ₁		.050		1.27	6,7
L ₂	.250		6.35		6,7
P	.100		2.54		
Q		.030		0.76	4
TL	.028	.048	0.71	1.22	3
TW	.036	.046	0.91	1.17	3
r		.010		0.25	9
α	45° TP		45° TP		5



NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Dimension TL measured from maximum HD.
4. Body contour optional within zone defined by HD, CD, and Q.
5. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
6. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
7. All three leads.
8. Dimension r (radius) applies to both inside corners of tab.
9. In accordance with ANSI Y14.5M, diameters are equivalent to Φx symbology.
10. Lead 1 = cathode, lead 2 = gate, lead 3 = anode (internally connected to the case).

FIGURE 1. Physical dimensions TO-206AA (formerly TO-18).

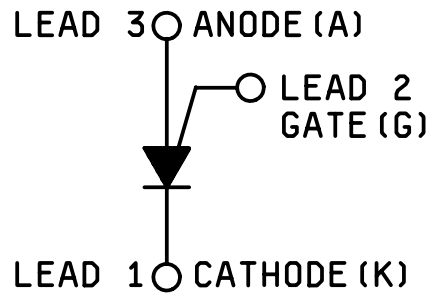
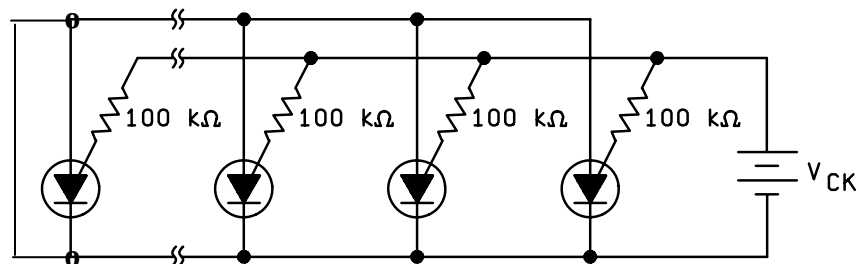
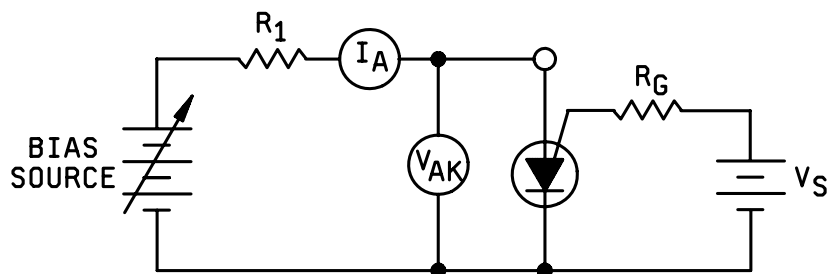


FIGURE 2. Symbol for programmable unijunction transistor.



NOTE: Any number of devices under test may be added in parallel up to the maximum capability of the power supply to maintain voltage under the theoretical worst case condition if all devices under test shorted.

FIGURE 3. Burn-in and operating life test circuit.



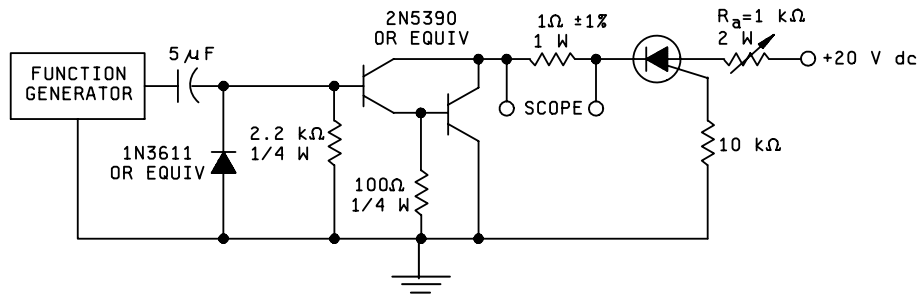
NOTES:

1. R1 chosen to limit current to a safe value.
2. Bias source is a well regulated 1 mV peak to peak ripple supply.

FIGURE 4. Valley point anode current and forward on-state voltage circuit.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 12

NOTES:



NOTE: Adjust function generator to pulse width = 10 μ s (square wave) and repetition rate = 1 kHz.
Adjust R_a for 5 V peak (equivalent to 5 A peak). Total test time = 1 minute minimum.

FIGURE 7. Peak anode current test circuit.

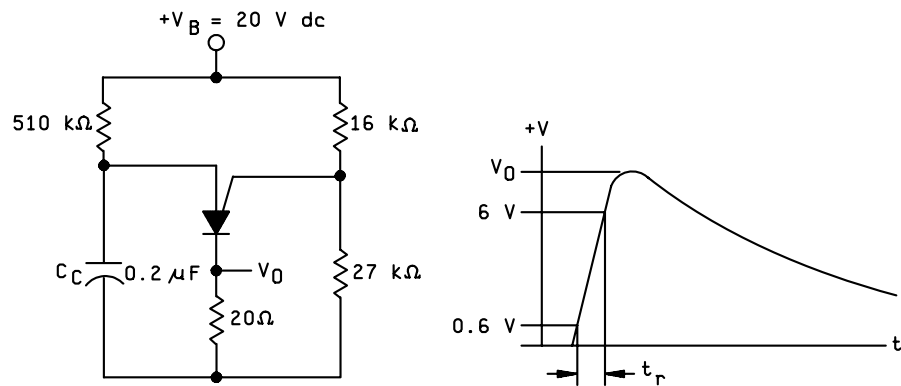


FIGURE 8. V_O and t_r test circuit.

5 PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Devices conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of duplicate specifications, drawings, and stock number listings.

6.2 Acquisition requirements. The acquisition requirements should specify the following:

- a. Complete PIN (see 1.2).
- b. Requirements for delivery of one copy of the conformance inspection data or certificate of compliance that parts have passed conformance inspection with each shipment of parts by the manufacturer.
- c. Requirements for packaging and packing.

6.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

I_F	On-state current, RMS, from anode through cathode.
I_{GAO}	Gate anode blocking current (dc), anode shorted to gate.
I_{GKS}	Gate to cathode blocking current (dc), anode shorted to gate.
I_P	Peak point anode current. This is the minimum value of anode current for which the slope of the static anode characteristic curve is zero for a specified value of V_S and R_G .
I_T	Maximum dc forward anode current.
I_{TSM}	Nonrepetitive peak forward current.
I_V	Valley point anode current. This is the maximum value of anode current for which the slope of the static anode characteristic curve is zero for a specified value of V_S and R_G .
R_G	Equivalent gate resistance.
V_{AKF}	Anode to cathode forward voltage.
V_{AKR}	Anode to cathode reverse voltage.
V_F	On-state voltage. The resultant dc voltage measured between the anode and cathode for specified values of on-state anode current (I_F).
V_{GA}	Voltage (dc) from gate to anode.
V_{GK}	Gate to cathode voltage, (dc) voltage from gate to cathode.
V_{GAR}	Gate to anode reverse voltage.
V_{GKR}	Gate to cathode reverse voltage.
V_P	Peak point anode voltage. The voltage from anode to cathode when the peak point anode current flows for a specified value of V_S and R_G .
V_S	Gate source voltage.
V_O	Cathode peak pulse voltage. This parameter is a relative indicator of the peak anode current available for use in firing circuits.
V_T	Offset voltage, at the peak point current (I_P). The difference between the anode peak point voltage (V_P) and the gate source voltage (V_S).

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 15

6.4 Replaceability. Devices covered by this drawing may be used as a substitute for MIL-S-19500/493.

DSCC drawing PIN (1)	Military part number
01039-2N6116	JAN2N6116
01039-2N6116TX	JANTX2N6116
01039-2N6116TXV	JANTXV2N6116
01039-2N6117	JAN2N6117
01039-2N6117TX	JANTX2N6117
01039-2N6117TXV	JANTXV2N6117
01039-2N6118	JAN2N6118
01039-2N6118TX	JANTX2N6118
01039-2N6118TXV	JANTXV2N6118
01039-2N6137	JAN2N6137
01039-2N6137TX	JANTX2N6137
01039-2N6137TXV	JANTXV2N6137
01039-2N6138	JAN2N6138
01039-2N6138TX	JANTX2N6138
01039-2N6138TXV	JANTXV2N6138

(1) Parts must be purchased to this DSCC Drawing PIN to assure that all performance requirements are met and tests performed.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed with this drawing and have submitted a certificate of compliance (see 3.4 herein) to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990 or emailed to semiconductor@dsc.dla.mil.

DSCC drawing PIN (1)	Vendor similar designation or type number	Vendor CAGE	Vendor name and address
01039-2N6116	2N6116	43611	Microsemi-NES 6 Lake Street Lawrence, MA 01841-3011
01039-2N6116TX	2N6116TX		
01039-2N6116TXV	2N6116TXV		
01039-2N6117	2N6117		
01039-2N6117TX	2N6117TX		
01039-2N6117TXV	2N6117TXV		
01039-2N6118	2N6118		
01039-2N6118TX	2N6118TX		
01039-2N6118TXV	2N6118TXV		
01039-2N6137	2N6137		
01039-2N6137TX	2N6137TX		
01039-2N6137TXV	2N6137TXV		
01039-2N6138	2N6138		
01039-2N6138TX	2N6138TX		
01039-2N6138TXV	2N6138TXV		

(1) Parts must be purchased to this DSCC PIN to assure that all performance requirements and tests are met.

6.6 Comments. Comments on this drawing should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dsc.dla.mil.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 037Z3	DWG NO. 01039
		REV A	PAGE 16