



DEFENSE LOGISTICS AGENCY
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June 16, 2026

MEMORANDUM FOR MILITARY/INDUSTRY DISTRIBUTION

SUBJECT: Initial Drafts of:

MIL-PRF-STACK (Capacitor, Fixed, Ceramic Dielectric (General Purpose and Temperature Stable), Stacked, Standard Reliability and High Reliability, General Specification for)

MIL-PRF-STACK/1 (Capacitor, Fixed, Ceramic Dielectric (General Purpose and Temperature Stable), Horizontally Stacked, Standard Reliability and High Reliability, Size 2220)

Project numbers: 5910-2026-038 and -039.

The subject documents are now available for viewing and downloading from the DLA Weapons Support (Columbus) - VA website:

<https://landandmaritimeapps.dla.mil/Programs/MilSpec/initialdrafts.aspx>

This new military specification and associated specification sheet are being developed to specify the requirements and quality assurance provisions for stacked capacitor assemblies utilizing extended range ceramic capacitors like those in [MIL-PRF-32535](#). Three product levels are offered: M (standard reliability), T (high reliability), and U (high reliability). MIL-PRF-STACK capacitors have higher capacitance values than [MIL-PRF-49470](#) capacitors of the same size and voltage rating.

The high reliability capacitors (T and U level) are intended for space, missile, and other high reliability applications. Requirements and quality assurance provisions for T and U level capacitors include ultrasonic inspection, destructive physical analysis, and an enhanced production lot definition. U level capacitors also require an additional post-termination ultrasonic inspection. Inspection of product for delivery for T and U level capacitors consists of group A and subgroups 1 and 2 of group B.

Concurrence or comments are required at this Center no later than **20 July 2026**. If comments are not received during the allotted coordination period, concurrence may be assumed. Late comments may be held for the next specification action. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply. Since Navy – EC is a custodian for this document; all Navy review activities should forward their comments directly to this Center.

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//Signature on file//

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PERFORMANCE SPECIFICATION

CAPACITOR, FIXED, CERAMIC DIELECTRIC (GENERAL PURPOSE AND TEMPERATURE STABLE), STACKED, STANDARD RELIABILITY AND HIGH RELIABILITY, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for general purpose and temperature stable, stacked ceramic capacitors. Three product levels are offered: M (standard reliability), T (high reliability), and U (high reliability). MIL-PRF-STACK capacitors have higher capacitance values than [MIL-PRF-49470](#) capacitors of the same size and voltage rating.

The high reliability capacitors (T and U level) are intended for space, missile, and other high reliability applications. Requirements and quality assurance provisions for T and U level capacitors include ultrasonic inspection, destructive physical analysis, and an enhanced production lot definition. U level capacitors also require an additional post-termination ultrasonic inspection. Inspection of product for delivery for T and U level capacitors consists of group A and subgroups 1 and 2 of group B.

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). Capacitors specified herein (see [3.1](#)); are identified by a PIN which consists of the product level designator, basic number of the performance specification, and a series of coded characters. The coded characters provide information concerning the characteristic, specification sheet number, capacitance, capacitance tolerance, voltage, and where applicable, lead configuration. The PIN is in the following form:

MSTACK	01	E2	B	103	K	J	M	B 1/
Performance specification number	Slash sheet number	Characteristic (see 1.2.1.1)	Voltage (see 1.2.1.2)	Capacitance (see 1.2.1.3)	Capacitance tolerance (see 1.2.1.4)	Configuration (see 1.2.1.5)	Product level (see 1.2.1.6)	Electrode (see 1.2.1.7)

1/ When a specific electrode material is not required, the electrode designator is left blank (see [1.2.1.7](#)).

1.2.1.1 Characteristic. The characteristic refers to the temperature characteristic (TC) of the capacitor as shown in [table I](#). The class and three-character characteristics (C0G and X7R) are as defined in [EIA-198-1](#).

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support (Columbus), ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990, or emailed to capacitorfilter@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.



MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE I. Temperature characteristic.

Symbol	Characteristic	Class	Capacitance change w/ reference to +25°C
E1 <u>1/</u>	C0G	I	0 ± 30 ppm/°C
E2	X7R	II	± 15 percent

1/ At the +25°C stability point, the capacitance measurement may be ± .2 percent or ± 0.05 pF, whichever is greater, from the +25°C reference.

1.2.1.2 Rated voltage. The rated voltage for continuous operation at +125°C is identified by a single letter as shown in [table II](#).

TABLE II. Rated voltage.

Symbol	Rated voltage
X	10
Y	16
Z	25
A	50
B	100
C	200
E	500

1.2.1.3 Capacitance. The nominal capacitance value, expressed in picofarads (pF) is identified by a three digit number; the first two digits represent significant figures and the last digit specifies the number of zeros to follow.

1.2.1.4 Capacitance tolerance. The capacitance tolerance is identified by a single letter as shown in [table III](#).

TABLE III. Capacitance tolerance.

Symbol	Capacitance tolerance
J	± 5 percent
K	± 10 percent
M	± 20 percent

1.2.1.5 Configuration. The configuration is identified by single letter as shown in [table IV](#) (see 3.1).

TABLE IV. Configuration.

Symbol	Lead style	Lead frame material
J	Formed inward (feet)	Unspecified
L	Formed outward (feet)	Unspecified
G	Formed inward (paddle)	Unspecified
H	Formed outward (paddle)	Unspecified
K	Formed inward (feet)	Nickel-iron class <u>1/</u>
M	Formed outward (feet)	Nickel-iron class <u>1/</u>
C	Formed inward (paddle)	Nickel-iron class <u>1/</u>
B	Formed outward (paddle)	Nickel-iron class <u>1/</u>
F	Formed inward (feet)	Phosphor-bronze class <u>2/</u>
D	Formed outward (feet)	Phosphor-bronze class <u>2/</u>
P	Formed inward (paddle)	Phosphor-bronze class <u>2/</u>
R	Formed outward (paddle)	Phosphor-bronze class <u>2/</u>

1/ Referenced in [MIL-STD-1276](#).

2/ Referenced in [ASTM B139/B139M](#).

MIL-PRF-STACK
DRAFT DATED 16 June 2026

1.2.1.6 Product level. The product level is identified by a single letter as shown in [table V](#).

TABLE V. Product level.

Symbol	Product level
M	Standard reliability
T	High reliability
U	High reliability

1.2.1.7 Electrode. The electrode material is identified by a single letter or left blank as shown in [table VI](#).

TABLE VI. Electrode material.

Symbol	Electrode material
P	Precious metal electrode (PME), palladium/silver
B	Base metal electrode (BME), nickel
Blank ^{1/}	Either PME or BME is acceptable.

^{1/} For ordering purposes only. Package marking will include the electrode material symbol (see [3.25](#)).

2. APPLICABLE PUBLICATIONS

2.1 General. The publications listed in this section are specified in sections 3 and 4 of this specification. This section does not include publications cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, users of this document are cautioned that they must meet all specified requirements of publications cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government publications.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these publications are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-STACK/1 - Capacitor, Fixed, Ceramic Dielectric (General Purpose and Temperature Stable), Stacked, Standard Reliability and High Reliability, Horizontally Stacked, Size 2220

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Test Methods Standard Electronic and Electrical Component Parts
MIL-STD-202-107 - Method 107, Thermal Shock
MIL-STD-202-108 - Method 108, Life (at Elevated Ambient Temperature)
MIL-STD-202-204 - Method 204, Vibration, High Frequency
MIL-STD-202-208 - Method 208, Solderability
MIL-STD-202-210 - Method 210, Resistance to Soldering Heat
MIL-STD-202-213 - Method 213, Shock (Specified Pulse)
MIL-STD-202-215 - Method 215, Resistance to Solvents
MIL-STD-202-220 - Method 220, Ultrasonic Inspection
MIL-STD-202-301 - Method 301, Dielectric Withstanding Voltage
MIL-STD-202-302 - Method 302, Insulation Resistance
MIL-STD-202-305 - Method 305, Capacitance

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- MIL-STD-790 - Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications
- MIL-STD-1276 - Leads for Electronic Component Parts

(Copies of these publications are available online at <https://quicksearch.dla.mil/>)

2.3 Non-Government publications. The following publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the publications are those cited in the solicitation or contract.

ELECTRONIC COMPONENTS INDUSTRY ASSOCIATION (ECIA)

- ECIA EIA-469 - Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

(Copies of this publication are available online at <http://www.ecianow.org>.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Capacitors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award (see 4.4 and 6.3).

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for capacitors covered by this specification. This QPL system shall be established and maintained in accordance with the procedures and requirements specified in MIL-STD-790 and herein.

3.4 Materials. Materials shall be as specified herein. However, when a definite material is not specified, a material shall be used which will enable the capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guarantee of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. Capacitors shall meet the interface and physical dimensions specified (see 3.1).

3.5.1 Lead attachment. When solder is used to attach the lead frame to the chip capacitor, the solder used shall have a liquidus temperature of +260°C or greater.

3.5.2 Terminal lead finish. The terminal lead finish shall be in accordance with code 32 or code 52 of MIL-STD-1276 (NOTE: The 200 microinch maximum dimension for code 52 is not applicable).

3.5.2.1 Pure tin. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of capacitor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.5).

3.6 Ultrasonic inspection (T and U levels only). When examined in accordance with 4.7.1, capacitors that exhibit unacceptable responses as specified in ECIA EIA 469 shall be rejected, except in the case of false responses as defined in MIL-STD-202-220. If false responses are suspected, the manufacturer may individually examine the capacitor and accept it if the false response is confirmed.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

3.7 Chip level DPA (T and U levels only). When examined as specified in [4.7.2](#), chip capacitors shall meet the requirements of [ECIA EIA 469](#) with the following exceptions:

a. Defect criteria for delaminations (see [6.4.2](#)):

- (1) Any single delamination of an interface of material layers which exceeds 20% of the interface (pertaining to the overall chip element length or width) and exceeds 0.005 inch (0.127 mm).
- (2) Any single delamination of an interface of material layers in the active area which exceeds 0.005 inch (0.127 mm) and displaces adjacent dielectric layers by more than 50% of the average dielectric thickness for the affected layer(s).

b. Defect criteria for margin defects:

- (1) Side margins: Any side margin that displays a minimum margin less than the values shown in [table VII](#).

TABLE VII. Side margins.

Rated voltage (V _{dc})	Minimum side margin (in (mm))
10 through 16	.0008 (0.020)
25	.0010 (0.025)
> 25 through 50	.0016 (0.040)
> 50 through 500	.0020 (0.050)

- (2) End margins: Any end margin with a minimum less than the values shown in [table VIII](#).

TABLE VIII. End margins.

Rated voltage (V _{dc})	Minimum end margin (in (mm))
10 through 16	.0014 (0.036)
25	.0016 (0.040)
> 25 through 50	.0020 (0.050)
> 50 through 500	.0030 (0.075)

- (3) Cover plate thickness: Any cover plate with a minimum thickness less than the values shown in [table IX](#).

TABLE IX. Cover plate thickness.

Rated voltage (V _{dc})	Minimum cover plate thickness (in (mm))
10 through 16	.0014 (0.036)
25	.0016 (0.040)
> 25 through 50	.0020 (0.050)
> 50 through 500	.0030 (0.075)

MIL-PRF-STACK
DRAFT DATED 16 June 2026

c. Defect criteria for cracks (see 6.4.1) in the ceramic: Any crack in the dielectric of the active area or any crack in the enveloping ceramic margins/borders that either reduces, or has the potential through further propagation, to reduce the effective margins to a point less than the limits defined by 3.7b.

d. Defect criteria for dielectric and electrode nonuniformities:

- (1) Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness (T) by more than 50 percent (see figure 1).

For capacitors with dielectric thicknesses less than or equal to 7 microns, apparent voids that reduce the total dielectric thickness (T) by more than 50 percent (see figure 1) may be further evaluated using a scanning electron microscope (SEM), or equivalent, to determine if the anomalies are true manufacturing voids or DPA process induced artifacts. This evaluation method shall be approved by the qualifying activity.

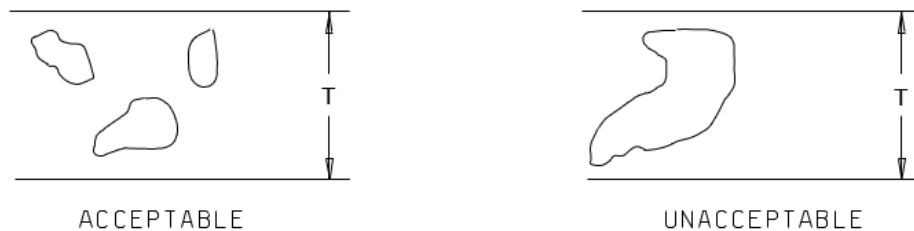


FIGURE 1. Dielectric parameters.

- (2) Undulations in the electrode and dielectric layers shall not be cause for rejection as long as both electrodes and dielectrics follow the same undulating pattern (see figure 2) without distorting the dielectric and the requirements of 3.7b are met.



FIGURE 2. Undulating electrode and dielectric layers.

3.8 Visual examination.

3.8.1 Visual examination (ceramic body defects). When capacitors are examined in accordance with 4.7.3.1, no device shall be acceptable that exhibits the following ceramic body defects:

- Cracks or pre-chip-outs.
- Exposed electrodes.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- c. Delaminations.
- d. Electrodes visible in chip-outs.
- e. Chip-outs longer than 30 percent of each axis or longer than .100 inch (2.54 mm), whichever is less.
- f. Lifted terminations.

3.8.2 Visual examination (lead attachment defects). When capacitors are inspected as specified in 4.7.3.2, no device shall be acceptable that exhibits the following lead attachment defects:

- a. Exposed electrodes.
- b. Solder balls or conductive epoxy particles.
- c. Exposed base metal on the lead frame that exceeds 5 percent of the total solderable area. NOTE: The surface of the lead may exhibit bare base metal on the edges and cut ends of the pins but not on the flat portion of the leads. These capacitor leads are not expected to be solderable above the lead bend.
- d. Leads shall not exhibit cuts, nicks, or scrapes exceeding 10 percent of the length of the leads.
- e. Less than or equal to 80 percent solder attachment.
- f. Fractured solder.
- g. Bent, twisted or fractured leads.
- h. Residual flux.

3.9 Thermal shock and voltage conditioning. When tested as specified in 4.7.4, capacitors shall withstand the extremes of high and low temperature without visible damage and meet the following requirements:

- a. Insulation resistance (at +125°C): Shall not be less than the initial requirement (see 3.10).
- b. Dielectric withstanding voltage (at +25°C): In accordance with 3.11.
- c. Insulation resistance (at +25°C): Shall not be less than the initial requirement (see 3.10).
- d. Capacitance (at +25°C): Shall be within the tolerance specified (see 3.1).
- e. Dissipation factor (at +25°C): In accordance with 3.13.

3.10 Insulation resistance. When measured as specified in 4.7.5, the insulation resistance shall not be less than the following:

- a. At +25°C: 100,000 megohms or 500 megohm-microfarads, whichever is less.
- b. At +125°C: 10,000 megohms or 25 megohm-microfarads, whichever is less.

3.11 Dielectric withstanding voltage. When tested as specified in 4.7.6, there shall be no evidence of damage or breakdown.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

3.12 Capacitance. When measured as specified in 4.7.7, the capacitance shall be within the specified tolerance (see 3.1).

3.13 Dissipation factor. When determined in accordance with 4.7.8, the dissipation factor shall not exceed the values shown in table X.

TABLE X. Dissipation factor limits.

Characteristic	Maximum allowable DF (%)				
	Rated Voltage (V_{dc})				
	10	16	25	50	≥ 100
X7R	5.0	5.0	5.0	3.5	3.0
C0G	0.15	0.15	0.15	0.15	0.15

3.14 DPA (T and U levels only). When inspected as specified in 4.7.9, there shall be no evidence of capacitor cracking.

3.15 Solderability. When capacitors are tested as specified in 4.7.10, the dipped surface of the leads shall be at least 95 percent covered with a new, smooth, solder coating. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. Bare base metal where the solder dip failed to cover the original coating is an indication of poor solderability and shall be cause for failure. In case of dispute, the percent of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

3.16 Life (at +125°C). When tested as specified in 4.7.11, capacitors shall meet the following requirements:

a. 250-hour limits:

- (1) Insulation resistance (at +125°C): Shall not be less than 50 percent of the specified value (see 3.10).
- (2) Visual examination: No mechanical damage. Marking shall remain legible.
- (3) Insulation resistance (at +25°C): Shall not be less than 50 percent of the specified value (see 3.10).
- (4) Capacitance: Change not to exceed ± 15 percent from the initial measured value for class II characteristics, and ± 3 percent from the initial measured value for class I characteristics.
- (5) Dissipation factor: Shall not exceed the specified limit (see 3.13).

b. 1,000-hour, 2,000-hour, and 4,000-hour limits:

- (1) Insulation resistance (at +125°C): Shall not be less than 30 percent of the specified value (see 3.10).
- (2) Visual examination: No mechanical damage. Marking shall remain legible.
- (3) Insulation resistance (at +25°C): Shall not be less than 30 percent of the specified value (see 3.10).
- (4) Capacitance: Change not to exceed ± 20 percent from the initial measured value for class II characteristics, and ± 3 percent from the initial measured value for class I characteristics.
- (5) Dissipation factor:
 - (a) Class II characteristics: Shall not exceed the limits shown in table XI.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE XI. Class II characteristic dissipation factor limits.

Rated Voltage (V _{dc})	Maximum DF (%)
≥ 50V	3.0
16V – 25V	5.0
10V	7.5

(b) Class I characteristics: Shall not be more than 20% greater than the initial specified limit (see 3.13).

3.17 Shock, specified pulse. When tested as specified in 4.7.12, there shall be no momentary or intermittent contact of 0.5 ms or greater duration, open-circuiting or short-circuiting, or other evidence of breakdown, arcing, and mechanical damage.

3.18 Resistance to soldering heat. When tested as specified in 4.7.13, capacitors shall meet the following requirements:

a. Insulation resistance at +25°C: Not less than the initial +25°C requirement (see 3.10).

b. Capacitance.

(1) Class II characteristics: Shall change not more than -5 percent to +15 percent from the initial measured value.

(2) Class I characteristics: Shall change not more than ± 3 percent from the initial measured value.

c. Dissipation factor: Shall not exceed the initial limits (see 3.13).

3.19 Temperature humidity bias. When tested in accordance with 4.7.14, IR shall not be less than 30 percent of the initial +25°C requirement for class I characteristics; not less than 10 percent of the initial +25°C requirement for class II characteristics (see 3.10).

3.20 Temperature characteristic. The capacitance change over the range of temperatures specified in 4.7.15 shall not exceed the limits specified (see table I). The capacitance value obtained in step C of table XXI shall be considered as the reference point.

3.21 Vibration, high frequency. When capacitors are tested as specified in 4.7.16, there shall be no intermittent contacts of 0.5 millisecond (ms) or greater duration, open-circuiting or short-circuiting, or evidence of mechanical damage.

3.22 Terminal strength or peel force. At the option of the manufacturer, either the terminal strength (see 3.22.1) or the peel force (see 3.22.2) test may be performed.

3.22.1 Terminal strength. When capacitors are tested as specified in 4.7.17.1, there shall be no loosening or rupturing of the terminals.

3.22.2 Peel force. When capacitors are tested as specified in 4.7.17.2, the force required to peel the lead frame attachment shall be greater than 2 pounds.

3.23 Dielectric breakdown voltage. When tested in accordance with 4.7.18, the recorded voltage at breakdown shall not be less than 6X rated voltage or 1,200 V_{dc}, whichever is less.

3.24 Resistance to solvents (ink marking only). When capacitors are tested as specified in 4.7.19, there shall be no evidence of mechanical damage and the marking shall remain legible.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

3.25 Package marking. Packaging containers shall be marked with the PIN (see 1.2.1), capacitance, capacitance tolerance, voltage, "JAN" brand, lot symbol, date code, and the CAGE code. The PIN shall include the electrode material code whether or not it was used for acquisition. The date code shall be of the form YYWW representing the 2-digit year and the 2-digit week (e.g., 40th week of 2017 = 1740). Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited.

3.25.1 Capacitor marking. Capacitors shall be legibly marked in a contrasting color in accordance with either of the two options below. The capacitor marking shall include the manufacturer's trademark or symbol. Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. The marking shall withstand the environmental conditions specified herein. The marking shall be a minimum resistance of 1×10^9 ohms per square and shall remain legible after coating the capacitors with 1.5 to 3 mils of transparent conformal coating such as polyurethane, acrylic, or the equivalent.

a. Option A: In accordance with table XII.

b. Option B: In accordance with table XIII using a two character system. The first character shall be an alphabetic symbol and shall designate the first and second significant figures. The second character shall be a numerical digit and shall designate the decimal multiplier of capacitance in pF (e.g., A1 = $1 \times 10^1 = 10$ pF, J5 = $2.2 \times 10^5 = 0.22 \times 10^6$ 0.22 μ F). The marking shall appear in black or legible contrast. The size and orientation of the marking shall be the option of the manufacturer.

Additional marking may appear provided that it does not interfere with the required marking.

TABLE XII. Marking for capacitors.

Character	Significant units	Capacitance (pF) and multiplier							
		Orange (x 0.1)	Black (x 1.0)	Green (x 10)	Blue (x 100)	Violet (x 1000)	Red (x 10,000)	Yellow (x 100,000)	White (x 1,000,000)
A	10	1.0	10	100	1000	10,000	100,000	1,000,000	10,000,000
B	11	1.1	11	110	1100	11,000	110,000	1,100,000	11,000,000
C	12	1.2	12	120	1200	12,000	120,000	1,200,000	12,000,000
D	13	1.3	13	130	1300	13,000	130,000	1,300,000	13,000,000
E	15	1.5	15	150	1500	15,000	150,000	1,500,000	15,000,000
H	16	1.6	16	160	1600	16,000	160,000	1,600,000	16,000,000
I	18	1.8	18	180	1800	18,000	180,000	1,800,000	18,000,000
J	20	2.0	20	200	2000	20,000	200,000	2,000,000	20,000,000
K	22	2.2	22	220	2200	22,000	220,000	2,200,000	22,000,000
L	24	2.4	24	240	2400	24,000	240,000	2,400,000	24,000,000
N	27	2.7	27	270	2700	27,000	270,000	2,700,000	27,000,000
O	30	3.0	30	300	3000	30,000	300,000	3,000,000	30,000,000
R	33	3.3	33	330	3300	33,000	330,000	3,300,000	33,000,000
S	36	3.6	36	360	3600	36,000	360,000	3,600,000	36,000,000
T	39	3.9	39	390	3900	39,000	390,000	3,900,000	39,000,000
V	43	4.3	43	430	4300	43,000	430,000	4,300,000	43,000,000
W	47	4.7	47	470	4700	47,000	470,000	4,700,000	47,000,000
X	51	5.1	51	510	5100	51,000	510,000	5,100,000	51,000,000
Y	56	5.6	56	560	5600	56,000	560,000	5,600,000	56,000,000
Z	62	6.2	62	620	6200	62,000	620,000	6,200,000	62,000,000
3	68	6.8	68	680	6800	68,000	680,000	6,800,000	68,000,000
4	75	7.5	75	750	7500	75,000	750,000	7,500,000	75,000,000
7	82	8.2	82	820	8200	82,000	820,000	8,200,000	82,000,000
9	91	9.1	91	910	9100	91,000	910,000	9,100,000	91,000,000

MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE XIII. Optional marking for capacitors.

First character				Second character	
Alphabetic character	Significant figures	Alphabetic character	Significant figures	Numerical character	Decimal multiplier
A	1.0	T	5.1	0	10 ⁰
B	1.1	U	5.6	1	10 ¹
C	1.2	V	6.2	2	10 ²
D	1.3	W	6.8	3	10 ³
E	1.5	X	7.5	4	10 ⁴
F	1.6	Y	8.2	5	10 ⁵
G	1.8	Z	9.1	6	10 ⁶
H	2.0	a	2.5	7	10 ⁷
J	2.2	b	3.5	8	10 ⁸
K	2.4	d	4.0	9	10 ⁹
L	2.7	e	4.5		
M	3.0	f	5.0		
N	3.3	m	6.0		
P	3.6	n	7.0		
Q	3.9	t	8.0		
R	4.3	y	9.0		
S	4.7				

3.25.2 Substitution of capacitance tolerance and rated voltage. Parts qualified to tighter capacitance tolerance or higher rated voltage are substitutable, with acquiring agency approval, for parts marked to looser capacitance tolerance or lower rated voltage provided all other values, such as case size, characteristic, and leads are the same. Unless specified in the contract or order (see 6.2), the substitutable parts shall not be remarked. In the event that the capacitance tolerances or rated voltages are remarked, the lot symbol and date code on the parts shall not be changed, and the workmanship criteria shall be met.

3.25.3 Product level substitution. Capacitors qualified and marked as T or U level capacitors are substitutable, with acquiring agency approval, for M level capacitors provided all other characteristics specified in the PIN (see 1.2.1) are the same. Unless specified in the contract or order (see 6.2), the substitutable parts shall not be remarked. In the event that the product level is remarked, the lot symbol and date code on the parts shall not be changed, and the workmanship criteria shall be met.

3.25.4 JAN and J marking. The United States Government has adopted and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" and "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein on in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets, the manufacturer shall remove completely the military part number and the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 6,069,576 for the certification mark "JAN" and Registration Number 2,577,735 for the certification mark "J".

3.26 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

3.27 Workmanship. Capacitors shall be processed in such a manner as to be uniform in quality when examined in accordance with 3.8.1 and 3.8.2.

4. VERIFICATION

4.1 Classification of inspections.

- a. Qualification inspection (see 4.4).
- b. Verification of qualification (see 4.4.4).
- c. In-process inspection (see 4.5)
- d. Conformance inspection (T and U levels: see 4.6.3 and 4.6.4. M level: see 4.6.3).
- e. Periodic inspection (M level only, see 4.6.4).

4.2 QPL system. The manufacturer shall establish and maintain a QPL system in accordance with 3.3. Evidence of such compliance is a prerequisite for qualification and retention of qualification.

4.2.1 Purchased raw materials. The following documentation for purchased raw materials shall be retained:

- a. Procurement documentation: Traceability.
- b. Physical and chemical property data.
- c. Performance evaluation/characterization data, if applicable.

4.2.2 In-house prepared materials. The following documentation for in-house prepared materials shall be retained:

- a. Fabrication process control data.
- b. Physical and chemical property data.
- c. Performance evaluation/characterization data, if applicable.

4.2.3 Manufacturing lot performance information. Lot performance information relating to material, process, lot conformance, inspections, and product shall be retained by the manufacturer for 10 years from the date of the manufacture of the capacitors.

4.3 Inspection conditions and reference measurements.

4.3.1 Conditions. Unless otherwise specified herein, all inspections shall be made in accordance with the "GENERAL REQUIREMENTS" of MIL-STD-202 except relative humidity shall not exceed 75 percent. Accuracy of all test voltage measurements shall be within ± 2.0 percent of the specified voltage. Unless otherwise specified herein, all test temperatures above +25°C shall have a tolerance of +4°C, -0°C.

4.3.2 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at +25°C ± 3 °C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ± 2 percent or less of the specified test voltage.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.3.4 Manufacturer's production inspection. The manufacturer may perform tests equal to or more stringent than those specified in in this document if approved by the qualifying activity. The following criteria shall be complied with:

- a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than that specified. NOTE: Includes optional voltage conditioning (see [4.7.4.2.3](#)).
- b. The parameters measured and the failure criteria shall be the same or more stringent than those specified herein.
- c. The lot rejection criteria are the same or more stringent than that specified herein.
- d. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification and concurrence by the qualifying activity.

4.3.5 Mounting. When specified in the test procedure, the capacitor shall be mounted on an FR4 or ceramic substrate board. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a capacitor in any of the tests for which it may be used. The test board shall be prepared with metallized areas of proper spacing to facilitate the mounting of the capacitors to the test board in order to provide both mechanical and electrical connection to the capacitor as required by the specific test. Unless otherwise specified, the dimensions of the test card are optional. The test board metallization material shall be compatible with the soldering technique to be employed and the material used on the capacitor termination. Capacitors shall be mounted on a test board by soldering the capacitor terminations directly to the test board metallized areas in accordance with the following:

- a. Solder and soldering flux shall be of such a quality as to enable the capacitors to meet all the requirements of this specification and shall be applied to the terminations of each capacitor.
- b. All capacitors shall be placed across the metallized areas of the test board with contact between the capacitors terminations and board metallized areas only. The use of adhesive to keep capacitors in place during mounting operation is allowable.
- c. Only ambient air cooling shall be used.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see [6.3](#)), on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample size. The number of capacitors to be submitted for qualification inspection shall be as specified in [table XIV](#) and in [appendix A](#).

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in [table XIV](#). Sample units shall have been subjected to the in-process screening required by this specification (see [4.5](#)). All sample units shall be subjected to the inspection of group I and group II. The sample shall then be divided as specified in [table XIV](#) as applicable.

4.4.3 Failures. Failures in excess of those allowed in [table XIV](#) shall be cause for refusal to grant qualification approval.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE XIV. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of failures allowed <u>1/</u>
<u>Group I (Screening)</u>				
Thermal shock	3.9	4.7.4.1	90 min. <u>2/</u>	See table XVIII
Voltage conditioning	3.9	4.7.4.2		
Insulation resistance (at +125°C)	3.10	4.7.5.2		
Dielectric withstanding voltage	3.11	4.7.6		
Insulation resistance (at +25°C)	3.10	4.7.5.1		
Capacitance	3.12	4.7.7		
Dissipation factor	3.13	4.7.8		
Visual examination			All	N/A
Ceramic body defects <u>4/</u>	3.8.1	4.7.3.1		
Lead attachment defects	3.8.2	4.7.3.2		
<u>Group II</u>				
Visual and mechanical examination; material, physical dimensions, design, construction, marking, and workmanship	3.1, 3.4, 3.25, and 3.27	4.7.3.3	90 <u>3/</u>	1
<u>Group III</u>				
Destructive physical analysis	3.14	4.7.9	6	0
<u>Group IV</u>				
Solderability	3.15	4.7.10	5	0
<u>Group V</u>				
Thermal shock	3.9	4.7.4.1	24	1
Life	3.16	4.7.11		
<u>Group VI</u>				
Shock, specified pulse	3.17	4.7.12	12	1
Resistance to soldering heat	3.18	4.7.13		
Temperature humidity bias	3.19	4.7.14		
<u>Group VII</u>				
Temperature characteristic	3.20	4.7.15	12	1
Vibration, high frequency	3.21	4.7.16		
<u>Group VIII</u>				
Terminal strength or peel force	3.22	4.7.17	12	0
<u>Group IX</u>				
Dielectric breakdown voltage	3.23	4.7.18	12	0
<u>Group X</u>				
Resistance to solvents (ink marking only)	3.24	4.7.19	6	1

1/ A sample unit having one or more defects will be charged as a single defective.

2/ Additional samples over the 90 minimum should be included, based on table XVIII, to allow for the percent defective allowable.

3/ One additional unit is included in the 90 unit sample to allow for the permitted defective in group II.

4/ Some ceramic chip surfaces may not be visible post assembly. The criteria of 3.8.1 shall apply only to visible ceramic defects.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.4.4 Verification of qualification. Every 12 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

- a. [MIL-STD-790](#) program.
- b. Product design has not been modified.
- c. Certification that the manufacturer still maintains the capabilities and facilities necessary to produce these items.
- d. Verification of the results of group A and group B inspections including identification of failed lots and subgroups and failure modes.

In the event that no production occurred during the reporting period, the manufacturer shall certify that it retains the capabilities and facilities necessary to produce the item. If during 2 consecutive reporting periods there has been no production, the manufacturer may be required, at the discretion of the qualifying activity, to submit the products to testing in accordance with the qualification inspection requirements.

4.5 In-process inspection. Each production lot shall be inspected as individual chips in accordance with [table XV](#).

TABLE XV. In-process inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Ultrasonic inspection (pre-termination) (T and U levels only)	3.6	4.7.1	100%
Chip level DPA (pre-termination) (T and U levels only ^{1/})	3.7	4.7.2	see table XVI
Ultrasonic inspection (post termination, pre-assembly) (U level only)	3.6	4.7.1	100%
Chip level DPA (post-termination) (U level only)	3.7	4.7.2	see table XVI
Visual examination (post termination, pre-assembly)	3.8.1	4.7.3.1	100%

^{1/} For U level, chip level DPA (pre-termination) is at the option of the manufacturer.

TABLE XVI. Chip level destructive physical analysis sample size.

Lot size	Minimum sample size	Accept	Reject
1 – 500	14	0	1
501 – 10000	32	1	2
10001 – 35000	50	2	3
35001 – 500000	80	3	4

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery. Inspection of M level product for delivery shall consist of the in-process inspection and group A inspection. Inspection of T and U level product for delivery shall consist of the in-process inspection, group A, and subgroups 1 and 2 of group B.

4.6.2 Inspection and production lot.

4.6.2.1 Inspection lot. An inspection lot shall consist of all capacitors of the same dielectric classification (class I or class II (see [table I](#))), produced under essentially the same conditions with the same basic materials, and offered for inspection at one time. Samples selected from the inspection lot shall be representative of the capacitance values and voltages in the approximate ratio of production.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.6.2.2 Production lot. A production lot shall consist of all capacitors of a single nominal capacitance/voltage rating of one design, from the same dielectric material lot, and processed as a single lot through all manufacturing steps on the same equipment. The lot may contain all standard capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:

- a. For T and U level capacitors, a production lot of stacked capacitors shall be manufactured with chips from a single chip lot. A single chip lot is one that is processed from a single lot of dielectric powder on a continuous basis. In addition, a single chip lot shall conform to the following:
 - (1) Raw materials, such as end termination base material, ceramic raw material, binders, and electrode ink, shall be traceable to the same lot and be from the same contractor.
 - (2) A lot number shall be assigned before electrode printing (inking) and be manufactured from the same slurry and cast on the same belt or comparable equipment (see 3.4).
 - (3) A single mix of a basic ceramic formulation fired through one kiln with one temperature profile during the process, with constant dielectric design, with, in general, no more than 20 percent variation in the number of active dielectrics being assembled in one continuous buildup. Sublots may be allowed to provide a spread in capacitance value to improve the yield. This will normally be done in the case of tight tolerances and low capacitance. In some cases, more than 20 percent variation in the number of active dielectrics may be required in these circumstances.
 - (4) End termination base material shall be consistent in formulation and traceable to a single batch and shall be fired in the same kiln with one temperature profile during the process. All capacitors shall enter the kiln in one continuous operation/run for end termination firing.
- b. Lot identity shall be maintained from the time the lot is assembled to the time it is accepted.
- c. The lot date code shall be assigned prior to the start of group A.
- d. The manufacturer may manufacture and test the production lot based on the voltage rating for that design and subsequently supply the final product at any voltage rating equal to or less than that for which it was manufactured and tested.

4.6.3 Group A inspection. Group A inspection shall consist of the inspections specified in [table XVII](#). The following details shall apply:

- a. Failure to meet percent defectives allowable (PDA) limits shall cause the lot to be rejected.
- b. For T and U level capacitors, a summary of the results of group A inspection on each lot that meets requirements shall be submitted to the purchaser with the capacitors.
- c. For T and U level capacitors, a copy of the applicable DPA report shall be submitted to the purchaser with each lot of capacitors.

4.6.3.1 Subgroup 1.

4.6.3.1.1 Sampling plan. Subgroup 1 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Capacitors failing the tests of subgroup 1 shall be removed from the lot. If screening requires more than the percent defectives allowable (PDA) in [table XVIII](#), the entire lot shall be rejected.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE XVII. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure	
<u>Subgroup 1</u> Thermal shock and voltage conditioning <u>1/ 2/</u>	3.9	4.7.4	100% inspection (see table XVIII)	
Visual examination <u>3/</u> Ceramic body defects <u>4/</u> Lead attachment defects	3.8.1 3.8.2	4.7.3.1 4.7.3.2	100% inspection	
<u>Subgroup 2</u> Visual and mechanical examination: Material, physical dimensions, design, construction, marking, and Workmanship	3.1, 3.4, 3.25, and 3.27	4.7.3.3	13 samples 0 failures	
<u>Subgroup 3</u> DPA (T and U levels only)	3.14	4.7.9	3 samples 0 failures	
<u>Subgroup 4</u> Solderability <u>5/</u>	3.15	4.7.10	M Level 5 samples 0 failures	T and U levels 3 samples 0 failures

- 1/ The DWV post-test is not applicable if optional voltage conditioning was performed at 250 percent or more of the rated voltage.
- 2/ Capacitance and dissipation factor failures shall be removed from the lot but shall not be considered defective for the determination of the PDA (see [4.6.3.1.1](#) and [table XVIII](#)).
- 3/ Visual examination may be performed at any time during subgroup 1.
- 4/ Some ceramic chip surfaces may not be visible post assembly. The criteria of [3.8.1](#) shall apply only to visible ceramic defects.
- 5/ The manufacturer may request the deletion of the subgroup 4 solderability test, provided an inline or process control system for assessing and assuring the solderability of leads can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement.

4.6.3.1.2 Rejected lots. Rejected T and U level lots shall not be supplied to this specification; however, they may be supplied as M level product provided they meet all of the M level requirements. For M level capacitors, production lots exceeding 10 percent or 1 unit, whichever is greater, defective allowable (see [table XVIII](#)) shall be segregated from new lots that have passed inspection. Rejected lots may be offered for acceptance only if the manufacturer 100 percent retests to the requirements of subgroup 1. Resubmitted lots shall be kept separate and shall be clearly identified as resubmitted lots. If, during 100 percent re-inspection to subgroup 1, the lot exceeds 5 percent or 1 unit, whichever is greater, defective, the lot shall be rejected and shall not be supplied to this specification.

TABLE XVIII. Percent defectives allowable for qualification (group I) and group A (subgroup 1).

Product level	PDA for last 48 hours during voltage conditioning at +125°C <u>1/</u> (whichever is greater)	PDA overall <u>2/</u> (whichever is greater)
T and U	.5 percent or 1 unit	5 percent or 1 unit
M	N/A	10 percent or 1 unit

- 1/ For optional voltage conditioning, the time required for meeting the PDA shall be calculated with the $T_{test(PDA)}$ equation in [4.7.4.2.3](#).
- 2/ Overall PDA applies to voltage conditioning only.

4.6.3.2 Subgroup 2.

4.6.3.2.1 Sampling plan. Subgroup 2 tests shall be performed on an inspection lot basis for M level capacitors and a production lot basis for T and U level capacitors. In the event of one or more failures, the lot shall be rejected.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.6.3.2.2 Rejected lots. The rejected lots shall be segregated from new lots and those that have passed inspection. Rejected lots shall be 100 percent reworked or scrapped. The rejected lot may be rescreened and the defects removed. The lot may then be resubmitted to the sample plan. If one or more defects of the same type are found in this second sample, the lot is rejected and shall not be supplied to this specification. If another defect of a different type is found in the second sample, a rescreen for that defect is also permitted.

4.6.3.3 Subgroup 3 (T and U levels only).

4.6.3.3.1 Sampling plan. Three samples shall be selected randomly from every production lot and subjected to the DPA test. If there are one or more defects, the lot shall be rejected.

4.6.3.3.2 Rejected lots. Rejected lots shall not be supplied to this specification; however, they may be supplied as M level product provided they meet all of the M level requirements.

4.6.3.3 Subgroup 4.

4.6.3.4.1 Sampling plan. Solderability tests shall be performed on an inspection lot basis for M level capacitors and on a production lot basis for T and U level capacitors. The samples shall be selected randomly and subjected to the solderability test. The manufacturer may use electrical rejects from the subgroup 1 and subgroup 2 tests for all or part of the samples to be used for solderability testing. If there are one or more defects, the lot shall be rejected.

4.6.3.4.2 Rejected lots. Rejected T and U level lots shall not be supplied to this specification. If inspection lot sampling is used for M level product, each production lot used to form the rejected inspection lot shall be individually submitted to subgroup 4 testing as specified in 4.6.3.4.1. Rejected M level production lots shall not be supplied to this specification.

4.6.3.4.3 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract or order.

4.6.4 Group B inspection. Group B inspection shall consist of the tests specified in table XIX and shall be performed on sample units from lots that have been subjected to and have passed group A inspection. For T and U levels, subgroups 1 and 2 of group B shall be performed on a production lot basis (see 4.6.1). Copies of group B read and record data shall be forwarded to purchaser with T and U level capacitors. T and U level capacitors may not be shipped until the conclusion of 1,000 hours of life test. For M level, group B shall be performed on an inspection lot basis every 6 months. Except where the results of this inspection show noncompliance with the applicable requirements (see 4.6.4.4), delivery of M level capacitors which have passed group A inspection shall not be delayed pending the results of this inspection.

4.6.4.1 Subgroup 1. The number of samples required by table XIX shall be selected from each T and U level production lots. For M level product, the number of sample units required by table XIX shall be selected from production every 6 months. The samples shall be divided evenly (6 and 6) into two dielectric classification groups (class I and class II (see table I)). Capacitor sizes manufactured during the period shall be represented, as far as practical, in the approximate ratio of production for each dielectric classification. The highest capacitance value in the largest capacitor size produced in each of the two dielectric classifications shall be represented in the sample. If only one dielectric classification is produced during the period, all samples shall be of that dielectric classification; however, the total number of samples (12) shall remain unchanged.

4.6.4.2 Subgroup 2 through subgroup 4. The number of samples required by table XIX shall be taken from each T and U level production lots for subgroup 2. For M level product, the number of samples required by table XIX of each dielectric classification (class I and class II (see table I)) shall be randomly selected from inspection lots every 6 months.

4.6.4.3 Disposition of sample units. Sample units that have been subjected to group B inspection shall not be delivered on the contract.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

TABLE XIX. Group B inspection. 1/ 2/

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure	Number of defectives permitted <u>3/</u>	
<u>Subgroup 1 (every 6 months)</u> Thermal shock Life	<u>3.9</u> <u>3.16</u>	<u>4.7.4.1</u> <u>4.7.11</u>	12	1	
<u>Subgroup 2 (every 6 months)</u> Resistance to soldering heat Temperature humidity bias	<u>3.18</u> <u>3.19</u>	<u>4.7.13</u> <u>4.7.14</u>	12	1	1 <u>7/</u>
<u>Subgroup 3 (every 6 months 5/ 6/)</u> Temperature characteristic Resistance to solvents (ink marking only) <u>8/</u> Terminal strength or peel force <u>4/</u>	<u>3.20</u> <u>3.24</u> <u>3.22</u>	<u>4.7.15</u> <u>4.7.19</u> <u>4.7.17</u>	12	1	
<u>Subgroup 4 (every 6 months)</u> Dielectric breakdown voltage	<u>3.23</u>	<u>4.7.18</u>	12	0	

1/ Group B inspection (subgroups 1 and 2 only) shall be required for each T and U level production lot.

2/ Unless otherwise specified herein, mounting of group B samples shall be at the discretion of the manufacturer.

3/ A sample unit having one or more defects shall be charged as a single defective.

4/ Sample size shall be 3 pieces with zero defectives permitted. The manufacturer may use group A subgroup 1 rejects for all or part of the sample to be used for terminal strength or peel force testing.

5/ For M level only, if a manufacturer can demonstrate that the subgroup 3 test has been performed five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.

6/ At the option of the manufacturer, separate/additional samples may be used for each test. The combined failures shall not exceed the number of failures allowed indicated in [table XIX](#).

7/ Total of one defective allowed for the combination of subgroup 2 and subgroup 3 inspections.

8/ Sample size shall be 4 pieces with zero defectives permitted.

4.6.4.4 Noncompliance.

4.6.4.4.1 M level noncompliance. If a sample unit fails to pass group B inspection, the manufacturer shall notify the qualifying activity and cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group B inspection shall be repeated on additional sample units (all inspections), or the inspection that the original sample failed, at the option of the qualifying activity. Group A inspection may be reinstituted, however, final acceptance shall be withheld until the group B inspection has shown that corrective action was successful. In the event of failure after re-inspection, information concerning the failure and corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

4.6.4.4.2 T and U level noncompliance. If the sample fails to pass group B inspection, the production lot shall not be delivered on the contract or order.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.7 Methods of examination and test.

4.7.1 Ultrasonic inspection (T and U levels only) (see 3.6). Capacitors shall be examined in accordance with MIL-STD-202-220. The following details and exceptions shall apply:

- a. Output device: Either a hard or soft copy shall be acceptable provided defects are noted on the copy. Soft copies shall be in a non-proprietary software format.
- b. Views: Views shall be bulk scan.
- c. Scan resolution: Scan resolution shall be 0.005 inch or less, transducer frequency up to 100 MHz (NOTE: For detection, the flaw must be a minimum of half the wavelength). Capacitors greater than 0.055 inch thick shall be imaged double-sided. At the option of the manufacturer, all capacitors may be imaged double-sided.
- d. Summary of results. A summary of the results of the ultrasonic inspection shall be included in the group A data that is submitted to the acquiring activity with the capacitors (see 4.6.3b). At a minimum, this summary shall include the number of capacitors tested, number of capacitors rejected, and the date inspected.
- e. Retention: Retention period shall be in accordance with 4.2.3.

4.7.2 Chip level DPA (T and U levels only) (see 3.7). Capacitors shall be examined in accordance with ECIA EIA-469. The following details shall apply:

- a. Sectioning of cast samples: After sectioning in accordance with ECIA EIA-469, the following is recommended to accurately detect feature size:
 - (1) After finishing with grit 600, move to 800, then 1000, then 1200, and finally 2400 grit or finer before the final polish with sub-micron diamond (0.3 micron or smaller) or alumina powder and a short/low nap cloth.
 - (2) Low pressure should be used during grinding.
 - (3) Plenty of water flow should be used.
 - (4) A minimal amount of time should be spent on the final polish.
- b. Recommended illumination techniques: Use of either vicinal illumination (see 6.7), dark-field illumination with a polarizer, or other techniques approved by the qualifying activity is recommended for inspection for cracks in the ceramic.
- c. For capacitors with very small design features, scanning electron microscopy may be necessary to properly disposition the DPA requirements specified in ECIA EIA-469 and herein.

4.7.3 Visual examination.

4.7.3.1 Visual examination (ceramic body defects) (see 3.8.1). Capacitors shall be visually examined using 7X to 10X magnification, for the criteria specified in 3.8.1.

4.7.3.2 Visual examination (lead attachment defects) (see 3.8.2). After assembly, all capacitor stacks shall be visually examined using 7X to 10X magnification, for the lead attachment criteria specified in 3.8.2.

4.7.3.3 Visual and mechanical examination. All capacitors shall be examined using 7X to 10X magnification to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, and 3.27).

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.7.4 Thermal shock and voltage conditioning (see 3.9). Capacitors shall be subjected to the tests of 4.7.4.1 and 4.7.4.2.

4.7.4.1 Thermal shock. Capacitors shall be tested in accordance with MIL-STD-202-107. The following details shall apply:

a. Test condition A, except that in step 3, units shall be tested at +125°C.

b. Number of cycles:

(1) Qualification:

(a) Group I:

(i) T and U levels: 20 cycles.

(ii) M level: 5 cycles.

(b) Group V:

(i) T and U levels: 100 cycles.

(ii) M level: 5 cycles.

(2) Group A:

(a) T and U levels: 20 cycles.

(b) M level: 5 cycles.

(3) Group B:

(a) T and U levels: 100 cycles.

(b) M level: 5 cycles.

c. Mounting:

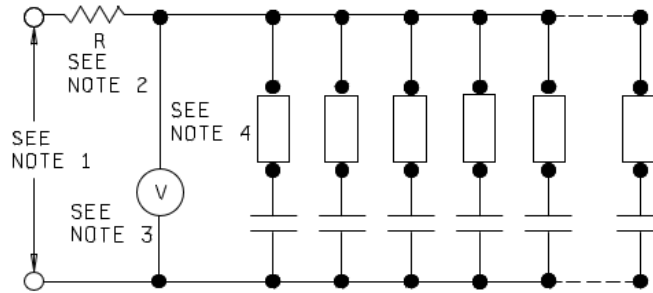
(1) Qualification (group V) and group B: Capacitors shall be mounted in accordance with 4.3.5.

(2) Qualification (group I) and group A: Not applicable.

4.7.4.2 Voltage conditioning. Capacitors shall be subjected to the voltage conditioning test in 4.7.4.2.1 for M level or 4.7.4.2.2 for T and U levels, or the optional voltage conditioning test in 4.7.4.2.3. It shall be verifiable that all parts offered for electrical tests have been exposed to the required voltage conditioning for the required time duration. When the optional voltage conditioning test of 4.7.4.2.3 is used, the traveler shall include the specific accelerated voltage used and the test duration. See figure 3 for a suggested test circuit. An alternate test circuit can be used, provided the notes of figure 3 are followed.

4.7.4.2.1 M level standard voltage conditioning. Voltage conditioning shall consist of applying a minimum of twice the rated voltage (120 percent of rated voltage for 500 volt rated parts) to the capacitors at the maximum rated temperature +4°C, -0°C for 100 hours, +25 hours, -4 hours. Voltage shall be applied and shall reach maximum value within 2 minutes, maximum. After completion of the exposure period, the electrical measurements of 4.7.4.3 shall be performed.

MIL-PRF-STACK
DRAFT DATED 16 June 2026



NOTES:

1. The power supply shall be capable of supplying the required test voltage.
2. The current limiting device shall be a resistor and/or a fuse. The current shall be limited to no more than 10A.
3. There shall be a voltage monitor that will trigger an alarm and shut off the test if the applied voltage drops by more than 5 percent. Time without voltage does not apply toward the minimum voltage conditioning hours (see 4.7.4.2.1 and 4.7.4.2.2).
4. At the option of the manufacturer, a fuse or a resistor may be used in series with each capacitor. The value of the resistors and fuses shall be such that they do not restrict the power supply's ability to provide the required test voltage to the capacitor under test (± 5 percent).

FIGURE 3. Suggested test circuit.

4.7.4.2.2 T and U level standard voltage conditioning. Voltage conditioning shall consist of applying twice the rated voltage (120 percent of rated voltage for 500 volt rated parts) to the units at the maximum rated temperature of +125°C +4°C, -0°C for a minimum of 168 hours and a maximum of 264 hours. Voltage conditioning may be terminated at any time during the 168 to 264 hour time interval, provided that the number of failures detected during the last 48 hours of test meets the PDA requirements specified in table XVIII. Failures shall be determined by blown fuses or hot IR failures. Voltage shall be applied and shall reach maximum value within 2 minutes, maximum. After completion of the exposure period, the electrical measurements of 4.7.4.3 shall be performed.

4.7.4.2.3 Optional voltage conditioning (voltage ratings of 200 volts or less only). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning tests of 4.7.4.2.1 or 4.7.4.2.2. All conditions of 4.7.4.2.1 (M level) or 4.7.4.2.2 (T and U levels only) apply, with the exception of the voltage applied, the test time, and the time required for meeting the PDA (T and U levels only). The accelerated condition selected for the optional voltage conditioning shall be used for the duration of the test. At no time shall a combination of standard and optional voltage conditioning be allowed on the same samples. The minimum time duration, $T_{test(min.)}$, and the time required for meeting the PDA (T level), $T_{test(PDA)}$, shall be calculated as follows:

$$T_{test(min.)} = \frac{A}{(E_{test}/E_{rated})^3} \quad T_{test(PDA)} = \frac{384}{(E_{test}/E_{rated})^3}$$

Where: $2 \times E_{rated} \leq E_{test} \leq 4 \times E_{rated}$

- | | | |
|------------------|---|--|
| E_{test} | = | Applied voltage |
| E_{rated} | = | Rated voltage of the capacitor |
| $T_{test(min.)}$ | = | Minimum test time in hours |
| $T_{test(PDA)}$ | = | Time required for meeting the PDA (T and U levels only) |
| A | = | 1344 for T and U levels or 800 for M level based on an acceleration factor of 8:1. |

4.7.4.3 Measurements after testing (see 3.9). After completion of the exposure period, the following electrical measurements shall be performed.

- a. Insulation resistance (+125°C): In accordance with 4.7.5.2. NOTE: This step may be skipped if step c is done at +125°C with +25°C test limits.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- b. Dielectric withstanding voltage: In accordance with [4.7.6](#).
- c. Insulation resistance (+25°C): In accordance with [4.7.5.1](#).
- d. Capacitance: In accordance with [4.7.7](#).
- e. Dissipation factor: In accordance with [4.7.8](#).

The manufacturer has the option of performing these electrical tests in any order except insulation resistance shall always be measured after dielectric withstanding voltage. If the voltage conditioning test is performed with individual fuses in series with each capacitor, any capacitor tested in a position where a fuse fails shall be tested for insulation resistance and dielectric withstanding voltage. If the capacitor meets the initial requirements for insulation resistance and dielectric withstanding voltage, the capacitor shall be rejected but shall not count against the PDA in [table XVIII](#). The manufacturer also has the option to not test capacitors with fuse failures and count these toward the PDA.

[4.7.5 Insulation resistance \(see 3.10\)](#). Capacitors shall be tested in accordance with [MIL-STD-202-302](#). The following details shall apply.

[4.7.5.1 Insulation resistance at +25°C](#).

- a. Test potential: Rated voltage, minimum.
- b. Test temperature: +25°C
- c. Special conditions: If a failure occurs at a relative humidity above 50 percent, the insulation resistance may be measured again at any relative humidity less than 50 percent.
- d. Points of measurement: Between the mutually insulated points.

[4.7.5.2 Insulation resistance at +125°C](#).

- a. Test potential: Rated voltage minimum.
- b. Test temperature: +125 ± 3°C
- c. Special conditions: Capacitors shall have stabilized at +125°C with test voltage applied prior to performing the test.
- d. Points of measurement: Between the mutually insulated points.

[4.7.6 Dielectric withstanding voltage \(see 3.11\)](#). Capacitors shall be tested in accordance with [MIL-STD-202-301](#). The following details shall apply:

- a. Magnitude and nature of test voltage: A minimum of 150 percent of the dc rated voltage for 500 volt rated parts, 250 percent to 400 percent of the direct current rated voltage for all other voltage ratings (see [3.1](#)).
- b. Duration of application of test voltage: 5 seconds ± 1 second. The test voltage shall be raised from zero volts to the specified value within 1 second, maximum.
- c. Points of application of test voltage: Between the capacitor-element terminals.
- d. Limiting value of surge current: Shall be limited to between 30 mA and 50 mA.
- e. Examination after test: Capacitors shall be examined for evidence of damage and breakdown.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

4.7.7 Capacitance (see 3.12). Capacitors shall be tested in accordance with MIL-STD-202-305. The following details and exceptions shall apply:

- a. Test frequency shall be as shown in table XX.

TABLE XX. Capacitance test frequency.

Test frequency	Characteristic	
	Class I	Class II ^{1/}
1 MHz $\pm$ 100 kHz	$\leq$ 1,000 pF	$\leq$ 100 pF
1 kHz $\pm$ 100 Hz	$>$ 1,000 pF	$>$ 100 pF and $\leq$ 10 μ F
120 Hz $\pm$ 10 Hz	N/A	$>$ 10 μ F

^{1/} At the option of the manufacturer, the capacitance measurement of a 100 pF class II capacitor may be performed at either 1 MHz $\pm$ 100 kHz or 1 kHz $\pm$ 100 Hz.

- b. Voltage: A root-mean-square potential of 1.0 ± 0.2 volt for 1MHz and 1kHz and 0.5 ± 0.1 volt for 120Hz.

NOTE: Following a dielectric withstanding voltage or insulation resistance test, capacitance measurement may be delayed for a period up to 24 hours.

4.7.8 Dissipation factor (see 3.12). The dissipation factor shall be measured with a capacitance bridge or other suitable method at the frequency and voltage specified in 4.7.7. Unless otherwise specified, the inherent accuracy of the measurement shall be ± 2 percent of the reading plus 0.1 percent dissipation factor (absolute). Suitable measurement techniques shall be used to minimize errors due to the connections between the measuring apparatus and the capacitor. The dissipation factor shall be measured under the same conditions as capacitance.

4.7.9 DPA (see 3.14). Capacitors shall be examined as specified in ECIA EIA-469 for the criteria specified in 3.14.

4.7.10 Solderability (see 3.15). Capacitors shall be tested in accordance with MIL-STD-202-208. The following details shall apply:

- a. The capacitors shall be preheated. The preheat shall not exceed 4°C per second. The maximum preheat temperature shall be within 50°C of the solder bath temperature.
- b. Number of terminations to be tested: All leads (see 3.1).

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- c. Coating durability: 2 as specified in [IPC/JEDEC J-STD-002](#), except preconditioning category C (8 hours $\pm$ 15 minutes steam conditioning).
- d. The leads shall be immersed above the lead bend.

4.7.11 Life (at +125°C) (see 3.16). Capacitors shall be tested in accordance with [MIL-STD-202-108](#). The following details and exceptions shall apply:

- a. Mounting: Capacitors shall be mounted in accordance with [4.3.5](#).
- b. Distance of temperature measurements from specimens, in inches: Not applicable.
- c. Test temperature and tolerance: +125°C, +4°C, -0°C.
- d. Procedure: Capacitors shall be subjected to the voltage and circuit specified in [4.7.4.2.2](#). In the event of a fuse failure, the procedure specified in [4.7.4.2.2](#) shall apply.
- e. Test duration:
 - (1) Qualification:
 - (a) T and U level: 4,000 hours.
 - (b) M level: 1,000 hours.
 - (2) Group B: 1,000 hours.
- f. Measurements during and after exposure: At the conclusion of 250, 1,000, 2,000, and 4,000 hours for T and U levels, 1,000 hours for M level, and while the capacitors are at the applicable high-test temperature, the insulation resistance shall be measured in accordance with [4.7.5.2](#). At the option of the manufacturer, M level readings may also be taken at 250 hours. At the option of the manufacturer, the units may be transferred to another chamber maintained at the same temperature for the purpose of measuring insulation resistance. The insulation resistance measurement shall be made only after the units have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in [4.3](#) and shall be visually examined for evidence of mechanical damage and obliteration of marking; capacitance, dissipation factor, and insulation resistance shall be measured in accordance with [4.7.7](#), [4.7.8](#), and [4.7.5.1](#), respectively.

4.7.12 Shock, specified pulse (see 3.17). Capacitors shall be tested in accordance with [MIL-STD-202-213](#). The following details shall apply:

- a. Mounting: Capacitors shall be rigidly mounted by the body.
- b. Test condition I: 100 G's.
- c. Measurements during shock: During the last shock in each direction, an electrical measurement shall be made to determine intermittent contacts of 0.5 ms or greater duration, or open-circuiting or short-circuiting.
- d. Examination after shock: Capacitors shall be visually examined for evidence of breakdown, arcing, and mechanical damage.

4.7.13 Resistance to soldering heat (see 3.18). Capacitors shall be tested in accordance with [MIL-STD-202-210](#). The following details and exceptions shall apply:

- a. Mounting: Capacitors shall be mounted in accordance with [4.3.5](#).

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- b. Test condition: I, except with only one heat cycle. NOTE: The combination of the mounting process and one heat cycle is effectively equivalent to two heat cycles.
- c. Measurements after test: Insulation resistance at +25°C, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.5.1, 4.7.7, and 4.7.8, respectively.
- d. Examination after test: Capacitors shall be visually examined for evidence of mechanical damage.

4.7.14 Temperature humidity bias (see 3.19). Capacitors shall be tested in accordance with the following:

- a. Mounting: Capacitors shall be mounted in accordance with 4.3.5.
- b. Procedure: Capacitors shall be subjected to an environment of +85°C with 85 percent relative humidity. A dc potential of rated voltage (± 5 percent) shall be applied continuously.
- c. Duration:
 - (1) Qualification: 1000 hours, minimum.
 - (2) Group B: 96 hours, minimum.
- d. Test circuit: There shall be one series resistor for each capacitor under test. The value of the series resistor shall be such that there is not greater than 5 percent voltage drop across the resistor as long as the IR value of the capacitor meets the IR specification.
- e. Measurements after test: Capacitors shall be removed from the chamber and allowed 3 hours $\pm$ 30 minutes to dry and stabilize at +25°C. IR shall then be measured in accordance with 4.7.5.1.

4.7.15 Temperature characteristic (see 3.20). The temperature of each capacitor shall be varied as specified in table XXI. Capacitance measurements shall be made at the frequency and voltage specified in 4.7.7. Capacitance measurements shall be made at each step specified in table XXI and at a sufficient number of intermediate points between step B and step D to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken only after the test temperature has stabilized.

TABLE XXI. Temperature characteristic cycle.

Step	Voltage, dc	Temperature, °C
A	None	+25 $\pm$ 2
B	None	-55 $\pm$ 2
C <u>1/</u>	None	+25 $\pm$ 2
D	None	+125 $\pm$ 2

1/ Reference point.

4.7.16 Vibration, high frequency (see 3.21). Capacitors shall be tested in accordance with MIL-STD-202-204. The following details and exception shall apply:

- a. Mounting: Capacitors shall be rigidly mounted; by the body. Electrical connections to the leads shall be made in such a manner that the leads are not damaged during the vibration test (i.e., external wiring to the capacitor shall be sufficiently supported). The test fixture shall be so constructed as to preclude any resonance within the test range. An examination of the mounting fixture shall be made on a vibrator. If any resonant frequencies are observed, adequate steps must be taken to damp the structure.
- b. Electrical load conditions: During the test, a dc potential equal to rated voltage or 200 volts, whichever is less (see 3.1), shall be applied between the terminals of the capacitor element under test.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

- c. Test condition D: 20 G's.
- d. Duration and direction of motion: Three hours in each of three mutually perpendicular planes.
- e. Measurements during vibration: During the last cycle in each direction, an electrical measurement shall be made to determine intermittent contacts of 0.5 ms or greater duration, or open-circuiting or short-circuiting.
- f. Examination after vibration: Capacitors shall be visually examined for evidence of mechanical damage.

4.7.17 Terminal strength or peel force (see 3.22).

4.7.17.1 Terminal strength (see 3.22.1). Capacitors shall be tested in accordance with MIL-STD-202-211. The following details and exceptions shall apply:

- a. Test condition A.
- b. Preparation of specimen: At the option of the manufacturer, the leads may be straightened prior to testing.
- c. Method of holding: Capacitors shall be held firmly by the body without contacting the lead frame. The load shall be applied gradually and evenly across the length of one terminal. For configurations J, L, K, M, F, and D the load shall be applied to all feet evenly via special fixturing or by soldering a tie bar across the feet at or above the lead bend.
- d. Applied force: 2 pounds.
- e. Direction of applied force: The point of application of the force and the force applied shall be in the same plane as the lead frame as shown in figure 4.
- f. Examination after test: Capacitors shall be visually examined for evidence of loosening or rupturing of the terminals.

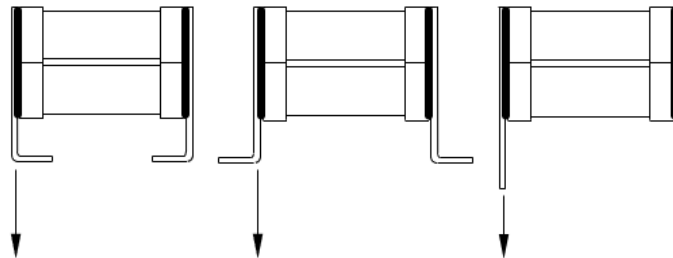


FIGURE 4. Terminal strength - direction of applied force.

4.7.17.2 Peel force (see 3.22.2). Capacitors shall be tested in accordance with the following:

- a. Preparation: Capacitor leads shall be bent through 90° such that a tensile force applied to the leads will result in a peeling force being applied to the lead frame attachment as shown in figure 5.
- b. Mounting: Capacitors shall be held by the leads. For configurations J, L, K, M, F, and D the load shall be applied to all feet evenly via special fixturing or by soldering a tie bar across the feet.
- c. Procedure: A tensile force shall be applied evenly in the direction shown in figure 5 until the lead frame attachment peels. The force required to peel the lead frame attachment shall be recorded.

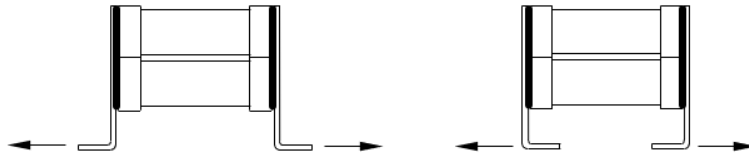


FIGURE 5. Terminal strength - direction of applied force.

4.7.18 Dielectric breakdown voltage (see 3.23). Each capacitor in the sample shall be connected in series with an instrument to measure current. The current measuring instrument shall be capable of measuring in μA or mA . A dc voltage shall be gradually applied at no greater than 175 volts per second until a breakdown occurs. Breakdown is when the leakage current reaches or exceeds 5 mA . Voltage at time of breakdown shall be recorded. If surface arcing occurs, the samples may be coated or immersed in a dielectric fluid such as peanut oil or a stable fluorocarbon-based insulating liquid.

NOTE: Care should be taken when testing high capacitance values (i.e. $\geq 4.7 \mu\text{F}$). Initial in-rush or charging currents may exceed the equipment's "trigger" level; registering a failure prior to the capacitor experiencing breakdown.

4.7.19 Resistance to solvents (ink marking only) (see 3.24). Capacitors shall be tested in accordance with MIL-STD-202-215. The following details shall apply:

- a. The marked portion of the capacitor body shall be brushed.
- b. Capacitors shall be visually examined for evidence of mechanical damage and obliteration of marking.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but not mandatory.)

6.1 Intended use. These capacitors are primarily designed for use where a small physical size with comparatively large electrical capacitance and high insulation resistance is required. General purpose (class II dielectrics, see table I) ceramic capacitors are not intended for frequency-determining or precision circuits but are suitable for use as by-pass, filter, and noncritical coupling elements in high-frequency circuits. All of these applications are of the type where dissipation factor is not critical and moderate changes due to temperature, voltage, and frequency variations do not affect the proper functioning of the circuit. Class I dielectric (see table I) ceramic capacitors are for use in critical frequency determining applications, timing circuits, and other applications where absolute stability is required. Three product levels are offered: M level (standard reliability) and T and U levels for higher reliability applications.

6.1.1 Precautionary note. Capacitors covered by this specification are very susceptible to thermal shock damage due to their large ceramic mass. Temperature profiles used should provide adequate temperature rise and cool-down time to prevent damage from thermal shock. The capacitors should be preheated. The preheat and cool down should not exceed 4°C per second. The maximum preheat temperature should be within 50°C of the solder bath temperature. Consult manufacturers for further recommendations.

MIL-PRF-STACK
DRAFT DATED 16 June 2026

6.1.2 Precautionary note. Capacitors covered by this specification have high mass and are susceptible to thermal and mechanical damage. Special board assembly processing and mounting precautions may be necessary, especially in high vibration environments. Consult manufacturers for recommendations.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification, the applicable specification sheet, and the complete PIN (see 1.2.1).
- b. Capacitor marking requirements (see 3.25.2 and 3.25.3).
- c. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from the DLA Weapons Support (Columbus), ATTN: VAT, PO Box 3990, Columbus, OH 43218-3990, or by email to vqp.chief@dla.mil.

6.3.1 Copies of SD-6, "Provisions Governing Qualification", are available online at <http://quicksearch.dla.mil/>.

6.4 Definitions.

6.4.1 Crack. A crack is a very slight separation along or across a boundary that usually occurs after sintering.

6.4.2 Delamination. A delamination is a significant separation along a material boundary or layer that occurs prior to or during sintering.

6.4.3 Chip-in. A chip-in is an area where ceramic can be seen to be forming a chip-out; however, the ceramic is still intact.

6.4.4 Chip-out. A chip-out is an area where ceramic has broken free from the capacitor.

6.4.5 Pinholes. A pinhole is a circular hollow or cavity.

6.4.6 Striations. Striations are vitrified layers without any actual separation.

6.5 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to [ASTM-B545](#) (Standard Specification for Electrodeposited Coatings of Tin).

6.6 Subject term (key word) listing.

Dielectric withstanding voltage
Dissipation factor
Insulation resistance
Base metal electrode
Precious metal electrode

6.7 Vicinal Illumination. For information regarding vicinal illumination, see S. Hull, "Nondestructive Detection of Cracks in Ceramics Using Vicinal Illumination", ASM International, Nov. 1999, ISBN 0-87170-646-6.

6.8 Changes from previous issue. Not applicable.

MIL-PRF-STACK
DRAFT DATED 16 June 2026
APPENDIX A

PROCEDURE FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix details the procedure for submission of samples for qualification inspection of capacitors covered by this specification. The procedures for extending qualification of the required sample to other capacitors covered by this specification are also outlined herein. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

A.2 SUBMISSION

A.2.1 Sample. A sample of the size required in [table XIV](#), of the highest capacitance value in each voltage rating, in each temperature characteristic, in each in each size, in each lead frame material (see [table IV](#)) for which qualification is sought shall be submitted. Any available capacitance tolerance (see [3.1](#)) for the PIN submitted for qualification may be used. Any lead style (see [table IV](#)) may be submitted.

A.3 EXTENT OF QUALIFICATION

A.3.1 Extent of qualification.

A.3.1.1 Capacitor size. Capacitor size qualification will be restricted to the capacitor size submitted.

A.3.1.2 Capacitance. Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted.

A.3.1.3 Capacitance tolerance. Qualification of any capacitance tolerance will extend to all available tolerances.

A.3.1.4 Voltage rating. Voltage rating qualification will be restricted to that submitted. Qualification may be extended to lower voltages than that submitted if the manufacturer can demonstrate that the capacitor design is the same.

A.3.1.5 Characteristic. Characteristic qualification will be restricted to that submitted.

A.3.1.6 Electrode material. Electrode material qualification will be restricted to that submitted.

A.3.1.7 Product level. Qualification of any T or U level capacitor will extend qualification to the equivalent M level capacitor with the same design. Qualification of any T level capacitor will extend qualification to the equivalent U level capacitor of the same design. The manufacturer shall request the qualifying activity to add them to the MIL-PRF-Stack QPL (Qualified Products List) for U level.

A.3.1.8 Lead frame material. Qualification of either Nickel-iron class or Phosphor-bronze class will extend qualification to the "unspecified" lead material. The manufacturer shall use qualified lead frame material (Nickel-iron class or Phosphor-bronze class) to supply configuration symbols J, L, G, or H.

A.3.1.9 Configuration. Qualification of any configuration symbol (J, L, G, H, K, M, C, B, F, D, P, R) will extend to all configuration symbols in the same lead frame material group (see [table IV](#)).

MIL-PRF-STACK
DRAFT DATED 16 June 2026

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC
Other - NA

Preparing activity:
DLA - CC

(Project 5910-2026-038)

Review activities:
Army - AR, AT, AV, MI
Navy - MC
Air Force - 19
Other - MDA

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.