

The following table summarizes changes to MIL-PRF-38535 Revision M.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
1	2.1	Update From : 2.1 <u>General</u>. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. sections 3, 4, or 5 of this specification, whether or not they are listed. To: 2.1 <u>General</u>. The documents listed in this section are specified in sections 3 or 4 of this specification. sections 3 or 4 of this specification, whether or not they are listed.	DLA Land and Maritime	Section 2 shall list only those documents referenced in sections 3 and 4 of the specification

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
2	3.4.2.2	Add new requirements for Microcircuit design and construction parameters. 3.4.2.2 <u>Qualification based on package construction</u>. . When manufacturer's desire to qualify microcircuits based on packages construction under this specification shall be as specified in the associated device specification and as specified herein. Adequacy of a device manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity. Only microcircuits offered in compliance with this specification shall be specified on a Standard Microcircuit Drawing (SMD) and shall meet the following: a. Microcircuit die shall not utilize TSV (Through Silicon Via) or TGV (Through Glass Via interconnect technology). b. Components are essentially co-planer with each other and the topography is considered "2 dimensional". Exceptions may be allowed on case by case basis (i.e. stacked die). c. The passive elements shall serve simple functions, directly interfacing with microcircuit ports (filtering, voltage shift, input/output conditioning, etc.) such that in a block diagram of the MIL-PRF-38535 device, the passive elements do not form any "block" (i.e., on their own constitute a network such that significant circuit function is implied independent of the microcircuit die). Refer to section 3.15 for passives allowed in construction of the microcircuit. d. For MCMs, an interposer is allowed to be used for connectivity of multiple flip chip die and wire bonding for standard die to die connectivity. e. The use of discrete semiconductors (diode/transistor), other complex elements/networks, thick and thin film substrate, should not be considered under MIL-PRF-38535.	JC 13.2 TG 20-02 (Definition of Hybrids vs ICs) & DLA Land and Maritime	Include package construction requirements for qualification that shall be met for acceptance in to MIL-PRF-38535 device vs other Mil-PRF-38534 or others military specifications.
3	3.6.2.a. 3.6.2.3	Add class P to the list of classes for "device class designator"	DLA Land and Maritime	Editorial
4	3.6.2.a. 3.6.2.b.	Update lead finish designator From: Y To: A	DLA Land and Maritime	Editorial typo

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5	Table IA Table II Table III Table IV Table V TABLE C-I	Add language (ceramic or organic) to Title block of tables From: Class Y To: Class Y (ceramic or organic)	DLA Land and Maritime	Adding this language for clarifying organic substrate requirements are included in class y.
6	Table IA Table II Table III Table IV Table V TABLE C-I	Add new header columns to distinguish "Hermetic" classes from "Non-hermetic" classes.	DLA Land and Maritime	Clarification
7	Table IA Table II Table III Table IV Table V TABLE C-I	Insert new screening and QCI criteria for plastic encapsulated microcircuit class N and introduce new class P: -Update existing PEM class N device requirements for military application. -Add new PEM class P device requirements for space application. Tables have been created for screening and QCI test that have additional columns itemizing test conditions for class N and class P	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	DLA conducted Engineering Practice Study for Class N comparing input from SAE AS6294 and coordination effort from JEDEC Task group. To develop a QML standard for PEMs.
8	Table IA	Update title of Table From: TABLE IA. <u>Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits.</u> To: TABLE IA. <u>Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits.</u>	DLA Land and Maritime	Added screening procedures for Non hermetic Classes N and P
9	Table IA	Screening test 4 Temperature cycle Update Class Y to add TM 1010 alternate Condition B for 15 cycles	JC13.7 Organic Class Y TG 2018-12	Alternate condition B may apply when package materials are limited in capability of meeting condition C. Coffin-Manson to calculate equivalent cycles; acceleration factor (AF)=1.4; 15 equivalent Condition B cycles

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
10	Table IA Footnote <u>4</u> /	Screening test 4 Temperature cycle Update footnote <u>4</u>/ From: <u>4</u>/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan. To: <u>4</u>/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan. For class Y devices with organic substrates, Condition B, -55 to +125 may be used.	DLA Land and Maritime	Alternate condition B may apply when package materials are limited in capability of meeting condition C.
11	Table IA footnote <u>12</u> / footnote <u>25</u> /	Update footnote <u>12</u>/ and add footnote <u>25</u>/. Apply footnote <u>12</u>/ to screening test #9, #11, #13 (class level S) devices. Apply footnote <u>25</u>/ to screening test #9, #11, #13 and #15 for (class level S) devices. •<u>12</u>/ For class, class Y and class P (class level S) microcircuit devices, pre-burn-in and post-burn-in interim electrical measurements shall be recorded and delta calculations shall be performed on 100 percent of devices. In lieu of delta measurements and calculation, equivalent statistical techniques may be used if approved by the Qualifying Activity. The specific delta parameters shall be as defined in the applicable device specification. •<u>25</u>/ For class V, class Y and class P (class level S) microcircuit devices, all specified pre-burn-in and post burn-in interim tested electrical parameters shall be read and recorded on 100 percent of devices. Specified electrical parameters that cannot be read and recorded shall be identified in the SMD if approved by the Qualifying Activity. In lieu of 100% Read and Record data collection, testing may be performed that includes automatic removal of units that are outside the normal electrical distribution of the product (outlier devices) as determined by statistical techniques if approved by the Qualifying Activity.	JC-13.2 TG 2011-01 and TG 2021-01	customers are wanting all parameters to be read and recorded, not just the delta parameters. footnote <u>12</u>/ will be split into two notes. –Delta calculation note (modified note <u>12</u>/): –Read-and-record note (new note <u>25</u>/):

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12	Table IA footnote <u>26/</u>	Add footnote <u>26/</u>. Apply footnote <u>26/</u> to screening test #15 (class level S) devices. <u>26/</u> For class V, class Y and class P (class level S) microcircuit devices, the supplier shall perform some variant of part-average-testing (PAT) and/or statistical-bin-analysis (SBA) that meets the intent of the guideline. The supplier determines the sample sizes and acceptance criteria per the test methods (see JEDEC standard JESD50C). If these tests are not possible for a given part, then the supplier shall provide justification to the Qualifying Activity. The PAT and/or SBA requirements may be performed in any sequence (e.g. at wafer sort and/or final test) in the screening flow.	JC-13.2 TG 2021-01	Apply footnote <u>26/</u> to Table 1A note for part-average-testing (PAT)
13	Table IA Screening test #17 Footnotes <u>3/</u> <u>21/</u>	Update Screening test #17, footnote <u>3/</u> and <u>21/</u> From: "SAM" To : "Acoustic Microscopy"	JC-13.2 flip chip TG 2018-01	Editorial
14	Table IA Screening test #20 Footnote <u>25/</u>	Remove screening test #20 and footnote <u>25/</u> Screening test #20 Radiation dose rate induced latch-up test <u>25/</u> TM1020 Footnote <u>25/</u> <u>25/</u> Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) subplot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.	DLA Land and Maritime	Remove radiation latch up test. This test does not belong in the screening table.

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15	Table IB	Update title of Table IB From: <u>Tests/monitors for plastic packages. 1/</u> To: <u>Tests/monitors for plastic packages (certified prior to 01 May 2023). 1/ 3/</u>	DLA Land and Maritime	Table IB only applies to legacy devices certified prior to the implementation date of this specification for rev M. of MIL-PRF-38535.
16	Table IB Test #12	Update from: "e.g., TM 1034 (dye penetrant test), cross-sectioning, C-mode scanning acoustical microscopy (CSAM) TM 2030, etc" To : "e.g., TM 1034 (dye penetrant test), cross-sectioning, acoustical microscopy (AM) TM 2030, etc"	JC-13.2 flip chip TG 2018-01	Editorial
17	Table IB Footnote <u>3/</u>	New footnote: <u>3/</u> The requirements of Table IB only apply to existing / legacy class N microcircuits with QML certification successfully completed prior to 01 May 2023, (<i>implementation date of Rev M MIL-PRF-38535</i>).	DLA Land and Maritime	The footnote allows for legacy items to remain exempt from the new class N requirements and covers existing manufacturers.
18	Table II Subgroup 2	Remove test c. and d. from all classes (Q, V, Y, class level S) columns "c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
19	Table II Subgroup 5	Apply footnote 6/ to subgroup 5 test Remove test c.and d. from class level B column. “c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.
20	Table II Footnote 6/	Update footnote 6/ From: “6/ For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, flip chip pull off test shall be performed per TM 2031 or TM 2011. Flip chip die shear test or substrate attach strength test shall be performed after underfill is cured per TM 2019 or TM 2027. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.” To: For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, TM 2019 Die Shear Strength, TM 2027 Substrate Attach Strength, or TM 2031 Flip Chip pull-off tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed on the passive elements per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.

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21	Table V Subgroup 3	Update class Y thermal shock test From: a. TM 1011 Test condition B, 15 cycles minimum a. TM 1011 Test condition B, 15 cycles minimum (Ceramic class Y only)	13.2 Manufacturer Comment	thermal shock test not applicable for QML-Y organic substrates.
22	Table V Subgroup 3	Subgroup 3 b. Temperature cycle Update Class Y to add TM 1010 alternate Condition B for 150 cycles From: b. TM 1010 Test condition C, 100 cycles minimum To: b. TM 1010 Test condition C, 100 cycles minimum or condition B 150 cycles	JC13.7 Organic Class Y TG 2018-12	Alternate condition B may apply when package materials are limited in capability of meeting condition C.
23	Table V Footnote <u>2</u> /	Update footnote <u>2</u> / Subgroup 1 (physical dimensions) and 5 (salt atmosphere) BGA/CGA packages : sample size 15/0 , but 12 samples without balls/columns means LGA level testing and 3 samples with balls/columns. From: <u>2</u> / Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns. To: <u>2</u> / Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns. For Subgroup 1 and 5, BGA/CGA packages may test 12 samples without balls/columns at land grid array (LGA) level and 3 samples with balls/columns.	DLA Land and Maritime	Both scenarios can be observed for corrosion affects in salt/seacoast atmospheric concerns test. Also, this approach is cost effective to manufacturers.

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24	Table V Footnote <u>7</u> /	Update footnote <u>7</u>/ From: <u>7</u>/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns. To: <u>7</u>/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns. For class Y devices with organic substrates, Condition B, -55 to +125 may be used.	DLA Land and Maritime	Alternate condition B may apply when package materials are limited in capability of meeting condition C.
25	Table V Footnote <u>17</u> / Footnote <u>18</u> /	Add new footnotes <u>17</u>/ and <u>18</u>/ Preconditioning shall be performed on surface mount devices in accordance with JESD22-A113, prior to subgroup 3 test for non hermetic device classes N, P and Y with organic substrates. Manufacturer may perform these test sequentially or in parallel (separate samples for 3b and 3c) in accordance to the manufacturers QM plan. Thermal shock is not applicable to class N, P, and organic class Y. <u>18</u>/ Applicability of this test to be determined by the manufacturers TRB and documented to the QM plan.	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	PEM classes N and P require preconditioning prior to Table V subgroup 3 test.

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26	6.4.4 A.3.1.3.4	Update definition From: <u>Integrated circuit (microcircuit)</u>. A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., This excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.) To: <u>Integrated circuit (microcircuit)</u>. Integrated circuit (microcircuit). A die with a high equivalent circuit element density, composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., this excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)	JC 13.2 TG 20-02 (Definition of Hybrids vs ICs) & DLA Land and Maritime	Updated for clarification
27	6.4.4.1 A.3.1.3.4.1	Update definition From: <u>Multichip microcircuit</u>. An integrated circuit or microcircuit consisting of elements formed on or within two or more semiconductor chips which are separately attached to a substrate or package. To: <u>Multichip microcircuit or multichip module (MCM)</u>. An integrated circuit or microcircuit consisting of two or more die which are attached to a substrate or package and meets all applicable requirements of section 3.4.	JC 13.2 TG 20-02 (Definition of Hybrids vs ICs) & DLA Land and Maritime	Updated for clarification of Multichip microcircuit as it applies to MIL-PRF-38535. Design and construction parameters requirements are added to section 3.4.2.2.
28	6.4.4.3 A.3.1.3.5	Remove definition from this specification at sections -6.4.4.3 & A.3.1.3.5 of revision L <u>Microcircuit module</u>. An integrated circuit, which is an assembly of microcircuits or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance, it is considered indivisible. Re-number sections A.3.1.3.6 through A.3.1.3.35 after removing A.3.1.3.5	JC 13.2 TG 20-02 (Definition of Hybrids vs ICs) & DLA Land and Maritime	The device described in this definition does not exist in MIL-PRF-38535 and should not be confused with Multichip module that pertain to MIL-PRF-38535.

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29	6.4.31	Remove the language ceramic from the definition. From: “...<u>Class Y</u>. A microcircuit employing a ceramic non-hermetic package,...” To: “...<u>Class Y</u>. A microcircuit employing a non-hermetic package...”	JC13.7 Organic Class Y TG 2018-12	Implications for Organic Class Y technology Removing ceramic package limitation for considering all things non-hermetic
30	6.4.35	Add new definition for Class P Device 6.4.35 Class P. A non-hermetic Plastic Encapsulated Microcircuit (PEM), which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections, and all applicable requirements of Appendix B herein. This product must be assessed by the user to determine if it is appropriate for use in users' system application. Due to new addition, renumber sections 6.4.35 - 6.4.49 and all references to these section through out the specification.	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	Class P is new PEM Class being proposed for space application.
31	6.4.40	Update definition From: <u>Class level S</u>. Class level S requirements contained in this document define the requirements for class V, class Y (class level S) (Space level product), including SMDs and M38510 JAN slash sheet product. Class level S is the highest reliability level provided for in this specification, it is intended for space applications. To: <u>Class level S</u>. Class level S requirements contained in this document define the requirements for class V, class Y, and class P (class level S) (Space level product), including SMDs and M38510 JAN slash sheet product. Class level S is the highest reliability level provided for in this specification, it is intended for space applications.	DLA Land and Maritime	Update to add class P to the list of class level S devices

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32	6.4.41	Update definition From: <u>Class level vs Class</u>. This specification defines the requirements for two class levels of product, class level S and class level B. Each class level is made up of multiple classes of product, class level S contains the requirements for classes V and Y product, and class level B contains the requirements for class Q product. To: <u>Class level vs Class</u>. This specification defines the requirements for two class levels of product, class level S and class level B. Each class level is made up of multiple classes of product, class level S contains the requirements for classes V, Y and P product, and class level B contains the requirements for class Q and Class B product.	DLA Land and Maritime	Update to add class P to the list of class level S devices Update to include class B product for class level B product.
33	6.4.49	Update definition From: "6.4.49 <u>Package integrity demonstration test plan (PIDTP)</u>. The package integrity demonstration test plan defines to address the manufacturability, test, quality and reliability issues associated with unique to specific non-traditional assembly/package techniques." To: "6.4.49 <u>Package integrity demonstration test plan (PIDTP)</u>. The package integrity demonstration test plan defines to address the manufacturability, test, quality and reliability issues associated with unique to specific assembly/package techniques as defined in Appendices B and H."	JC13.7 Organic Class Y TG 2018-12	Editorial: Remove the language non traditional and add language " as defined in Appendices B and H
34	6.4.51	Add new definition for Glass Transition Temperature (Tg) 6.4.51 <u>Glass transition temperature</u>. The glass transition temperature is the temperature which an amorphous solid becomes soft upon heating or brittle upon cooling.	DLA Land and Maritime	Editorial

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35	A.2.3 A.4.8.1.1.9 A.4.8.1.2.e A.4.8.1.2.5	Z540.3 Withdrawn - Superseded by ISO/IEC 17025 International Organization for Standardization (ISO) ISO/IEC 17025 - General requirements for the competence of testing and calibration laboratories (Copies of these documents are available online at https://www.iso.org or from ISO Central Secretariat, Chemin de Blandonnet 8, CP 401, 1214 Vernier, Geneva, Switzerland.)	DLA Land and Maritime	Withdrawn as an active standard (October 2020) and superseded by ISO/IEC 17025:2017
36	A.3.2.1	Update last sentence of A.3.2.1. From: “...The manufacturer's electrical test specification shall be documented in a device specification table I format, or equivalent, that is clear to the user and shall be available to the user upon request.” To: “...The manufacturer's electrical test specification shall be documented in a SMD device specification table I format, or equivalent, that is clear to the user and shall be available to the user upon request.”	DLA Land and Maritime	Added the word SMD to clarify Table I is referencing Table I of the SMD device specification.
37	TABLE A-IA	Add title to existing table. TABLE A-IA. Internal <u>lead wires K value</u> .	DLA Land and Maritime	Editorial Table title missing
38	A.3.5.6.3	Update section to include new lead free allowance language From: “...Tin shall be alloyed with a minimum of 3 percent lead by weight. The lead finish designator (see A.3.6.2.7) shall apply to the finish of the leads or terminals....” To: “... Tin shall be alloyed with a minimum of 3 percent lead by weight. However, the use of lead-free solder bumps internal to the device with underfill or encapsulation and mitigated per H.3.4.4.1.2.1 are allowed. Lead-free solder bumps shall have a control plan documented in the PIDTP for QA approval. The lead finish designator (see A.3.6.2.7) shall apply to the finish of the leads or terminals....”	JC-13.7 lead free TG 2018-02	Allow the use of lead-free solder bumps used internal to device with underfill or encapsulation and mitigated per SAE 6537

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39	TABLE A-III	Update to Gold Plating Omit the requirement that only Cobalt shall be used as a hardener. Add a footnote to table A-III to reference MIL-DTL-45204 for electro deposited gold plating applications Update coating "composition requirements column" for gold plate coatings From: Shall contain a minimum of 99.7 percent gold. Only cobalt shall be used as the hardener. To: Shall contain a minimum of 99.7 percent gold. <u>6/</u> Add new footnote <u>6/</u> Electrodeposited gold plating purity, hardness, and alloy materials shall be in accordance with MIL-DTL-45204, Type III, Grade A.	DLA Land and Maritime	MIL-DTL-45204 is a military specification for electrodeposited gold plating. - Type III requires 99.9 percent gold minimum and Grade A represents a Knoop hardness of 90 maximum.
40	A.4.7.1 A.4.8.1.2 A.4.8.1.2.b. A.4.8.1.2.g A.4.8.1.2.h A.4.8.1.2.l.(3)(b)	Update data retention items pertaining to lot identification, traceability, screening, qualification, and quality conformance inspections From: 5 years To: 10 years	DLA Land and Maritime	DLA conducted an Engineering Practice Study and are requesting an increased time for record retention to address concerns over spec requirements vs program requirements.

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41	B.3.10	Update definition From: B.3.10 <u>Package integrity demonstration test plan (PIDTP)</u> . Manufacturability, test, quality and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan are: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, and c) solder terminations. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1). To: "B.3.10 <u>Package integrity demonstration test plan (PIDTP)</u>. Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1)."	JC13.7 Organic Class Y TG 2018-12	Remove the language non traditional and add passive components to the list of microcircuit construction technologies requiring a PIDTP.
42	B.3.13	Update verbiage From: "B.3.13 <u>Moisture sensitivity level (MSL)</u>. Non-hermetic devices such as class Y can exhibit sensitivity to moisture-induced stress and must..." To: "B.3.13 <u>Moisture sensitivity level (MSL)</u>. Non-hermetic devices can exhibit sensitivity to moisture-induced stress and must..."	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	All non-hermetic devices will need testing to determine MSL level.
43	B.4.2	Update title From: "B.4.2 <u>Screening for solder termination microcircuits of class V and class Y.</u>" To: "B.4.2 <u>Screening for solder termination microcircuits of class V, class P and class Y.</u>"	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	Include class P along with class V and Y.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
44	B.4.3	Update title From: B.4.3 <u>Technology conformance inspection (TCI) for class V and class Y.</u> To: "B.4.3 <u>Technology conformance inspection (TCI) for class V, class P and class Y.</u> "	JC 13.2 TG 2020-01 (PEMs for space) & DLA Land and Maritime	Include class P along with class V and Y.
45	Table C-I	Update title of Table and include new TCI/QCI test columns in table for class N and class P. From: TABLE C-I. <u>Group E (RHA) TCI/QCI test for class Q, class V and class Y.</u> To: TABLE C-I. <u>Group E (RHA) TCI/QCI test for class Q, class V, class Y, class N and Class P.</u>	DLA Land and Maritime	Added <u>Group E (RHA) TCI/QCI test</u> for Non hermetic Classes N and P
46	H.2.3	Add non-government publication. SAE ARP6537 - Risk Mitigation for Pb-free Solders Used Internally to Parts	DLA Land and Maritime	Editorial
47	H.2.3	Add non-government publication. EIA/IPC/JEDEC JOINT STANDARD publication EIA/IPC/JEDEC J-STD-002 - Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires	DLA Land and Maritime	Editorial

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48	H.2.3	Add non-government publication. ASTM E1640 - Standard Test Method for Assignment of the Glass Transition Temperature by Dynamic Mechanical Analysis. ASTM E-1356 - Standard Test Method for Assignment of the Glass Transition Temperatures by Differential Scanning Calorimetry ASTM D7028 - Standard for Glass Transition Temperature (DMA Tg) of Polymer Matrix Composites by Dynamic Mechanical Analysis (DMA) ASTM E1545 - Standard Test Method for Assignment of the Glass Transition Temperature by Thermomechanical Analysis was also mentioned.	DLA Land and Maritime	Editorial
49	H.3.2.2.3.2.1	Add new certification criteria H.3.2.2.3.2.1 <u>Epoxy and molding compound materials</u>. Plastic encapsulated microcircuit (PEM) device manufacturers shall document characteristics of epoxy and molding compound materials to their QM plan for QA review and approval. Robust molding compound materials are required to meet higher operating temperature, quality, and reliability issues. For selection of epoxy and molding compound materials the following properties shall be tested in accordance with TM 5011 of MIL-STD-883 during initial qualification of PEM devices: a) Glass transition temperature (Tg) b) Coefficient of thermal expansion (CTE) ppm/C above or below glass transition temperature Tg.	DLA Land and Maritime	Criteria added for determining glass transition temperature (Tg) and coefficient of thermal expansion (CTE) to address reliability concerns.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
50	H.3.2.2.3.2.2	Add new certification criteria H.3.2.2.3.2.2 <u>Glass transition temperature</u>. Glass transition temperature is a first order effect on package robustness specifically modulus and coefficient of thermal expansion (CTE). Knowing the glass transition temperature (Tg) of the molding compound or epoxy of plastic encapsulated microcircuit (PEM) is required for defining package operating temperature. The glass transition temperature (Tg) test method selection should be based on molding compound and may be used by the vendor/suppliers option but test method needs to remain the same for subsequent test i.e. ASTM E-1356: Differential Scanning Calorimetry is a quicker test method. Manufacturers shall document the suppliers performed test data i.e. Certificate of Compliance (CofC) includes glass transition temperature (Tg), CTE, mold compound type and shelf life for QA review and approval and shall be included in the manufacturers QM plan.	DLA Land and Maritime	Criteria added for determining glass transition temperature (Tg) and coefficient of thermal expansion (CTE) to address reliability concerns.
51	H.3.4.4.1	Update definition From: H.3.4.4.1 <u>Package integrity demonstration test plan (PIDTP)</u> . Manufacturability, test, quality and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications shall be addressed in a Package Integrity Demonstration Test Plan at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan are: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, and c) solder terminations. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP.. To: "H.3.4.4.1 <u>Package integrity demonstration test plan (PIDTP)</u>. Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications shall be addressed in a Package Integrity Demonstration Test Plan at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP."	JC13.7 Organic Class Y TG 2018-12	Remove the language non traditional and add passive components to the list of microcircuit construction technologies requiring a PIDTP

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
52	H.3.4.4.1.2 1) Substrate materials.	Update From: "1) <u>Substrate materials</u>. The substrate materials shall be documented in the PIDTP, and shall include landing pad composition." To: 1) <u>Substrate materials</u>. The substrate materials shall be documented in the PIDTP, and shall include the following properties and characterizations: i) Substrate core and build-up layer materials ii) Conductor material and composition iii) Landing pad construction and composition iv) Solder mask material and thickness v) Coefficient of thermal expansion (CTE) vi) Glass transition temperature (Tg) if appropriate vii) Moisture absorption and outgassing characterization (MSL level characterization) viii) Radiation exposure effects on materials (part of product qualification)	JC13.7 Organic Class Y TG 2018-12	Evaluation items regarding the substrate materials to be included in the PIDTP
53	H.3.4.4.1.2 2) Bump geometry and quality.	Update From: "2) <u>Bump geometry</u>. The solder bump geometry shall be documented in the PIDTP, and shall include bump height, bump diameter and bump pitch, as well as a description of the under bump metallurgy (UBM) shape, size and thickness." To: "2) <u>Bump geometry and quality</u>. The solder bump geometry and wafer level inspections shall be documented in the PIDTP, and shall include the following items: i) Bump height ii) Bump diameter iii) Minimum bump pitch iv) Under bump metallurgy (UBM) construct v) UBM shape and size vi) Bump yield vii) Bump shear	JC-13.2 flip chip TG 2018-01	Combine bump geometry with additional bump quality evaluation criteria. Items listed should be documented as a part of the PIDTP

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
54	H.3.4.4.1.2 3) Solder bump deposition process and materials.	Update From: "3) <u>Solder bump deposition process and materials</u>. The solder bump deposition process shall be documented in the PIDTP (e.g., plated, evaporation, solder paste), along with the solder alloy. In addition, the UBM deposition process (e.g., plated, evaporation, sputtered) and composition shall be documented in the PIDTP." To: "3) <u>Solder bump construction process and materials</u>. The solder bump construction process shall be documented in the PIDTP (e.g., plated, evaporation, solder paste, ball drop), along with the bump material composition (e.g., alloy). In addition, the Under Bump Metallization (UBM) deposition process (e.g., plated, evaporation, sputtered) and composition shall be documented in the PIDTP. "	JC-13.2 flip chip TG 2018-01	Editorial clarification
55	H.3.4.4.1.2 4) Flux materials..	Update From: "4) <u>Flux materials</u>. The flux type (e.g., no-clean, water soluble) and materials employed for solder bump interconnect reflow shall be documented in the PIDTP." To: "4) <u>Flux materials</u>. If flux is used during flip chip assembly, the flux type (e.g., no-clean, water soluble) and materials employed for solder bump interconnect reflow shall be documented in the PIDTP."	JC-13.2 flip chip TG 2018-01	Editorial clarification

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
56	H.3.4.4.1.2. 5) Underfill materials	Update From: "5) <u>Underfill materials</u>. Underfill materials shall be documented in the package integrity demonstration test plan (PIDTP). The PIDTP shall address the relevant properties of the underfill and how they are characterized. The properties below shall be included to the PIDTP: i) Coefficient of thermal expansion (CTE) ii) Glass transition temperature (Tg) iii) Viscosity iv) Pot life v) The shelf life vi) Underfill particle size/Filler contents vii) Underfill cure time and temperatures viii) Bond strength ix) Ionic impurities x) Underfill Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM." To: "5) <u>Underfill materials</u>. Underfill materials shall be documented in the package integrity demonstration test plan (PIDTP) and shall include the following properties and characterizations, as well as those in accordance with MIL-STD-883 Test Method 5011: i) Coefficient of thermal expansion (CTE) ii) Glass transition temperature (Tg) iii) Thermal conductivity iv) Underfill Outgassing test: For non-hermetic flip chip devices (e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM."	JC13.7 Organic Class Y TG 2018-12	Items explicitly listed in this section are those important to the user relative to understanding impact on reliability and thermal performance Items removed from this section will be covered in TM5011 Table I for Adhesives.
57	H.3.4.4.1.2. 5.1) Underfill Quality	Insert new section 5.1) <u>Underfill Quality</u>: Manufacturer shall perform stress tests to evaluate the underfill material and process for complete fill and strength. i) Die shear or die pull-off strength performed during PIDTP for one-time evaluation. ii) Voiding iii) Incomplete fill iv) Excess underfill material control	JC-13.2 flip chip TG 2018-01	List evaluation items regarding the Underfill quality to be included in the PIDTP.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
58	H.3.4.4.1.2 5.2) Underfill long term reliability test	Update: From: “ <u>Underfill long term reliability test</u>: Manufacture’s shall perform following long term underfill reliability test (1) Temperature cycling test: Cured underfill with solder bump temperature cycling test shall be performed for 1,000 cycles in accordance with TM1010 condition C (-65 to 150°C) and subsequently (2) SAM test shall be performed to verify underfill void and delamination. The sample size 10(0) shall be considered as minimum during underfill package initial qualification.” To: “ <u>Underfill long term reliability test</u>: Manufacture’s shall perform the following long term underfill reliability test. i) Temperature cycling test: Cured underfill with solder bump temperature cycling test shall be performed for 1,000 cycles in accordance with TM1010 condition C (-65 to 150°C) or condition B depending on package capability. For cases with glass transition temperature(Tg) below 125°C the upper temperature may be set at underfill glass transition temperature. a) Post temp cycle Acoustic Microscopy test shall be performed to verify underfill void and delamination. The sample size 10(0) shall be considered as minimum during underfill package initial qualification. b) Additional destructive evaluation may be required depending on acoustic microscopy results.	JC-13.2 flip chip TG 2018-01	List evaluation items regarding the Underfill long term reliability to be included in the PIDTP

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
59	H.3.4.4.1.2 6) Thermal interface materials (TIM) ...	Update: From: "6) <u>Thermal interface materials (TIM) for Lid attach/adhesive materials.</u> Devices with lid or heat spreader attached to the back side of a microcircuit die, the lid attach/adhesive thermal interface materials shall be documented in the PIDTP. The following test parametric results may be considered with C of C or initial certification test performed by TIM suppliers/users; and approved by QA: a) Viscosity. b) Density c) Volume resistivity d) Lap shear adhesion e) Expiration Date f) Pot life g) Glass transition temperature (Tg) h) Dissipation factor i) Ionic impurities j) Coefficient of thermal expansion (CTE) k) Thermal conductivity l) Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. TIM outgassed limits shall be <1% for total mass loss and <0.1% for CVCM. To: "6) <u>Thermal interface materials (TIM) for Lid attach/adhesive materials.</u> Devices with lid or heat spreader attached to the back side of a microcircuit die, the lid attach/adhesive thermal interface materials shall be documented in the PIDTP and include the following properties and characterizations, as well as those in accordance with MIL-STD-883 Test Method 5011" a) Glass transition temperature (Tg) b) Coefficient of thermal expansion (CTE) c) Thermal conductivity d) Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. TIM outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.	JC13.7 Organic Class Y TG 2018-12	Items explicitly listed in this section are those important to the user relative to understanding impact on reliability and thermal performance Items removed from this section will be covered in TM5011 Table I for Adhesives.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
60	H.3.4.4.1.2 7) Flip chip bump shear test ...	Update: From: <u>"Flip chip bump shear test.</u> For flip chip, a bump shear test shall be performed in accordance with JEDEC JESD22-B117 or equivalent to determine the shear strength of the solder bumps for initial qualification as a part of the wafer bump technology qualification and shall be documented to the PIDTP." To: <u>" Flip chip bump shear test.</u> For flip chip, a bump shear test shall be performed on bumped wafers in accordance with JEDEC JESD22-B117 or equivalent (e.g. method 2019, 2031) to determine the shear strength of the individual solder bumps for initial qualification. The test method does not define the pass/fail criteria for small bumps used in flip-chip. Data analysis should be done to evaluate the process variability. The evaluation process shall be documented in the PIDTP. Die shear tests 2011, 2019, or 2031 are not useful as the mechanical strength of the flip-chip assembly will either exceed the tool capability or the die will be destroyed and not provide meaningful information."	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.
61	H.3.4.4.1.2.1 <u>Pb free bump qualification for Flip-chip devices</u>	Insert new section H.3.4.4.1.2.1 <u>Pb free bump qualification for Flip-chip devices</u> : For microcircuit devices containing Pb-free solder bumps with Underfill/Encapsulation, the materials and processes unique to Pb-free solder bump alloy and underfill composition shall be documented in the PIDTP for QA approval. Manufacturer processes and materials shall be qualified by addressing, as a minimum, the test in table H-I for Pb free bump initial qualification and risk mitigation:	JC13.7 Lead free TG 2018-02 DLA Land and Maritime	Allow the use of lead-free solder bumps used internal to device with underfill or encapsulation and mitigated per SAE 6537
62	TABLE H-I.	Insert new table TABLE H-I. <u>Assembly process technology testing for flip chip packages containing Pb free bump</u> .	JC13.7 Lead free TG 2018-02 DLA Land and Maritime	Qualification TABLE H-I. added for assembly process technology testing per mitigations in accordance with SAE 6537

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
63	H.3.4.4.1.3. Solder terminations	Update: From: "For space use microcircuits employing solder terminations (class V or class Y), the PIDTP shall address the materials..." To: "For space use microcircuits employing solder terminations (e.g ball grid array or column grid array), the PIDTP shall address the materials..."	JC13.7 Organic Class Y TG 2018-12	Editorial clarification.
64	TABLE H-IA TABLE H-IB TABLE H-IIA TABLE H-IIB	Update titles of tables: From: - TABLE H-IA. <u>Assembly process technology testing for hermetic and non-hermetic packages</u> - TABLE H-IB. <u>Assembly process technology testing for plastic packages</u> - TABLE H-IIA. <u>Technology characterization testing for hermetic and non-hermetic packages</u> - TABLE H-IIB. <u>Technology characterization testing for plastic packages</u> To: - TABLE H-IA. <u>Assembly process technology testing for hermetic (classes Q, V) and non-hermetic packages (class Y)</u> - TABLE H-IB. <u>Assembly process technology testing for plastic packages (classes N, P)</u> - TABLE H-IIA. <u>Technology characterization testing for hermetic (classes Q, V) and non-hermetic packages (class Y)</u> - TABLE H-IIB. <u>Technology characterization testing for plastic packages (classes N, P)</u>	DLA Land and Maritime	Clarify which device classes are applicable for each table.
65	Table H-IA Group 1	Update: From: a. Thermal shock TM1011 condition C, 100 cycles To: a. Thermal shock TM1011 condition C, 100 cycles (Ceramic class Y only)	13.2 Manufacturer Comment	thermal shock test not applicable for QML-Y organic substrates.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
66	Table H-IA Group 1	Update item c. for both hermetic and non hermetic package columns From: "SAM" To : "Acoustic Microscopy"	JC-13.2 flip chip TG 2018-01	Editorial
67	Table H-IA Group 1	Add footnotes <u>2/</u> and <u>3/</u> to item d. for both hermetic and non hermetic package columns d. Bond strength TM 2011 (die-mount and wire bond) plus Die cracks TM 2010 <u>2/ 3/</u>	JC-13.2 flip chip TG 2018-01	Flip chip does not have wire bonds. Flip chip die pull-off or shear testing does not provide useful information.
68	Table H-IA Group 1	Add footnotes <u>3/</u> to item e. for both hermetic and non hermetic package columns . e. Die shear or stud pull TM 2019 or TM 2027 <u>3/</u>	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
69	Table H-IA Group 1	Remove items f. and h. from both hermetic and non-hermetic package columns f. Flip chip die pull off test TM 2031 (before underfill dispense) h. Flip chip die shear test TM 2019 or TM 2027 (after underfill cured)	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.
70	Table H-IA Group 2	Add footnotes <u>4/</u> to constant acceleration test. for both hermetic and non hermetic package columns c. Constant acceleration TM 2001 <u>4/</u>	JC-13.2 flip chip TG 2018-01	Constant acceleration is not applicable for flip chip.
71	Table H-IA Footnotes <u>2/</u>	Add New footnote <u>2/</u> Flip chip does not have wire bonds. Wire pull testing does not apply.	JC-13.2 flip chip TG 2018-01	Not applicable to flip chip
72	Table H-IA Footnote <u>3/</u>	Add New footnote <u>3/</u> Flip chip die pull-off or shear testing does not provide useful information. The required force either exceeds the tool capability or results in extreme damage to the die. Bump adhesion quality can be inferred using the electrical test, radiography, and/or acoustic microscopy.	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
73	Table H-IA Footnote <u>4</u> /	Add New footnote <u>4</u> / Constant Acceleration (Centrifuge) is not applicable for flip chip. No wires in the package that can move and create shorts.	JC-13.2 flip chip TG 2018-01	Constant acceleration is not applicable for flip chip.
74	Table H-IA Footnote <u>5</u> /	Add New footnote <u>5</u> / to group 7, Solderability TM 2003 for non-hermetic packages. <u>5</u> / Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002.	13.2 Manufacturer Comment	J-STD-002 allows preconditioning dry back vs steam aging for non-hermetic packages.
75	Table H-IB Group #1	Apply new footnotes <u>2</u> / and <u>3</u> / b. In-line bond strength <u>2</u> / c. In-line ball bond shear <u>2</u> / d. In-line die shear/stud pull <u>3</u> / <u>2</u> / Flip chip does not have wire bonds. Wire pull testing does not apply. <u>3</u> / Flip chip die pull-off or shear testing does not provide useful information. The required force either exceeds the tool capability or results in extreme damage to the die. Bump adhesion quality can be inferred using the electrical test, radiography, and/or acoustic microscopy.	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.
76	Table H-IB Group #2	Update Group #2, From: "SAM" To : "Acoustic Microscopy"	JC-13.2 flip chip TG 2018-01	Editorial
77	Table H-IB Group #3	Update add new footnote <u>4</u> / From: "a. TM 1010 condition C or JESD22-A104" To: "a. TM 1010 condition C or JESD22-A104 <u>4</u> /" <u>4</u> / Package materials with limited high and low temperature range may apply an alternate test condition and shall be specified in the manufacturer's QM plan.	JC-13.2 flip chip TG 2018-01	Alternate condition may apply for package material unable to meet the extreme temperatures of the test conditions listed in the table.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
78	Table H-IB Group #4	Remove group #4 Thermal shock test.	JC-13.2 PEMs TG 2020-01	Not applicable for epoxy molded / Plastic encapsulated packages"
79	Table H-IB Group #6	Update add new footnote <u>4/</u> From: "TM 1008, 1,000 hours at +150°C" To: "TM 1008, 1,000 hours at +150°C <u>4/</u> " <u>4/</u> Package materials with limited high and low temperature range may apply an alternate test condition and shall be specified in the manufacturer's QM plan.	JC-13.2 flip chip TG 2018-01	Alternate condition may apply for package material unable to meet the extreme temperatures of the test conditions listed in the table.
80	Table H-IB Footnotes <u>2/</u>	Add New footnote <u>2/</u> Flip chip does not have wire bonds. Wire pull testing does not apply.	JC-13.2 flip chip TG 2018-01	Not applicable to flip chip packages.
81	Table H- IB Footnote <u>3/</u>	Add New footnote <u>3/</u> Flip chip die pull-off or shear testing does not provide useful information. The required force either exceeds the tool capability or results in extreme damage to the die. Bump adhesion quality can be inferred using the electrical test, radiography, and/or acoustic microscopy.	JC-13.2 flip chip TG 2018-01	For flip chip devices, die shear or pull of strength tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die.
82	Table H-IB Footnote <u>4/</u>	Add New footnote <u>4/</u> Package materials with limited high and low temperature range may apply an alternate test condition and shall be specified in the manufacturer's QM plan.	JC-13.2 flip chip TG 2018-01	Alternate condition may apply for package material unable to meet the extreme temperatures of the test conditions listed in the table.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
83	Table H-IB Footnote <u>5</u> /	Add New footnote <u>5</u> / to group 7, Solderability TM 2003. <u>5</u> / Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002.	13.2 Manufacturer Comment	J-STD-002 allows preconditioning dry back vs steam aging.
84	Table H-IIB Group #1B	Add new Group #2, Process Resistance to Moisture Test: MSL per manufacturer's specification	JC-13.2 flip chip TG 2020-01	All non-hermetic devices will need testing to determine MSL level.
85	Table H-IIB Footnote <u>4</u> /	Add New footnote <u>4</u> / to group 5, Susceptibility to leakage and corrosion <u>4</u> / Alternative to Autoclave, unbiased HAST may be performed in accordance with JESD22-A118	13.2 Manufacturer Comment	Alternate test method may apply
86	Table H-IIB Group #6	Update Group #6, From: "SAM" To : "Acoustic Microscopy"	JC-13.2 flip chip TG 2018-01	Editorial