

The following table summarizes changes to MIL-PRF-38535 Revision N.

~~Proposed deletions are in red strikeout.~~

Proposed changes to second draft in green highlight

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
1	3.3.4.1, 3.4, 3.6.2.2, 3.6.7.2, 3.6.8, 6.3, 6.4.38, A.3.2.2, A.3.4.1, A.3.4.2.1, A.3.6.2.8, A.3.6.9.2, B.3.3, G.3.3.1, H.3.1.11, H.3.3.1, H.3.6, FIGURE H-1, FIGURE H-2	Name change to all references throughout From: DLA Land and Maritime To: DLA Weapons Support	DLA Weapons Support	DLA " Land and Maritime has been updated to DLA " Weapons Support".
2	3.4.1.3.3	Add new Alternate Wafer Fabrication Facility Audit Requirement. This change establishes a pathway for the approval of a wafer fabrication facility in lieu of an on-site audit when deemed necessary by DLA-QA. See MIL-PRF-38535 document for details	DLA Weapons Support	This change introduces a flexible alternative that modernizes the approval process.
3	TABLE I.	This proposal introduces new TABLE I, that accompanies Alternate Wafer Fabrication Facility Audit Requirement. In lieu of an onsite audit. See MIL-PRF-38535 document for details	DLA Weapons Support	This alternate method is not a relaxation of standards but a shift in verification methodology. It mandates manufacturer adherence to new procedural testing requirements, as will be defined in Table I

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
4	3.4.2.3	Add new qualification by extension for multichip microcircuits This change provides a standardized, risk-based qualification path for complex Multichip Microcircuits (MCMs) and stacked-die devices, leveraging existing die data. See MIL-PRF-38535 document for details		This approach leverages previously qualified die data, reducing redundant testing while maintaining robust reliability standards through comprehensive engineering analysis and testing.
5	Table IA Screening Tests 4. Temperature cycling	Update Class N and Class P From: TM 1010, condition B, -55 to 125 °C 15 cycles minimum To: TM 1010 or JESD22-A104, condition B, -55 to 125 °C 15 cycles minimum	Manufacturer Comment	Update to align with TABLE H-IB. Assembly process technology testing for plastic packages (classes N, P).
6	3.4.3 C.3.3.1.	Update sections of 3.4.3 and C.3.3.1 From: ..." for device classes B, Q, S, V, Y or T shall be submitted for QA approval. The designator RHA levels are defined below:" To: ..." for device classes B, Q, S, V, N, P, Y or T shall be submitted for QA approval. The designator RHA levels are defined below:"	DLA Weapons Support	Corrects a gap by adding Classes N and P to the RHA section. This ensures that any device class can be qualified for radiation hardness.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
7	3.10	Update section 3.10 solderability From: 3.10 Solderability. All parts shall be capable of passing the solderability test in accordance with TM 2003 of MIL-STD-883, on delivery. To: 3.10 Solderability. All devices shall be capable of passing the solderability requirements in accordance with MIL-STD-883, Test Method 2003. Alternative solderability testing in accordance with IPC/JEDEC J-STD-002 is permitted for organic class Y, N, and P. However, preconditioning of steam aging shall be performed in accordance with MIL-STD-883, Test Method 2003 for all Column Grid Array (CGA) packages and Ball Grid Array (BGA).	DLA Weapons Support, & Manufacturers comments	Bridges the gap for solderability testing between MIL-STD-883, TM2003 and IPC/JEDEC J-STD-002.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
8	3.12 and A.4.8.1.1.14	Update From: <u>ESD control program</u>. ESD protection, control, grounding procedures and training programs are very important key points to mitigate ESD damage at the microcircuits manufacturing and testing process. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all wafer fabrication, wafer bumping, wafer scribing, coring services, automatic handling equipment's, assembly facilities, testing station, packaging and handling of dice and devices in accordance with JESD625 or ANSI/ESDA S20.20. The established ESD control program documentation shall be under document control and TRB shall review and inspect periodically. To: Electrostatic Discharge (ESD) control program. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all stages, including, but not limited to, wafer fabrication, wafer bumping, wafer scribing, coring services, automatic handling equipment, assembly facilities, testing stations, packaging and handling of dice and devices in accordance with JESD625 or ANSI/ESDA S20.20. For wafer fabrication specifically, this ESD program shall utilize Human Body Model (HBM) and Charged Device Model (CDM) techniques by addressing the effects of electrostatic surface charge that can lead to product reticle damages due to electrostatic discharge (ESD), electrostatic attraction (ESA), and electric field-induced migration (EFM). The plan shall incorporate: a. A charge mitigation strategy and specific ESD protection measures in sensitive areas, targeting finished wafers, reticles, and their carriers. b. Assessments to monitor electrostatic discharge risks shall be performed and documented in the quality management plan. c. An ESD audit shall be performed in all ESD Protected Areas (EPAs) within wafer fabrication in accordance with ANSI/ESD S20.20. Any tailoring of the S20.20 standard for wafer production shall be under document control and reviewed by the TRB periodically.	EEE Parts Bulletin recommendation	This update for ESD control program is for preventing ESD damage at the wafer foundry, assembly facility and testing station.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
9	4.3	Update section of 4.3 From: ... "All product shipped shall be capable of passing TCI in accordance with tables II, III, IV, and V; for plastic packages see table IB herein."... To: ... "All product shipped shall be capable of passing TCI in accordance with tables II, III, IV, and V; for existing / legacy class N microcircuits with QML certification successfully completed prior to 01 May 2023, see table IB herein." ...	DLA Weapons Support	This change is for clarification. The requirements of Table IB only applies to legacy class N devices.
10	TABLE IB	Update TABLE IB. footnote <u>3</u>/ From: <u>3</u>/ The requirements of Table IB only apply to existing / legacy class N microcircuits with QML certification successfully completed prior to 01 May 2023, (implementation date of Rev M MIL-PRF-38535). To: <u>3</u>/ The requirements of Table IB only apply to existing / legacy class N microcircuits with QML certification successfully completed prior to 01 May 2023.	DLA Weapons Support	This is an editorial change that removes the explanatory parenthetical text. The date itself is the binding requirement, and the extra context is unnecessary.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
11	TABLE II footnote 8/	Update TABLE II footnote 8/ adding From: 8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003. To: 8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003. Alternative solderability testing in accordance with IPC/JEDEC J-STD-002 is permitted for classes Y, N, and P, subject to the requirements specified in paragraph 3.10.	DLA Weapons Support, & Manufacturers comments	Bridges the gap for solderability testing between MIL-STD-883, TM2003 and IPC/JEDEC J-STD-002.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
11	TABLE IV	Update TABLE IV to apply footnote 2/ to all classes	Manufacturer Comment	This is a corrective action to fix an error from the 2013 harmonization of MIL-STD-883 into this specification. During that update, Footnote 2/ was inadvertently omitted from device classes Q and N; this change applies it correctly to all classes as intended. This proposed change would contradict with paragraph A.4.5.4, DLA will remove the proposed change of including Footnote 2 for Class Q and Class N devices in Table IV. The sampling frequency will remain aligned with the established periodic requirements defined in A.4.5.4.
12	Table V Subgroup 3 b. Temperature cycling	Update Class N and Class P From: ii) TM1010 Condition B (150 cycles min) To: ii) TM1010 or JESD22-A104 Condition B (150 cycles min)	Manufacturer Comment	Update to align temperature cycling test with TABLE H-IB. Assembly process technology testing for plastic packages (classes N, P).

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
13	TABLE V Subgroup 3	Update classes N and P subgroup 3 From: c. JESD22-A118 Unbiased HAST Condition B and/or (JESD22-A110) Biased HAST Condition B <u>18/</u> To: c. JESD22-A118 Unbiased HAST Condition A or B and/or (JESD22-A110) Biased HAST Condition A or B <u>18/</u>	Manufacturer Comment	This change provides manufacturers with flexibility of either Condition A or B for Biased and Unbiased HAST.
14	TABLE V Footnote <u>12/</u>	Internal gas analysis test Update footnote <u>12/</u> From: <u>12/</u> Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity. To: <u>12/</u> Test three devices 3(0); if one fails, test two additional devices with no failures. If two or more devices fail from the initial test sample, the manufacturer may resubmit a minimum of three additional devices to the same or an alternate lab approved by the qualifying activity, with no failures allowed. If all resubmitted samples pass 3(0), the lot shall be accepted for QCI coverage. Identified failures on the IGA report shall be investigated for root cause and the qualifying activity shall be notified.	DLA Weapons Support	Clarifies the IGA resubmission process and sample sizes. QA notification for any identified failure.
15	6.3	Update to include email contact information for information pertaining to qualification products.	DLA Weapons Support	Per MIL-STD-961, it states to (insert name, mailing address, and email of qualifying activity).

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
16	6.3.1	Update to add new section "6.3.1 Provisions governing qualification. Copies of "Provisions Governing Qualification "SD-6" are available online at https://quicksearch.dla.mil/qsSearch.aspx ."	DLA Weapons Support	Provides pointer to the overarching DoD qualification rules and procedures outlined in SD-6.
17	6.4.4 & A.3.1.3.4	Update From: Integrated circuit (microcircuit). Integrated circuit (microcircuit). A die with a high equivalent circuit element density, composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., this excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.) To: Integrated circuit (microcircuit). A die with a high equivalent circuit element density, composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., this excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)	DLA Weapons Support	This editorial change removes duplicated text from the definition.
18	6.4.4.1 & A.3.1.3.4.1	Update From: 6.4.4.1 Multichip microcircuit or multichip module (MCM). An integrated circuit or microcircuit consisting of two or more die which are attached to a substrate or package and meets all applicable requirements of section 3.4. To: 6.4.4.1 Multi-Chip Microcircuit or Multi-Chip Module (MCM). An integrated circuit or microcircuit consisting of two or more die in a single package.	DLA Weapons Support	Simplifies the definition of MCM for clarity and removes reference to section 3.4.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
19	6.4.14 , G.2.3, G.3.3.c, G.3.3.1.i, H.2.3, H.3.2.1.3, J.2.3, J.3.12.a,	Update document reference to new name "SAE EIA-557"	DLA Weapons Support	Update document name change through out .
20	6.4.9, Table IV Group C life test footnote 3/ A.3.1.3.14	Added clarification Delta parameters shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in electrical parametric limit. The specific delta parameters shall be as defined in the applicable device specification.	User and DLA Weapons Support	Added clarification for regarding delta parameters.
21	A.3.1 A.4.8.1.3.8	Remove reference to (DSCC-VQC-42 or equivalent)	DLA Weapons Support	This editorial change corrects an oversight by removing the final two references to the obsolete document DSCC-VQC-42, which was cancelled and intended for full removal in the previous MIL-PRF-38535 Revision L.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
22	A.3.4.1.2	Update Process monitor programs. From: A.3.4.1.2 <u>Process monitor programs</u>. Process monitor programs performed by the manufacturer shall be established as a minimum for the following processes: Scanning Electron Microscope (SEM), wire bonding, die attachment, lid seal, particle detection, lead trimming, and final lead finish thickness. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lot(s). With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors and procedures shall be maintained and available for review. To: A.3.4.1.2 <u>Process monitor programs</u>. Process monitor programs performed by the manufacturer shall be established as a minimum for the following processes: Scanning Electron Microscope (SEM), wire bonding, die attachment, lid seal, internal gas analysis (IGA), particle detection, lead trimming, and final lead finish thickness. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lot(s). With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors and procedures shall be maintained and available for review.	DLA Weapons Support	This change elevates Internal Gas Analysis (IGA) to a formal process monitor program.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
23	A.3.4.1.2.7	Add internal gas analysis program monitor requirement. A.3.4.1.2.7 <u>Internal Gas Analysis</u>. Manufacturer(s) shall monitor and control internal moisture and gas content in cavity-type packages using in-situ moisture monitors for IGA per MIL-PRF-883, Test method 1018 at +100 °C. a. Each package ~~type~~ family shall be monitored using sample units per assembly lot, as defined by the manufacturer(s) and approved by the TRB. Sample units shall be structurally identical with respect to package ~~type~~ family, sealing method, processes and materials to ensure that hermeticity test results from ~~one-device~~ samples are representative of the lot grouping. b. Moisture shall not exceed 5,000 ppmv. Monitoring program shall establish a statistical process average with control limits. Exceeding control limits shall require corrective action , including root cause analysis, containment, and potential revision of sampling frequency or grouping. c. Manufacturers shall document and track He, H₂, O₂, Ar, CO₂, fluorocarbons, bombing gases and moisture levels for all IGA monitors. d. Devices shall be marked or otherwise traceable (i.e. QCI or engineering sample) before being sent to the laboratory for testing. e. Samples that exceed IGA control limits (established by the manufacturer) shall be investigated for root cause (i.e., sealer, materials, processes...etc.) and corrective action shall be executed, if appropriate. ~~Note: Package type grouping is critical to ensure test data correlation and avoid variability caused by differences in package case outline configuration, internal geometry, or sealing material characteristics.~~	DLA Weapons Support	This new addition of IGA process monitoring will support improving hermeticity concerns.
24	Table A-1	Add to major change table y. Epoxy and molding compound materials Notify qualifying activity and document in QM plan/PIDTP (MIL-STD-883 TM 5011)	DLA Weapons Support	Clarification

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
25	A.3.5.5.2	Update From: A.3.5.5.2 <u>Internal wire size and material</u>. For class level S microcircuits, the internal wire diameter shall be 0.001 inch minimum (0.0254 mm) or of sufficient diameter to meet the minimum fusing requirements and bond pull strength requirements with the approval of qualifying activity. The internal lead wire shall be the same metal as the die metallization. To: A.3.5.5.2 <u>Internal wire size and material</u>. For class level S microcircuits, the internal wire diameter shall be 0.001 inch minimum (0.0254 mm) or of sufficient diameter to meet the minimum fusing requirements and bond pull strength requirements with the approval of qualifying activity. The internal lead wire shall be the same metal as the die metallization. ~~However, Class P device may allow gold internal lead wire to aluminum bond pads on a case-by-case basis and documented in the Standard Microcircuit Drawing (SMD).~~ However, for Class V Multi-Chip Microcircuit (MCM) and Class P (PEM) devices, a bi-metallic interface (e.g., gold-aluminum) for internal wire bonding may be permitted on a case-by-case basis, provided it is in accordance with A.3.5.5.2.1 and is documented in the Standard Microcircuit Drawing (SMD).	Manufacturer Comment	~~The manufacturers have issues applying monometallic lead wire in non-hermetic class P devices. This change introduces a flexible alternative of gold-to-aluminum wire bonds for Class P devices on a case-by-case basis.~~ Manufacturers have issues applying monometallic lead wire in Class V MCMs or class P devices. This change introduces a qualification pathway bi-metallic interface (e.g., gold-to-aluminum) wire bonds only applicable to class V MCMs or Class P devices on a case-by-case basis
26	A.3.5.5.2.1	Add new requirements section A.3.5.5.2.1 <u>Bi-Metallic wire bond qualification</u> ~~for class V (class level S) devices. For class level S microcircuits, the internal lead wire shall be the same metal as the die metallization. However, if a manufacturer uses a bi-metallic interface (e.g. gold-aluminum) for internal wire bonding, it shall be evaluated on a case-by-case basis. Prior to wire bonding, When a bi-metallic interface is utilized in accordance with A.3.5.5.2,~~ the die surface shall undergo plasma cleaning in air or inert atmosphere to remove contaminants and oxides. This process shall be documented in the QM plan and approved by the QA. Manufacturers shall perform the qualification test in TABLE A-IB for risk mitigation to assess intermetallic compound (IMC) growth, bond integrity, and to ensure mechanical reliability.	JEDEC JC 13.2 TG 25-02	The manufacturers have issues applying monometallic lead wire in class V MCM advanced packages or class P devices. This change introduces a qualification pathway bi-metallic interface (e.g., gold-to-aluminum) wire bonds only applicable to class V MCMs or Class P devices on a case-by-case basis.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
27	TABLE A-IB	Add new requirements TABLE TABLE A-IB. <u>Bi-Metallic wire bond qualification for class V (class level S) devices.</u> See MIL-PRF-38535 document for details Add: 1/ TABLE A-IB is restricted to only Class V MCM devices or Class P (PEM) devices when a bi-metallic interface is utilized in accordance with A.3.5.5.2		Additional test on bi-metallic wire bond will provide detailed qualification and lot acceptance test plan for validation in class V (MCM devices) or Class P.
28	TABLE A-III	Update TABLE A-III for coating of Gold flash palladium Adding language in the coating composition requirements column: For lead finishes utilizing a nickel base palladium with a gold flash (e.g., NiPdAu, NiPdAuAg), the total thickness of the multi-layer finish stack shall be a minimum of 20 microinch.	Manufacturer Comment	The previous language was ambiguous as to how the minimum thickness should be measured. This change clarifies that the requirement applies to the total combined thickness of all layers in the finish stack (e.g., Ni+Pd+Au).
29	B.3.10	Update From: B.3.10 <u>Package integrity demonstration test plan (PIDTP)</u> . Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1)." To: "B.3.10 <u>Package integrity demonstration test plan (PIDTP)</u> . Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., classes Y and P), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1).	DLA Weapons Support	Clarification update that includes Class P to the examples of non-hermetic packages requiring a PIDTP.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
30	B.4.2	Update From: B.4.2.1 Ball grid array (BGA) microcircuits . For BGA microcircuits post-assembly screening burn-in test may be performed before the solder balls have been attached to the package. Electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package. To: B.4.2.1 <u>Ball grid array (BGA) microcircuits</u> . For BGA microcircuits post-assembly screening <u>(including electrical test and burn-in)</u> test may be performed before the solder balls have been attached to the package. Electrical test shall be performed across the full military temperature range ~~after~~ <u>before</u> attachment of the solder balls on the package. <u>After ball attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the ball attach process, and visual inspection shall be performed according to TM 2009 of MIL-STD-883.</u>	DLA Weapons Support, & Manufacturers comments	This change permits BGA manufacturer the option to test BGAs, either in LGA or BGA format. Similar to Column grid array microcircuits.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
31	H.3.2.2.3.2.2	Update From: H.3.2.2.3.2.2 <u>Glass transition temperature</u>. Glass transition temperature is a first order effect on package robustness specifically modulus and coefficient of thermal expansion (CTE). Knowing the glass transition temperature (Tg) of the molding compound or epoxy of plastic encapsulated microcircuit (PEM) is required for defining package operating temperature. The glass transition temperature (Tg) test method selection should be based on molding compound and may be used by the vendor/suppliers option but test method needs to remain the same for subsequent test i.e. ASTM E-1356: Differential Scanning Calorimetry is a quicker test method. Manufacturers shall document the suppliers performed test data i.e. Certificate of Compliance (CofC) includes glass transition temperature (Tg), CTE, mold compound type and shelf life for QA review and approval and shall be included in the manufacturers QM plan. To: H.3.2.2.3.2.2 <u>Glass transition temperature</u>. Glass transition temperature is a first order effect on package robustness specifically modulus and coefficient of thermal expansion (CTE). Knowing the glass transition temperature (Tg) of the molding compound or epoxy of plastic encapsulated microcircuit (PEM) is required for defining package operating temperature. The glass transition temperature (Tg) test method selection should be based on molding compound and may be used by the vendor/suppliers option but test method needs to remain the same for subsequent test i.e. ASTM E-1356: Differential Scanning Calorimetry is a quicker test method. Manufacturers shall document the suppliers performed test data i.e. material certificate of conformance-includes glass transition temperature (Tg), CTE, mold compound type and shelf life for QA review and approval and shall be included in the manufacturers QM plan.	DLA Weapons Support	This is a clarification to specify that the required material data (e.g., Tg, CTE) is provided via the raw polymeric materials certificate of conformance, not the Certificate of Compliance (CofC) for the final device.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
32	H.3.4.4.1.1	Update From: H.3.4.4.1.1 <u>Non-Hermetic packages</u>. For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Moisture sensitivity level characterization (ref: IPC/JEDEC J-STD-020D) shall be performed for exposed flip-chip underfill or thermal grease/epoxy. To: H.3.4.4.1.1 <u>Non-Hermetic packages</u>. For class Y and class P microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Moisture sensitivity level characterization (ref: IPC/JEDEC J-STD-020) shall be performed for all ~~exposed organic materials of~~ non-hermetic packages ~~(i.e. epoxy, underfill, etc).~~	proposed from JEDEC TG2020-01	Addition of Class P to the PIDTP scope to cover all exposed organic materials. Also updates an editorial correction to remove the revision letter from the J-STD-020 document reference.
33	TABLE H-I	Update Biased Humidity test To add option for Temperature Humidity Biased(THB) and add option for test condition 85°C/85% relative humidity, 1000 hours JESD22-A101(THB) or JESD22-A110 (Biased HAST) 130°C/85% relative humidity, for 96 hours Or 110°C/85% relative humidity, for 264 hours Or 85°C/85% relative humidity, 1000 hours	Manufacturer Comment	Update option for JESD22-A101(THB) and 85°C/85% relative humidity, 1000 hours For Pb-Free wafer bump of flip chip device qualification.
34	TABLE H-I	Update Thermal Shock test Add new footnote 4/ 4/ Thermal shock is not applicable to class N, P, and organic class Y.	Manufacturer Comment	Thermal shock is not applicable to class N, P, and organic class Y.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
35	Table H-I Footnote <u>3</u> /	Update From: Biased HAST test shall apply to non-hermetic packages only. For ceramic hermetically sealed packages biased HAST test shall be replaced with HTOL (Steady State Life Test, MIL-STD-883, TM 1005) test for bump integrity under high temperature (either 110°C/85% RH for 96 hours or 130°C/85% RH for 264 hours). To: Biased HAST test shall apply to non-hermetic packages only. For ceramic hermetically sealed packages biased HAST test shall be replaced with HTOL (Steady State Life Test, MIL-STD-883, TM 1005) test for bump integrity under high temperature (either 130°C/ for 96 hours minimum or 110°C/ for 264 hours minimum).	Manufacturer Comment	This is an editorial correction to fix an error where the test temperatures were inverted. The change correctly associates the 130°C condition with the 96-hour duration and the 110°C condition with the 264-hour duration. "85%RH" should be removed since TM1005 only specifies temperature and no specific moisture requirement for hermetic seal packages.
36	TABLE H-IA Footnote <u>5</u> /	Update From: <u>5</u>/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002. To: <u>5</u>/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002. for Class Y, subject to the requirements specified in paragraph 3.10.	DLA Weapons Support, & Manufacturers comments	Bridges the gap for solderability testing between MIL-STD-883, TM2003 and IPC/JEDEC J-STD-002.
37	TABLE H-IB Footnote <u>5</u> /	Update From: <u>5</u>/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002. To: <u>5</u>/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002. subject to the requirements specified in paragraph 3.10.	DLA Weapons Support, & Manufacturers comments	Bridges the gap for solderability testing between MIL-STD-883, TM2003 and IPC/JEDEC J-STD-002.

REF No.	PARAGRAPH	CHANGE	SOURCE	REASON
38	TABLE H-IIB Group number 3	Update Biased HAST From: b. Biased HAST (500 hours, +130°C , 85% RH) To: b. Biased HAST (192 hours, +130C, 85%) or (528 hours, +110C, 85%) or (2000 hours, +85C, 85%)	Manufacturer Comment	Manufacturers consider 500 hours too extreme for plastic packages.
39	TABLE H-IIB Footnote <u>3/</u>	Update Footnote <u>3/</u> From: <u>3/</u> Five hundred hours of highly accelerated stress testing (HAST) is preferred but the qualifying activity shall consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing shall be included in the QM plan. To: <u>3/</u> The qualifying activity shall consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing shall be included in the QM plan.		Remove reference to 500 hours of HAST. This update aligns with the change proposal outline previously in Ref No. 28
42	TABLE H-IIB	Added Moisture sensitivity Level (MSL) test method From: Per manufacturer's specification To: Per manufacturer's specification or JEDEC J-STD-020	DLA Weapons Support	To be consistent with MSL referenced in B.3.13
40	H.3.6.1 H.3.6.2	Add new sections H.3.6.1 and H.3.6.2 to formalize the Certificate of Compliance (C of C) signature delegation process and define C of C submission requirements for SMD revisions.	DLA Weapons Support	This change introduces a formal process for C of C signature authority.
41	J.3.5	Update From: ...except as modified in accordance with section 4.2... To: ...except as modified in accordance with SMD section 4.2...	DLA Weapons Support	This is an editorial clarification.
42	TABLE H-IIB	Added Moisture sensitivity Level (MSL) test method From: Per manufacturer's specification To: Per manufacturer's specification or JEDEC J-STD-020	DLA Weapons Support	To be consistent with MSL referenced in B.3.13