

PERFORMANCE SPECIFICATION

RESISTOR, CHIP, FIXED, BULK METAL FOIL,
ESTABLISHED RELIABILITY, SPACE LEVEL,
GENERAL SPECIFICATION FOR

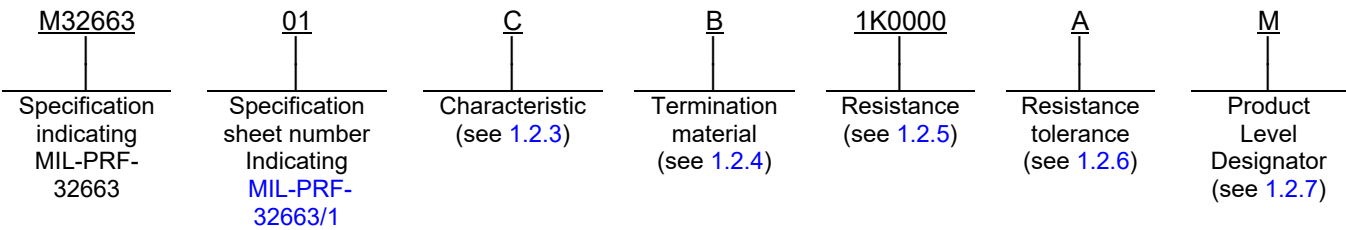
This specification is approved for use by all Departments
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for established reliability (ER), and space level, fixed, bulk metal foil (BMF), ultra-precision chip resistors primarily intended for incorporation into surface mount applications. These resistors have a high degree of stability with respect to time under normal conditions. ER resistors covered by this specification have life failure rates (FR) ranging from 1 percent to 0.001 percent per 1,000 hours (see 1.2.7). These FRs are established at 60 percent confidence on the basis of life tests. Table I provides a summary of performance characteristics for these resistors. Designers are CAUTIONED on using these resistors in high power pulse applications (see 6.7).

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). The PIN provides information concerning the resistor style and resistor characteristic, termination type, resistance value, resistance tolerance, and product designator. The PIN is in the following form:



1.2.2 Style. The style (see 3.1) is identified by a three-letter symbol RF* followed by a four-digit number. The first two letters identify BMF ultra-precision resistors in a flat chip configuration, the last letter (*) identifies the termination (see 1.2.4) and the numbers identify the size of the resistor.

1.2.3 Characteristic. The characteristic is identified by a single letter C, D or E, in accordance with table I.

1.2.4 Termination material. The termination material designation will be in accordance with table II (see 4.8.1.3).

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support (Columbus), ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990, or emailed to resistor@dlamail. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



MIL-PRF-32663
w/AMENDMENT 1

TABLE I. Characteristics.

Test or condition	Units	Symbol		
		C	D	E
Maximum ambient temperature at full wattage (see 3.6)	Temperature °C	70	70	70
Maximum ambient temperature at zero wattage (see 3.6)	Temperature °C	150 200 <u>7/</u>	150 200 <u>7/</u>	150 200 <u>7/</u>
Thermal shock (TS) (see 3.9) Qualification (100 cycles) Group A Group C	Maximum percent change in resistance (0.005 ohm additional allowed for measurement error)	±0.03% ±0.01% ±0.01%	±0.03% ±0.02% ±0.02%	±0.1% ±0.1% ±0.1%
Short time overload (STOL) (see 3.10)		±0.01%	±0.02%	±0.1%
Power conditioning (PC) (see 3.11)		±0.01%	±0.02%	±0.1%
Combined change after TS, STOL & PC		±0.02%	±0.03%	±0.1%
Low temperature operation (see 3.12)		±0.01%	±0.02%	±0.1%
High temperature exposure (see 3.13)		±0.02% ±0.03% <u>7/</u>	±0.05%	±0.1%
Moisture resistance (see 3.15)		±0.05%	±0.1%	±0.2%
Life (see 3.17 & figure 3) Qualification FR level		±0.025% ±0.1%	±0.05% ±0.5%	±0.5% ±2.0%
+125°C power rating (see 3.17) <u>7/</u>		±0.025%	±0.05%	±0.5%
Board flex (see 3.20)		±0.1%	±0.2%	±0.2%
Resistance to soldering heat (see 3.14)	Maximum percent change in resistance (0.01 ohm additional allowed for measurement error)	±0.02% ±0.03% <u>7/</u>	±0.03% ±0.05% <u>7/</u>	±0.2% ±0.3% <u>7/</u>
Resistance temperature coefficient (see 3.16)	ppm/°C	±3 <u>1/</u> ±5 <u>2/</u>	±5 <u>1/</u> ±8 <u>2/</u>	±10
Resistance tolerance ± percent (see table V)	± percent	0.01 <u>1/</u> 0.02 <u>3/</u> 0.05 <u>4/</u> 0.1 <u>5/</u> 0.25 <u>6/</u>	0.02 <u>1/</u> 0.05 <u>3/</u> 0.1 <u>4/</u> 0.25 <u>5/</u> 0.5 <u>6/</u>	0.1 <u>3/</u> 0.25 <u>4/</u> 0.5 <u>5/</u> 1.0 <u>6/</u>

- 1/ For values of 250 Ohms and higher.
2/ For value range of 10 to < 250 Ohms.
3/ For value range of 100 and higher.
4/ For value range of 50 and higher.
5/ For value range of 25 and higher.
6/ For value range of 10 and higher.
7/ For termination G only.

MIL-PRF-32663
w/AMENDMENT 1

TABLE II. Termination material.

Type	Material	Termination area	Code letters
Solderable <u>1/</u>	Base metallization barrier metal, solder coated	Wraparound <u>2/</u>	B <u>2/</u>
Solderable <u>1/</u>	Base metallization barrier metal, gold coated	Wraparound <u>2/</u>	G <u>2/</u> <u>3/</u>

1/ Solderable termination is suitable for solder reflow operation and will meet the solderability test (see [figure 2](#)).

2/ See [6.4.4](#).

3/ See [3.5.3](#), [3.6](#), [6.4.5](#) and [Table A-I](#) for application considerations.

1.2.5 Resistance. The nominal resistance expressed in ohms is identified by six characters consisting of five digits and a letter. The letter is used simultaneously as a decimal point and as a multiplier. For resistance values:

- Greater than or equal to 1 ohm but less than 1,000 ohms, the letter R is used to represent a decimal point and multiplier (X1) (see table III).
- Greater than or equal to 1,000 ohms but less than 1 megohm, the letter K is used to represent a decimal point and multiplier (X1000) (see table III).

All digits preceding and following the letters (R and K) of the group represent significant figures. The resistance value designations are shown in table III. Minimum and maximum resistance values will be as specified herein (see [3.1](#)). The standard values for every decade will follow the sequence specified in [table IV](#) for resistance tolerances B, C, D and F. The resistance values for tolerances T, Q and A may be any value within the limits specified (see [3.1](#)), but it is preferred that values be chosen from the B, C and D columns of [table IV](#).

TABLE III. Designation of resistance values.

Designation	Resistance (ohms)
1R0000 to 9R8800 inclusive	1.0 to 9.88 inclusive
10R000 to 98R800 inclusive	10.0 to 98.8 inclusive
100R00 to 988R00 inclusive	100 to 988 inclusive
1K0000 to 9K8800 inclusive	1000 to 9880 inclusive
10K000 to 98K800 inclusive	10000 to 98800 inclusive
100K00 to 988K00 inclusive	100000 to 988000 inclusive

MIL-PRF-32663
w/AMENDMENT 1

TABLE IV. Standard resistance values for the 10 to 100 decade.

B C D	F	B C D	F	B C D	F	B C D	F	B C D	F	B C D	F
10.00	10.00	15.40	15.40	23.70	23.70	34.80	34.80	51.10	51.10	75.00	75.00
10.10		15.60		24.00		35.20		51.70		75.90	
10.20	10.20	15.80	15.80	24.30	24.30	35.70	35.70	52.30	52.30	76.80	76.80
10.40		16.00		24.60		36.10		53.00		77.70	
10.50	10.50			24.90	24.90	36.50	36.50	53.60	53.60	78.70	78.70
10.60		16.20	16.20	25.20		37.00		54.20		79.60	
10.70	10.70	16.40		25.50	25.50	37.40	37.40	54.90	54.90	80.60	80.60
10.90		16.50	16.50	25.80		37.90		55.60		81.60	
		16.70									
11.00	11.00	16.90	16.90	26.10	26.10	38.30	38.30	56.20	56.20	82.50	82.50
11.10		17.20		26.40		38.80		56.90		83.50	
11.30	11.30	17.40	17.40	26.70	26.70	39.20	39.20	57.60	57.60	84.50	84.50
11.40		17.60		27.10		39.70		58.30		85.60	
11.50	11.50			27.40	27.40	40.20	40.20	59.00	59.00	86.60	86.60
11.70		17.80	17.80	27.70		40.70		59.70		87.60	
11.80	11.80	18.00		28.00	28.00	41.20	41.20	60.40	60.40	88.70	88.70
12.00		18.20	18.20	28.40		41.70		61.20		89.80	
		18.40									
12.10	12.10	18.70	18.70	28.70	28.70	42.20	42.20	61.90	61.90	90.90	90.90
12.30		18.90		29.10		42.70		62.60		92.00	
12.40	12.40	19.10	19.10	29.40	29.40	43.20	43.20	63.40	63.40	93.10	93.10
12.60		19.30		29.80		43.70		64.20		94.20	
12.70	12.70			30.10	30.10	44.20	44.20	64.90	64.90	95.30	95.30
12.90		19.60	19.60	30.50		44.80		65.70		96.50	
13.00	13.00	19.80		30.90	30.90	45.30	45.30	66.50	66.50	97.60	97.60
13.20		20.00	20.00	31.20		45.90		67.30		98.80	
		20.30									
13.30	13.30	20.50	20.50	31.60	31.60	46.40	46.40	68.10	68.10		
13.50		20.80		32.00		47.00		69.00			
13.70	13.70	21.00	21.00	32.40	32.40	47.50	47.50	69.80	69.80		
13.80		21.30		32.80		48.10		70.60			
14.00	14.00			33.20	33.20	48.70	48.70	71.50	71.50		
14.20		21.50	21.50	33.60		49.30		72.30			
14.30	14.30	21.80		34.00	34.00	49.90	49.90	73.20	73.20		
14.50		22.10	22.10	34.40		50.50		74.10			
		22.30									
14.70	14.70	22.60	22.60								
14.90		22.90									
15.00	15.00	23.20	23.20								
15.20		23.40									

MIL-PRF-32663
w/AMENDMENT 1

1.2.6 Resistance tolerance. The resistance tolerance is identified by a single letter in accordance with table V.

TABLE V. Resistance tolerance.

Symbol	Resistance tolerance (percent)
T	±0.01
Q	±0.02
A	±0.05
B	±0.1
C	±0.25
D	±0.5
F	±1.0

1.2.7 Product level designator. The product level designator is specified in table VI by a single letter which identifies ER or space level resistors.

TABLE VI. Product level designator.

Product level designator	Product level
M	1/ 1.0
P	1/ 0.1
R	1/ 0.01
S	1/ 0.001
T	Space level
U	1/ 0.01 with group A and all of B inspection tests performed on each production lot.
V	1/ 0.001 with group A and all of B inspection tests performed on each production lot.

1/ FR level in percent per 1000 hours.

2. APPLICABLE PUBLICATIONS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

(See supplement 1 for list of associated specifications.)

MIL-PRF-32663
w/AMENDMENT 1

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-202 - Electronic and Electrical Component Parts
- MIL-STD-202-106 - Method 106, Moisture Resistance
- MIL-STD-202-107 - Method 107, Thermal Shock
- MIL-STD-202-108 - Method 108, Life (At Elevated Ambient Temperature)
- MIL-STD-202-208 - Method 208, Solderability
- MIL-STD-202-210 - Method 210, Resistant to Soldering Heat
- MIL-STD-202-215 - Method 215, Resistant to Solvents
- MIL-STD-202-218 - Method 218, Board Flex
- MIL-STD-202-303 - Method 303, DC Resistance
- MIL-STD-202-304 - Test Method Standard Method 304, Resistance-Temperature Characteristic
- MIL-STD-690 - Failure Rate Sampling Plans and Procedures
- MIL-STD-790 - Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications
- MIL-STD-1285 - Marking of Electrical and Electronic Parts.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA)

- NASA 1124 - Outgassing Data for Selecting Spacecraft Materials

(Hard copies of this document are no longer available from the NASA Goddard Materials Branch or the DLA Document Services. This information is only available at <https://outgassing.nasa.gov>.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE INTERNATIONAL

- SAE-EIA-554-1 - Assessment of Outgoing Nonconforming Levels in Parts Per Million (ppm)
- SAE-EIA-557 - Statistical Process Control Systems

(Copies of these documents are available online at <https://www.sae.org>.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) INTERNATIONAL

- ASTM E595 - Materials from Outgassing in a Vacuum Environment, Total Mass Loss and Collected Volatile Condensable, Standard Test Method for

(Copies of this document are available online at <http://www.astm.org>.)

GLOBAL ELECTRONICS ASSOCIATION

- IPC CC 830 - Qualification and Performance of Electrical Insulation compound for Printed Wiring Assemblies

(Copies of this document are available online at <https://www.electronics.org/>)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related, specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Resistors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.2.1 have been met and are being maintained.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790 (all product levels) and MIL-STD-690 (ER parts only). In addition, the manufacturer shall also establish a Statistical Process Control (SPC) and Part Per Million (ppm) system that meets the requirements as described in 3.3.1 and 3.3.2 respectively.

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish an SPC system that meets the requirements of SAE-EIA-557. Typical manufacturing processes for application of SPC include formation of resistance elements, trimming, and termination. In addition, the manufacturer shall demonstrate resistance temperature characteristic (RTC) control in the process.

3.3.2 PPM system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a ppm system for assessing the average outgoing quality of lots in accordance with SAE-EIA-554-1 and 4.6.4. Data exclusion, in accordance with SAE-EIA-554-1, may be used with approval of the qualifying activity. The ppm system shall identify the ppm rate at the end of each month and shall be based on a six month moving average. PPM-2 and DC resistance shall be assessed for each style. Due to low production volume, ppm assessment does not apply to space level lots.

3.4 Materials. Materials shall be used which will enable the resistors to meet the performance requirements of this specification. The BMF Ingots used for manufacturing of resistors to this specification, shall be qualified as "Particle Free" in accordance with Appendix C of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. Resistors shall meet the interface and physical dimensions specified (see 3.1).

3.5.1 Termination. Unless otherwise specified, both terminations (areas) shall be available on one surface of the body of the resistor chip (see table II).

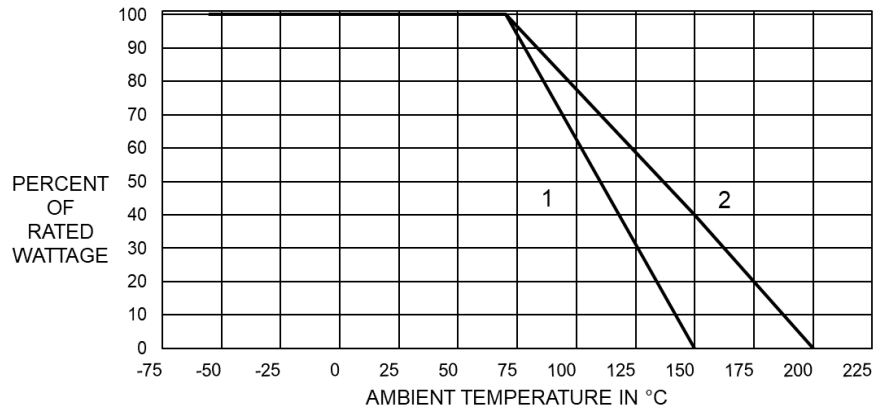
3.5.2 Barrier metallization. The barrier metallization for the B and G terminations shall be nickel. The metallization shall be a minimum of 50 microinches.

3.5.3 Gold termination. Gold termination thickness shall be between 15 and 35 microinches (see 6.4.5)

3.5.4 Pure tin. The use of pure tin, as an underplate or final finish is prohibited both internally and externally. Tin content of resistor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.4.6).

3.6 Power rating. The resistors shall have a power rating based on continuous full-load operation at an ambient temperature of 70°C for different mounting substrates (see 3.1). For operation at temperatures in excess of 70°C the load shall be derated in accordance with figure 1.

MIL-PRF-32663
w/AMENDMENT 1



NOTE: These curves - (1) for termination B or G when mounted on FR4 (or similar), (2) for termination G when mounted on polyimide or ceramic, indicate the percentage of nominal wattage to be applied at temperature higher than 70°C. The curves apply only to units mounted on a board (see 4.8.1.3); however, at no time shall the applied voltage exceed the maximum for each style (see 3.1).

FIGURE 1. Derating curve for high ambient temperatures and different mounting substrates.

3.7 Voltage rating. Resistors shall have a rated DC continuous working voltage or an approximate sine wave root-mean-square (rms) continuous working voltage corresponding to the wattage (power) rating, as determined from the following formula:

$$E = \sqrt{PR}$$

Where:

E = Continuous rated dc or rms working voltage in volts.
P = Rated wattage in watts.
R = Nominal resistance in ohms.

3.8 DC resistance. When resistors are tested as specified in 4.8.2, the DC resistance shall be within the specified tolerance of the nominal resistance (see 1.2.5).

3.8.1 Resistance value deviations. All maximum deviations as specified in this section are to be considered absolute limits with the exception of the contact resistance adjustments.

3.9 Thermal shock.

3.9.1 Thermal shock (failure rate levels (FRL) M, P, R, S, U and V). When resistors are tested as specified in 4.8.3, there shall be no evidence of mechanical damage (see 3.24.2). The combined change in resistance for thermal shock, short time overload and power conditioning shall not exceed the value listed in table I, and shall be within the specified initial resistance tolerance of the nominal resistance for group A tests. The change in resistance for group C tests shall not exceed the value specified in table I.

3.9.2 Thermal shock (space level only). For the 100 cycle qualification test, there shall be no evidence of mechanical damage (see 3.24.2); the change in resistance shall not exceed the values listed in table I.

3.10 Short time overload. When resistors are tested as specified in 4.8.4, there shall be no evidence of arcing, burning, or charring, the combined change in resistance for thermal shock, short time overload and power conditioning shall not exceed the values listed in table I and shall be within the specified initial resistance tolerance of the nominal resistance for group A tests. For group C test the change in resistance shall not exceed the values listed in table I.

MIL-PRF-32663
w/AMENDMENT 1

3.11 Power conditioning. When resistors are tested as specified in 4.8.5, there shall be no evidence of mechanical damage (see 3.24.2); the change in resistance shall not exceed the values listed in table I. For group A test the combined change in resistance, for thermal shock, short time overload and power conditioning, shall not exceed the values listed in table I.

3.12 Low temperature operation. When resistors are tested as specified in 4.8.6, there shall be no evidence of mechanical damage (see 3.24.2); the change in resistance between the initial and the final measurement at 25°C ±5°C shall not exceed the value specified in table I.

3.13 High temperature exposure. When resistors are tested as specified in 4.8.7, there shall be no evidence of mechanical damage (see 3.24.2); the change in resistance shall not exceed the value specified in table I.

3.14 Resistance to soldering heat. When resistors are tested as specified in 4.8.8, there shall be no evidence of mechanical damage (see 3.24.2); no demetallization or leaching of the terminations, and the change in resistance shall not exceed the value specified in table I.

3.15 Moisture resistance. When resistors are tested as specified in 4.8.9, there shall be no evidence of mechanical damage (see 3.24.2); the change in resistance between the initial and final measurements shall not exceed the value specified in table I.

3.16 Resistance temperature characteristic. When resistors are tested as specified in 4.8.10, the resistance temperature characteristic, at each of the temperatures specified in 4.8.10a referred to 25°C ± 3°C, shall not exceed the values specified in table I.

3.17 Life. When resistors are tested as specified in 4.8.11, there shall be no evidence of mechanical damage (see 3.24.2) and the change in resistance shall be in accordance with 3.17.1 through 3.17.4.

3.17.1 Qualification. The change in resistance between the initial measurement and any succeeding measurements up to and including 2,000 hours shall not exceed the value specified in table I.

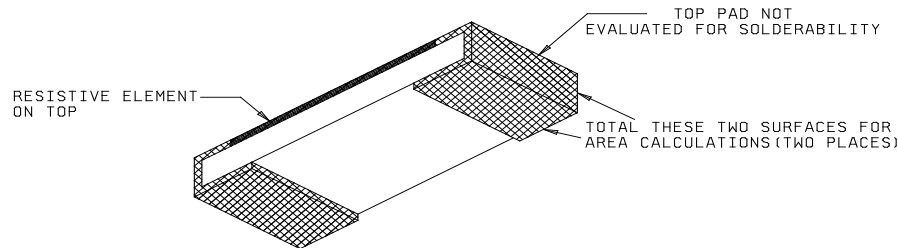
3.17.2 FRL determination (ER). The change in resistance between the initial measurement and any of the succeeding measurements shall not exceed the value specified in table I. This single failure criterion shall be applicable to all measurements during the life test for purposes of determining FRL qualification and is applicable as a parallel requirement with 3.17.1 to measurements made during the life test specified for qualification inspection.

3.17.3 +125°C power rating (for G termination). For qualification inspection only, the change in resistance after 2000 hours shall not exceed the value specified in table I. The data acquired is not applicable to the establishment, maintenance, or extension of FR level (see 3.1).

3.17.4 +70°C power rating (for G termination). For qualification inspection only, the change in resistance after 2000 hours shall not exceed the value specified in table I for qualification. The data acquired is not applicable to the establishment, maintenance, or extension of FR level (see 3.1).

3.18 Solderability (applicable to terminations B and G). When resistors are tested as specified in 4.8.12, the immersed metallized surface shall be at least 95 percent covered with a new clean smooth coating and shall exhibit no demetallization or leaching of the terminal areas. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area. The top surface of the termination need not be considered in the evaluation for solderability (see figure 2). For coverage calculations, defective areas on each termination shall be compared to the total area of the end and bottom surfaces on the same termination.

Resistor with B and G terminations



NOTE:

Ends and bottom are surfaces to be evaluated for B and G terminations.

FIGURE 2. Solderability coverage.

3.19 Mounting integrity.

3.19.1 Solder mounting integrity (applicable to termination B and G). When resistors are tested as specified in 4.8.13.1, the resistor shall remain mounted intact to the test board and there shall be no evidence of mechanical damage (see 3.24.2).

3.20 Board flex. When tested in accordance with 4.8.14, resistors shall meet the following:

- a. Resistance:
 - (1) Measured at maximum board deflection. Change in resistance between initial reading and while at maximum board deflection shall not exceed limit in table I.
 - (2) Measured after removal of force for board flex test. Change in resistance between initial reading and post-board flex test shall not exceed limit in table I.
- b. Visual Examination: There shall be no evidence of mechanical damage (see 3.24.2) to the resistor body or termination when examined in accordance with 4.8.14 at the end of the test.

3.21 Resistance to solvents. When resistors are tested as specified in 4.8.15, there shall be no evidence of mechanical damage (see 3.24.2) and the marking shall remain legible. The color dot marking shall be in accordance with MIL-STD-1285.

3.22 Marking legibility test (applicable to laser marked resistors). When resistors are tested as specified in 4.8.16, the marking shall remain legible.

3.23 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.24 Visual and mechanical inspection.

3.24.1 Visual inspection during in-process, qualification Group I and Group A Subgroup 2 inspections. When resistors are inspected as specified in 4.8.1.1a, it shall be verified that the interface, physical dimensions, marking, and workmanship are in accordance with the applicable requirements.

3.24.2 Mechanical inspection after Group A, Group B and Group C inspections. When resistors are inspected as specified in 4.8.1.1b, there shall be no evidence of mechanical damage in accordance with the applicable requirements.

MIL-PRF-32663
w/AMENDMENT 1

3.25 Outgassing (space level only). When examined as specified in 4.8.17, the samples shall meet the following requirements:

- a. Total Mass Loss (TML) shall not exceed 1 percent.
- b. Volatile Condensable Material (VCM) shall not exceed 0.1 percent.

3.25.1 Outgassing test data (see 2.2.2). Data listed in NASA 1124 may be used in lieu of actual test data for applicable materials.

3.26 Marking. A noncorrosive label containing the following information shall be applied to each unit package. PIN, "JAN" marking, date code, source code, and manufacturer's production lot code (see 4.6.2.2). Date and source code shall be in accordance with MIL-STD-1285. The following is an example of the complete marking.

12345	-	CAGE
1901J	-	Date code and JAN marking
M3266301C	-	PIN (see 1.2.1)
1K0000AM	-	PIN (see 1.2.1)
#####	-	Manufacturer's production lot code

The date code shall be the date of the wafer singulation operation. The common manufacturing record shall include the same date code as that placed on the parts covered by the record. At the option of the manufacturer, resistors may be marked (i.e., laser, screen printed, etc.). Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. Additional marking may appear on the package provided that it does not interfere with the required marking. The marking process must be approved by the qualifying activity based on testing specified herein. The marking shall remain legible after all tests.

3.26.1 Individual chip marking. Marking of individual chip resistors is not required but is permitted. Where space allows, chip resistors may be marked in accordance with the following rule: First four characters out of six indicating the resistance, see 1.2.5, shall be used for marking.

3.26.2 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable associated specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable associated specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the military part number and the "JAN" or "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 6,069,576 for the certification mark "JAN" and Registration Number 2,577,735 for the certification mark "J".

3.26.3 Allowable substitution. A manufacturer may supply better products to less stringent product levels, resistance temperature characteristics, or resistance tolerances as specified in table VII. The label shall reflect the original part number ordered. Parts that are physically marked shall not be remarked unless specified in the contract or order (see 6.2).

3.27 Workmanship. Resistors shall be processed in such a manner as to be uniform in quality and shall meet the requirements of 3.1, 3.4, 3.5, 3.5.1 through 3.5.4 inclusive, and be free from other defects that will affect life, serviceability, or appearance, and shall pass the visual inspection as specified in Appendix B.

MIL-PRF-32663
w/AMENDMENT 1

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.4).
- b. Verification of qualification (see 4.5).
- c. Conformance inspection (see 4.6).
- d. Periodic inspection (see 4.7).

4.2 Reliability and quality.

4.2.1 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance is a prerequisite for qualification and verification of qualification.

4.2.2 SPC program. A SPC program shall be maintained in accordance with SAE-EIA-557. Evidence of such compliance shall be verified by the qualifying activity of this specification as a prerequisite for qualification and continued qualification.

TABLE VII. Allowable substitution.

Product level	Acceptable FR substitute
T (space) V (0.001) U (0.01) S (0.001) R (0.01) P (0.1) M (1.0)	----- T 1/ V, T 1/ V, T 1/ V, U, S, T 1/ V, U, S, R, V, U, S, R, P
Resistance tolerance	Acceptable resistance tolerance substitute
T Q A B C D F	---- T T, Q T, Q, A T, Q, A, B T, Q, A, B, C T, Q, A, B, C, D
Characteristic	Acceptable characteristic substitute
C D E	--- C C, D

1/ T level substitution is by qualifying activity approval.

4.3 Inspections conditions and precautions.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the general requirements of MIL-STD-202.

4.3.2 Precautions. Adequate precautions shall be taken during inspection to prevent condensation of moisture on resistors, except during the moisture resistance temperature cycling tests.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3).

MIL-PRF-32663
w/AMENDMENT 1

4.4.1 Sample. The number of sample units comprising a sample of resistors to be submitted for qualification inspection shall be as specified in [appendix A](#) to this specification. The sample shall be taken at random from a production run and shall be produced with equipment and procedures normally used in production and which have been subjected to and passed the requirements of In-process and Quality conformance inspection (see [4.6.3](#)). Qualification shall not be granted if group A inspection requirements are not complied with.

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in [table VIII](#) in the order shown. Sample sizes and extent of qualification for characteristics shall be specified in [appendix A](#) of this specification.

4.4.3 Defective. Defectives in excess of those allowed in [table VIII](#) shall be cause for refusal to grant qualification.

4.4.4 FRL verification (ER only).

4.4.4.1 Procedure. FR qualification shall be in accordance with the general requirements of [MIL-STD-690](#) and the following details:

- a. Procedure I: Qualification at the initial FR level. Level M (1.0 percent) of FRSP-60 shall apply. Sample units shall be subjected to the qualification inspection specified in group IV, [table VIII](#) (see [4.4.2](#)). Entire life test sample shall be continued on test to 10,000 hours as specified in [3.17.1](#) upon completion of the 2,000 hour qualification.
- b. Procedure II: Extension of qualification to lower FR levels. To extend qualification to the R (0.01 percent), S (0.001 percent), U (0.01 percent) and V (0.001 percent) FR levels, two or more styles of similar construction may be combined.
- c. Procedure III: Maintenance of FR level qualification. Maintenance period A of FRSP-10 shall apply. Regardless of the number of production lots produced during this period, the specified number of unit hours shall be accumulated to maintain qualification (see [4.7](#)).

4.5 Verification of qualification. Every 12 months the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification is based on meeting the following requirements.

- a. [MIL-STD-790](#) program.
- b. Design of resistor has not been modified.
- c. Lot rejection for group A (subgroup 2 and subgroup 4) does not exceed 5 percent or one lot, whichever is greater.
- d. Lot rejection for group B inspection does not exceed 5 percent or one lot, whichever is greater.
- e. Periodic group C inspection requirements are met.
- f. FRL's are maintained as required.
- g. PPM assessment. (NOTE: Grouping of styles is permitted).
- h. Continued qualification to the space level (T) shall be based on:
 - (1) Maintaining minimum Established Reliability Failure Rate Level of R, S, U or V.
 - (2) Maintenance of the test capability and lot control system for testing space level resistors (see [A.3.1](#)).
 - (3) Submission of monthly Group-C subgroup 1 (Life test) samples representative of their production percentage or more.
 - (4) Reporting of Space-Level Group-C testing for each [MIL-STD-690](#) reporting period as a subgroup (with styles, pieces on test, accumulated hours, etc.).

TABLE VIII. Qualification inspection.

MIL-PRF-32663
w/AMENDMENT 1

Inspection	Requirement paragraph	Method Paragraph	Number of samples <u>3/</u>	Number of defects allowed
<u>Certification requirements</u>				
Outgassing (space level only)	3.25	4.8.17	-----	-----
<u>Group I</u> Visual and mechanical inspection	3.1, 3.4, 3.5, 3.5.1 through 3.5.4 inclusive, 3.24, and 3.27	4.8.1	All sample units except group V	0
DC resistance	3.8	4.8.2		
<u>Group II</u> Resistance to soldering heat Resistance temperature characteristic Low temperature operation High temperature exposure	3.14 3.16 3.12 3.13	4.8.8 4.8.10 4.8.6 4.8.7	10 highest 10 critical 10 lowest (30)	1
<u>Group III</u> Resistance to soldering heat Moisture resistance	3.14 3.15	4.8.8 4.8.9	10 highest 10 critical 10 lowest (30)	1
<u>Group IV</u> Life	3.17 and 3.17.1	4.8.11	34 highest 34 critical 34 lowest (102)	1
<u>Group IVA 1/</u> +125°C power rating	3.17 and 3.17.3	4.8.11	34 highest 34 critical 34 lowest (102)	1
<u>Group IVB 1/</u> +70°C derated power on fiberglass board	3.17 and 3.17.4	4.8.11	34 highest 34 critical 34 lowest (102)	1
<u>Group V</u> Solderability	3.18	4.8.12	10 any value	1
<u>Group VI</u> Solder mounting integrity Board flex	3.19.1 3.20	4.8.13.1 4.8.14	10 any value 10 any value (20)	1
<u>Group VII</u> Resistance to solvents Marking legibility test (laser marking) <u>2/</u>	3.21 3.22	4.8.15 4.8.16	10 any value 10 any value (20)	0
<u>Group VIII (space level only)</u> Thermal shock (100 cycles)	3.9.2	4.8.3	10 highest 10 critical 10 lowest (30)	0

1/ Test applicable to G termination only.

2/ Test applicable for laser marked parts only.

3/ The total number of samples shall be divided into 2 equal parts for highest and lowest values, if critical value isn't applicable for the product style.

MIL-PRF-32663
w/AMENDMENT 1

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery.

4.6.1.1 ER resistors. Inspection of product for delivery shall consist of in-process inspection (4.6.3), group A and group B inspections. Group B inspection for preparation of delivery is not required when the qualifying activity has allowed group B testing to be performed quarterly (see table XII). Group B inspection shall be performed on inspection lot basis for product level M, P, R, and S and production lot for product level T, U, and V.

4.6.1.2 Space level. Inspection of product for delivery shall begin with "R", "S", "U", or "V" level product then upscreened to space level by resubmitting them to the entire group A and B inspection, and shall be performed on a production lot basis. Test deletion or reduction is not allowed for space level product.

4.6.2 Inspection and production lot.

4.6.2.1 Inspection lot. An inspection lot shall consist of resistors of the same style, characteristic, and termination type and manufactured under essentially the same process and conditions with the same basic materials and having the same date code. ER and space level lots shall be kept separate. An inspection lot can combine resistors of different characteristics for group A subgroups 2, 3, and 4, and group B inspections.

4.6.2.2 Production lot. A production lot shall consist of all resistors of the same style, nominal resistance value, resistance tolerance, resistance temperature characteristic, termination material manufactured and tested as a group using the same material, processes, specifications and procedures. Lot identity shall be maintained throughout the manufacturing cycle. ER and space level lots shall be kept separate.

4.6.3 In-process inspection and quality conformance inspection.

4.6.3.1 In-process inspection. Each production lot shall have an in-process precap visual inspection prior to external overcoat application and resistor singulation, and shall be in accordance with table IX.

TABLE IX. In-process inspection.

Inspection	Requirement Paragraph	Test method paragraph	Sample size
Precap visual inspection	Appendix B.3	4.8.1	100 percent

4.6.3.1.1 In-process screening. Each production lot shall be submitted to 100% electrical screening that includes at least Thermal Shock, Power Shot (Overload) and CLT (Component Linearity Test) followed with resistance measurements. Internal limits for resistance change shall apply. This screening will be part of the inspection system.

4.6.3.2 Group A inspection. Group A inspection shall consist of the examinations and tests as specified in table X.

4.6.3.2.1 Subgroup 1 tests. Subgroup 1 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Resistors that are out of resistance tolerance, or which experience a change in resistance greater than that permitted for the tests of this subgroup, shall be removed from the lot. Lots having more than 5 percent total rejects, due to exceeding the specified resistance tolerance and resistance change limit, shall not be furnished on contracts. For resistors with T, Q and A tolerance, the rejects due to exceeding the resistance tolerance shall not be counted and 5% criterion will apply only to resistors with resistance changes exceeding the limit after testing.

MIL-PRF-32663
w/AMENDMENT 1

4.6.3.2.1.1 Manufacturer's production inspection. If the manufacturer performs tests similar to those specified in subgroup 1, [table X](#) as the final step of his production process, group A, subgroup 1 inspection may be waived. Authority to waive the subgroup 1 inspection shall be granted by the qualifying activity only. The following criteria must be complied with:

- a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than those specified for subgroup 1. Test conditions shall be equal to or more stringent than those specified for subgroup 1 tests.
- b. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.
- c. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.
- d. The lot rejection criteria are the same as, or more stringent than, those specified herein.
- e. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification to and concurrence from the qualifying activity.
- f. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than those specified for subgroup 1. Test conditions shall be equal to or more stringent than those specified for subgroup 1 tests.
- g. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.
- h. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.
- i. The lot rejection criteria are the same as, or more stringent than, those specified herein.
- j. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification to and concurrence from the qualifying activity.
- k. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than those specified for subgroup 1. Test conditions shall be equal to or more stringent than those specified for subgroup 1 tests.
- l. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.
- m. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.
- n. The lot rejection criteria are the same as, or more stringent than, those specified herein.
- o. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification to, and concurrence from, the qualifying activity.

MIL-PRF-32663
w/AMENDMENT 1

TABLE X. Group A inspection (ER and space level).

Inspection	Requirement Paragraph	Method paragraph	Sampling procedure
<u>Subgroup 1</u>			
Thermal shock	3.9	4.8.3	4.6.3.2.1
Short time overload	3.10	4.8.4	
Power conditioning	3.11	4.8.5	
DC resistance	3.8	4.8.2	
<u>Subgroup 2</u>			
Visual inspection	3.1, 3.4, 3.5 through 3.5.4 inclusive, and 3.24	4.8.1	4.6.3.2.2
<u>Subgroup 3</u>			
Solderability <u>1/</u>	3.18	4.8.12	4.6.3.2.3
<u>Subgroup 4</u> <u>2/</u>			
Resistance to solvents	3.21	4.8.15	4.6.3.2.4
Marking legibility <u>3/</u>	3.22	4.8.16	

1/ The manufacturer may request the deletion of the Subgroup 3 solderability test, provided an in-line or process control system for assessing and assuring the solderability of terminations can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement in case of dispute. If the design, material, construction, or processing of the part is changed or if there are any quality problems, the qualifying activity may require resumption of the test. (NOTE: Not applicable to space level.)

2/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space level.)

3/ Test applicable for laser marked parts only.

4.6.3.2.2 Subgroup 2 (visual inspection). The subgroup 2 test shall be performed on an inspection lot basis for ER parts and a production lot basis for space level parts. A sample of parts shall be randomly selected in accordance with [table XI](#). If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of parts shall be randomly selected in accordance with [table XI](#). If one or more defects are found in this second sample for the same quality characteristic, the lot shall be rejected and shall not be supplied to this specification.

4.6.3.2.3 Subgroup 3 (solderability) test. The subgroup 3 test shall be performed on an inspection lot basis for ER parts and on a production lot basis for space level parts. A sample shall be randomly selected from each lot in accordance with [table XI](#). As an option, the manufacturer may use electrical rejects from subgroup 1 tests for all or part of the sample. If there are one or more defects, the lot shall be considered to have failed.

4.6.3.2.3.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in [3.18](#). An additional sample shall be randomly selected from each production lot in accordance with [table XI](#). If the lot fails this solderability test, the lot may be reworked and retested. Any individual production lot that fails the solderability retest shall be considered to have failed and that lot will not be supplied to the requirements of the specification.

4.6.3.2.3.2 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

MIL-PRF-32663
w/AMENDMENT 1

TABLE XI. Sampling plans for subgroup 2 and subgroup 3 and ppm assessment.

Lot size	Sample size for subgroup 2	Sample size for subgroup 3	Sample size for ppm assessment
1 to 5	100%	100%	100%
6 to 13	100%	5	100%
14 to 125	13	5	100%
126 to 150	13	5	125
151 to 280	20	5	125
281 to 500	29	5	125
501 to 1,200	34	5	125
1,201 to 3,200	42	5	125
3,201 to 10,000	50	8	125
10,001 to 35,000	60	13	294
35,001 to 150,000	74	20	294
150,001 to 500,000	90	20	345
500,001 and over	102	20	435

4.6.3.2.4 Subgroup 4. The manufacturer may use electrical rejects from the subgroup 1 screening tests for all or part of the samples to be used for the subgroup 4 testing. In case there are one or more defects, the lot shall be considered to have failed.

- a. Laser marked resistors. Twelve samples of laser marked resistors shall be selected randomly from each inspection lot and subjected to the subgroup 4 tests (six to resistance to solvents and six to marking legibility).
- b. Ink marked or color dot marked resistors. Six resistors marked with color dots or screen printed characters shall be subjected to resistance to solvents test only.

4.6.3.2.4.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. Each production lot that was used to form the failed inspection lot shall be individually submitted to the subgroup 4 test as required in 3.21 or 3.22.

- a. For either laser marked or ink/color dot marked parts, if the failures occurred during resistance to solvents testing, then an additional eight samples shall be randomly selected from each production lot and tested for resistance to solvents.
- b. If the failures occurred during marking legibility testing, then an additional eight samples shall be randomly selected from each production lot and tested for marking legibility. If there is one or more defects in the production lot sample, that production lot shall be considered to have failed and that product will not be supplied to the requirements of this specification. Individual production lots that pass the minimum marking test are available for shipment.

4.6.4 PPM assessment. The manufacturer shall establish and maintain a system for assessing the average outgoing quality in ppm of lots supplied to this specification. This ppm assessment should be based on inspections performed on each inspection lot to verify that resistors meet DC resistance and tolerance requirements (i.e., ppm-2). For ER resistors, this inspection shall occur after the group A, subgroup 1, 100 percent screens have been completed. In the event of one or more failures, the lot shall be rejected.

- 4.6.4.1 Sampling plans. Minimum sample sizes for inspection lots shall be selected in accordance with table XI.

MIL-PRF-32663
w/AMENDMENT 1

4.6.4.2 Rejected lots. Any rejected inspection lot shall be segregated from new lots and those lots which have passed the ppm assessment:

- a. The manufacturers can submit individual production lots that do not contain the samples that failed the inspection lot test to the ppm assessment. A sample from these production lots shall be selected in accordance with [table XI](#). Those production lots that have zero defects are available for shipment. Data from these production lots shall also be used for ppm calculations.
- b. For those production lots that contain the samples that failed the inspection lot test, the production lot may be rescreened for the quality characteristics found defective in the sample and any defects removed. A second sample in accordance with [table XI](#) shall be selected. If one or more defects are found, this lot is rejected and shall not be supplied to the specification.

4.6.4.3 PPM calculations. PPM calculations shall be based on the accumulated results of the initial sample. Calculations and exclusions shall be in accordance with [SAE-EIA-554-1](#). (NOTE: PPM calculations shall not be based on the second sample submission for a rejected lot as described in [4.6.4.2](#)).

4.6.5 Group B inspection. Group B inspection shall consist of the inspections specified in table XII in the order shown, and shall be performed on samples from lots which have been subjected to and have passed the group A inspection. Group B inspection shall be performed on weekly inspection lot basis for product levels M, P, R, S, and on every production lot for product level T, U, and V.

TABLE XII. Group B inspection (ER and space level).

Inspection	Requirement paragraph	Method paragraph	Number of Samples
Weekly			
<u>Subgroup 1</u> <u>1/</u> Resistance temperature characteristic (RTC)	3.16	4.8.10	20 samples
<u>Subgroup 2</u> <u>2/</u> Solder mounting integrity Board flex	3.19.1 3.20	4.8.13.1 4.8.14	10 samples 10 samples

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity can be performed on a quarterly basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to T, U and V failure rate levels).

2/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, these tests, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every three years after the deletion as part of long term design verification. If the design, material, construction, or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute. (NOTE: Not applicable to T, U and V failure rate levels).

4.6.5.1 Sampling plan.

4.6.5.1.1 Subgroup 1. Twenty sample units shall be randomly selected for test. If one or more defects are found, the affected production lot shall be 100% screened for RTC [on unmounted units] and defectives removed. After screening and removal of defectives, a new sample of 20 parts shall be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.5.1.2 Subgroup 2. Ten sample units shall be randomly selected for each of the tests. If one or more defects are found, a 10 piece sample shall be taken from each production lot and the failing test shall be repeated. If one or more defects are found in this second sample, the affected production lot(s) shall be rejected and shall not be supplied to this specification.

MIL-PRF-32663
w/AMENDMENT 1

4.6.5.1.3 Disposition of sample units. Sample units which have been subjected to group B inspection shall not be delivered on the contract or order.

4.7 Periodic group C inspection (ER only). Group C inspection shall consist of the tests specified in [table XIII](#), in the order shown. Group C inspection shall be made on sample units selected from lots which have passed group A and group B inspection. Group C samples shall be representative of production. The allowable number of defectives shall be as indicated in [table XIII](#).

4.7.1 Sampling plan. If more than 1,000 resistors of any style or style grouping are produced over the maintenance period, the group C tests shall be performed as specified. If the production rate is less than 1,000 resistors for any style or style grouping over the maintenance period, then the monthly or quarterly group C inspection may be postponed until at least 1,000 resistors of that style or grouping are produced (except for the monthly life test). In any case, the monthly tests shall be performed at least once every 3 months. The quarterly tests shall be performed at least every 6 months. This requirement is waived if the manufacturer has obtained a reduced inspection status through the qualifying activity.

If the qualification was granted to resistors marked using both marking methods (laser and ink) the sample shall contain units with both markings as described below in relevant paragraph. In the event no production occurred for a particular marking method, units with the missing marking method will be submitted to testing as follows:

- a) Monthly subgroup 1 - for at least 3 months during each 12-months Qualification Verification period.
- b) Quarterly subgroup 1 – for at least one quarter during the above maintenance period.

TABLE XIII. Group C inspection.

Inspection	Requirement paragraph	Method paragraph	Number of samples	Number of defects allowed
Monthly (see 4.7.2)				
<u>Subgroup 1</u>				
Life (ER)	3.17.2	4.8.11	4.7.2.1	4.7.2.1
<u>Subgroup 2 1/</u>				
Thermal shock	3.9	4.8.3	30	1
Low temperature operation	3.11	4.8.6		
Short time overload	3.10	4.8.4		
Quarterly (see 4.7.3)				
<u>Subgroup 1 1/</u>				
Resistance to soldering heat	3.14	4.8.8	30	1
Moisture resistance	3.15	4.8.9		
<u>Subgroup 2 1/</u>				
High temperature exposure	3.13	4.8.7	30	1

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space level.)

4.7.2 Monthly.

4.7.2.1 Subgroup 1. Samples shall be accumulated from ER and T level lots, and placed on extended life test in accordance with 4.8.11 once a month for the full 10,000 hour life test. A sufficient number of samples shall be selected by the manufacturer so that the maintenance of FR requirements complies with the specified maintenance period. Samples shall be representative of production of individual styles, characteristics, marking method and terminations in the maintenance period. As far as practical, the manufacturer shall select the resistance values so that all resistance decades produced during the maintenance period are represented.

4.7.2.2 Subgroup 2. Subgroup 2 tests shall be performed on a sample size of 30 units of one chip size, tightest characteristic, and each termination material with one defective allowed for each group of 30. The sampling shall be made in such a way, that each chip size resistors are tested at least once during 12 months period.

4.7.3 Quarterly.

4.7.3.1 Subgroup 1. Every 3 months, 30 units of one chip size, tightest characteristic, and each termination material produced during this period (any resistance value) shall be subjected to quarterly tests specified in table XIII, in the order shown. The sample shall contain units marked with laser and ink, if current production utilized both marking methods. The sampling shall be made in such a way, that each chip size resistors are tested at least once during 18 months period.

4.7.3.2 Subgroup 2. Every 3 months, 30 units of one chip size, tightest characteristic, and each termination material produced during this period (any resistance value) shall be subjected to quarterly tests specified in table XIII. The sampling shall be made in such a way, that each chip size resistors are tested at least once during 18 months period.

4.7.4 Noncompliance. If a sample fails to pass group C inspection, the contractor shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, processes, etc., and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the Government). Group A and group B inspections may be reinstituted; however, final acceptance shall be withheld until group C reinspection has shown that the corrective action was successful.

4.8 Methods of inspection.

4.8.1 Visual and mechanical inspection and chip mounting.

4.8.1.1 Visual and mechanical inspection.

- a. Visual inspection during in-process, qualification Group I, and Group A Subgroup 2 inspections. Unless otherwise specified, resistors shall be examined under 30X to 60X magnification. In case of conflict 30X will be the referee power, unless otherwise specified, to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, 3.5.1 through 3.5.4 inclusive, 3.24.1 and Appendix B).
- b. Mechanical inspection after qualification and Groups A, B and C inspections. Unless otherwise specified, resistors shall be examined for mechanical damage (see 3.24.2 and Appendix B.4) under 30X minimum for Group A, 4X minimum for Group B and 10X minimum for Group C and qualification.

4.8.1.2 Chip mounting procedures. When specified herein, the chip resistor shall be mounted on a test board as described in 4.8.1.3. For those test procedures where mounting requirements are unspecified, the chip resistors may be tested unmounted using pressure contacts.

MIL-PRF-32663
w/AMENDMENT 1

4.8.1.3 Specified mounting. When specified in the test procedure, the chip resistor shall be mounted on a test board as specified on [figure 3a](#), and [figure 3b](#) using test substrates as described in [4.8.1.3.1](#), [4.8.1.3.2](#), or [4.8.1.3.3](#). The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip resistor in any of the tests for which it may be used. The test board shall be prepared with metallized surface land areas of proper spacing so that a test board surface area of at least four times the resistor chip surface area is provided for each resistor chip mounted. The metallized surface land areas shall be designed in a pattern to accommodate a number of resistor chips. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. The resistor orientation for mounting shall be in the usual configuration with the resistor element facing away from the test board (e.g., no “flip chip” or “tombstone” allowed). The mounting shall be done by soldering the chip terminations directly to the test board metallized land areas in the following manner:

- a. Solder and soldering flux shall be of such a quality as to enable the chip resistors to meet all the requirements of this specification and shall be applied to the terminations of each chip of code letters B and G (see [1.2.4](#)).
- b. All chips shall be placed across the metallized land areas of the test board with contact between the chip termination's and board land areas only. The use of adhesive to keep chips in place during mounting operation is allowable except for preparation of solder mounting integrity test pieces.
- c. For load life, the test board, with all chips in position, shall be placed on a heat transfer unit (molten solder, hot plate, tunnel oven, etc.) with suitable time and temperature to assure proper reflow mounting.

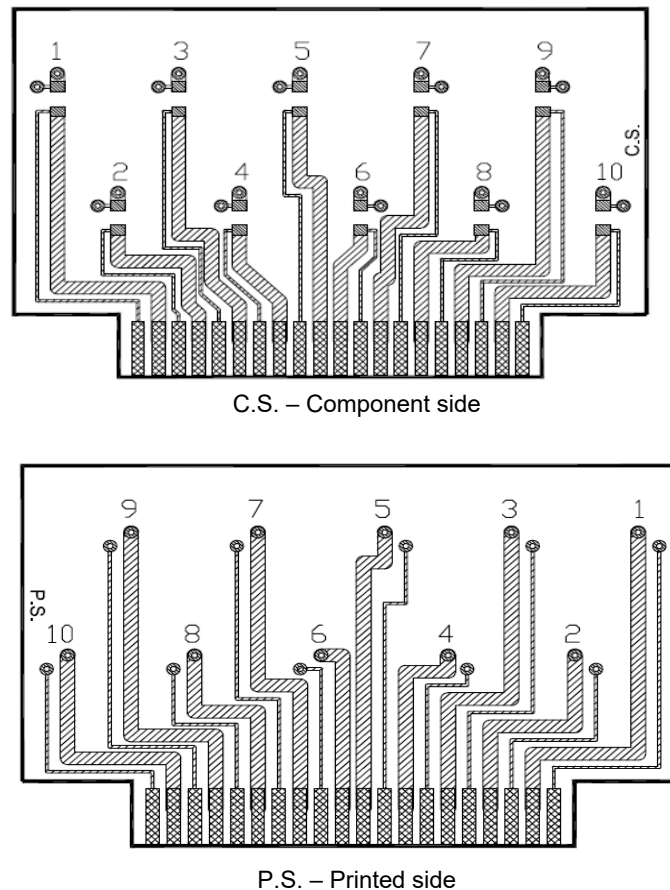


FIGURE 3a. Suggested test board (fiberglass, polyimide)

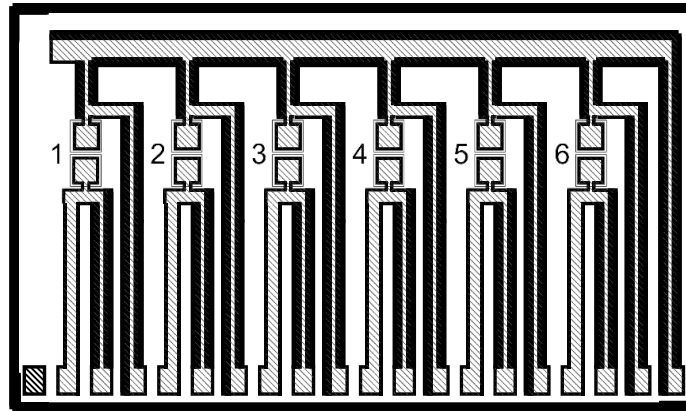


FIGURE 3b. Suggested test board (ceramic)

NOTES:

1. Suggested fiberglass test board (e.g., G30 or FR-4, glass epoxy): 1.000 inch (25.40 mm) x 1.500 inch (38.10 mm) x 0.0625 inch thick (1.5875 mm).
2. Suggested high temperature test board (e.g. Polyimide) shall have the same dimensions as in Note 2.
3. Suggested ceramic test board (e.g., 92-96 percent alumina): 1.000 inch (25.40 mm) x 2.000 inch (50.80 mm) x 0.025 inch (0.64 mm) thick.
4. The contacts fit a printed circuit board connector with 0.100 inch (2.54 mm) in contact center, appropriate for 4-terminal measurements.
5. A larger test board, to suitable scale, may be used to accommodate additional test samples or additional style/size configurations.

4.8.1.3.1 Fiberglass base board. Fiberglass base boards can be FR-4, G-10, G-30, or equivalent. A fiberglass test board, with copper lamination, shall be used for testing and the copper lamination shall be 70 micrometers copper (2 oz.) thickness (maximum).

4.8.1.3.2 Polyimide board. Polyimide (PI) board can be 33N, 85N or equivalent. A PI test board, with copper lamination, shall be used for testing and the copper lamination shall be 70 micrometers copper (2 oz.) thickness (max).

4.8.1.3.3 Ceramic board. Ceramic board can be 92 to 96 percent alumina, 0.020 to 0.025 inch thick. A ceramic test board, with printed silver conductors, shall be used for testing and the conductor layer shall be 15 micrometers thickness (max).

4.8.2 DC resistance. The DC resistance shall be measured in accordance with [MIL-STD-202-303](#). The following details and exceptions shall apply:

- a. Measuring apparatus: Different types of measuring test equipment (multimeters, bridges, or equivalent) are permitted to be used on the initial and final readings of this test, provided the equipment is the same type, model, or if it can be shown that the performance of the equipment is equivalent or better.

MIL-PRF-32663
w/AMENDMENT 1

- b. Test voltage for bridges: Measurements of resistance shall be made by using the test voltages up to the maximum values specified in table XIV. The test voltage chosen, whether it is the maximum or a lower voltage which would still provide the sensitivity required, shall be applied across the terminals of the resistor. This same voltage shall be used whenever a subsequent resistance measurement was made.
- c. Measurement energy for electronic test equipment: The measurement energy applied to the unit under test shall not exceed 10 percent of the 25°C rated wattage times 1 second.
- d. Temperature: Unless otherwise specified herein, the temperature at which subsequent and final resistance measurements are made in each test shall be within $\pm 2^{\circ}\text{C}$ of the temperature at which the initial resistance measurement was made.

TABLE XIV. Standard DC resistance test voltages.

Nominal resistance	Maximum test voltage			
	10 to 24 milliwatts	25 to 99 milliwatts	100 to 225 milliwatts	226 to 1,000 milliwatts
<u>ohms</u>	<u>Volts</u>	<u>Volts</u>	<u>Volts</u>	<u>Volts</u>
1 to 9.88	0.2	0.3	0.7	1.0
10 to 98.8	0.3	0.3	1.0	1.0
100 to 988	1.0	1.0	1.0	3.0
1,000 to 9,880	3.0	3.0	3.0	10.0
10,000 to 98,880	10.0	10.0	10.0	30.0
100,000 or higher	30.0	30.0	30.0	100.0

4.8.3 Thermal shock (see [3.9](#)). Resistors shall be tested in accordance with [MIL-STD-202-107](#). The following details and exceptions apply:

- a. Mounting:
 - (1) For qualification (space level only) and group C inspection, resistors shall be mounted on a test board as specified in [4.8.1.3](#):
 - "B" termination parts shall be mounted on fiberglass boards as specified in [4.8.1.3.1](#).
 - "G" termination parts shall be mounted on polyimide boards as specified in [4.8.1.3.2](#).
 - (2) For group A inspection, resistors shall not be mounted. Resistors may be placed in metal baskets, vials, or other apparatus as long as resistors are subjected to the specified temperature extremes.
- b. Measurement before thermal shock cycling:
 - (1) Qualification test: DC resistance shall be measured as specified in [4.8.2](#). The DC resistance shall be within the specified resistance tolerance of the nominal resistance value.
 - (2) Group A test: DC resistance shall be measured as specified in [4.8.2](#).
 - (3) Group C test: DC resistance shall be measured as specified in [4.8.2](#).
- c. Test condition F (except temperatures shall be 150°C +10°C, -0°C and -65°C +0°C, -10°C in both cases). For space level qualification the test condition shall be F-3 and temperatures as specified herein.

MIL-PRF-32663
w/AMENDMENT 1

d. Measurement after thermal shock cycling:

- (1) Qualification test: After stabilization at room temperature, the DC resistance shall be measured as specified in [4.8.2](#).
- (2) Group A test: At the option of the manufacturer, the DC resistance may be measured after thermal shock, but the acceptance criteria shall be based only on the combined effects of thermal shock, short time overload and power conditioning (see [3.11](#)).
- (3) Group C test: After stabilization at room temperature, the DC resistance shall again be measured as specified in [4.8.2](#) (on mounted resistors).

4.8.4 Short time overload (see [3.10](#)). For group A inspection, chip resistors shall be tested unmounted (after thermal shock). For group C inspection, chip resistors shall be tested mounted on test board (after low temperature operation).

a. Initial measurements:

- (1) Group A test: Initial DC resistance shall be measured as specified in [4.8.2](#) before thermal shock.
- (2) Group C test: Initial DC resistance shall be measured as specified in [4.8.2](#) on mounted resistors.

b. Operating condition: In still air, with no circulation other than created by the heat of the resistors being operated, a DC test potential, 2.5 times the rated continuous working voltage but not exceeding twice the maximum voltage (see [3.1](#)), shall be applied for 5 seconds to the resistor under the following conditions:

- (1) Unmounted resistors (Group A) shall be placed in a supporting fixture/jig and no forced air cooling will be utilized.
- (2) Resistors on test board (Group C) shall be mounted in accordance with [4.8.1.3](#).

c. Inspection after test:

- (1) Group A test: The resistors shall be stabilized at room temperature after which the DC resistance shall be measured as specified in [4.8.2](#); the final measurement shall be made after power conditioning test.
- (2) Group C test: The resistors shall be stabilized at room temperature after which the DC resistance shall be measured as specified in [4.8.2](#).

4.8.5 Power conditioning (see [3.11](#)). Chip resistors shall be tested in accordance with [MIL-STD-202-108](#). The following details and exceptions shall apply:

- a. Test temperature and tolerance: 70°C +5°C, -0°C.
- b. Initial measurements: At the option of the manufacturer, the DC resistance may be measured before power conditioning. In such case, measurements shall be made outside the chamber at room temperature. This measurement shall be used as the reference temperature for all subsequent measurements under the same condition.
- c. Operating condition: A DC voltage or filtered or nonfiltered full-wave rectified AC voltage shall be applied to the chip resistor intermittently, one and one-half hours "on" and one-half hour "off", for 100 hours ±4 hours and at the test temperature. During the "on" cycle, the voltage shall be regulated and controlled to maintain ±5 percent of the required test voltage. Unless otherwise specified (see [3.1](#)), power applied shall be one and one-half times rated power (at +70°C) not to exceed maximum voltage for the style. For B termination chip resistors, at no time during the test shall the resistor element temperature exceed 150°C. Adjust the ambient temperature, when necessary, in order to accomplish this.

MIL-PRF-32663
w/AMENDMENT 1

- d. Measurements after test: Following a thirty minute minimum stabilization period, DC resistance shall be measured as specified in [4.8.2](#). The acceptance criteria shall be based on the combined effects of thermal shock, short time overload and power conditioning.
- e. Inspection after test: Chip resistors shall be inspected in accordance with [4.8.1.1](#).

4.8.6 Low temperature operation (see [3.12](#)). A DC resistance measurement shall be made as specified in [4.8.2](#), mounted on a test board as specified in [4.8.1.3](#). The resistors shall be placed in a cold chamber maintained at -65°C +0°C, -5°C. After stabilization at this temperature, full rated continuous working voltage as specified in [3.7](#) shall be applied for 45 minutes +5 minutes, -0 minutes. Fifteen minutes +5 minutes, -0 minutes after the removal of the voltage, the resistors shall be removed from the chamber and stabilized at room temperature; the DC resistance shall be measured as specified in [4.8.2](#).

4.8.7 High temperature exposure (see [3.13](#)). Resistors shall be mounted on a test board as specified in [4.8.1.3](#), B termination parts – on a fiberglass board, G termination parts – on polyimide or ceramic board. Then the DC resistance shall be measured as specified in [4.8.2](#). The resistors shall then be subjected to a continuous temperature of 150°C ±5°C (200°C ±5°C for G termination) or as specified in applicable specification sheet (see [3.1](#)) for a period of 100 hours ±4 hours, in a test chamber with forced air circulation. The resistors shall be stabilized at room temperature after which the DC resistance shall be measured as specified in [4.8.2](#).

4.8.8 Resistance to solder heat (see [3.14](#)). Resistors shall be tested in accordance with [MIL-STD-202-210](#). The following details and exceptions shall apply:

- a. Measurement before test: DC resistance shall be measured as specified in [4.8.2](#).
- b. Mounting: “B” termination resistors shall be mounted on a fiberglass test board and “G” termination resistors shall be mounted on polyimide or ceramic test board as specified in [4.8.1.3](#). The test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, tunnel oven, etc.) with the temperature transitioned to 245°C ±5°C for B termination and 275°C ±5°C for G termination. The chips shall remain at the specified temperature until the solder melts and reflows forming a homogenous solder bond. This mounting procedure shall be considered one heat cycle.
- c. Second heat cycle: Test condition J, except this is the last heat cycle. For G termination, the component temperature shall be 260°C ±5°C for 30 seconds ±5 seconds. (NOTE: When a hot plate is used, the temperature shall be 245°C ±5°C for 60 seconds ±5 seconds for B termination, 275°C ±5°C for 60 seconds ±5 seconds for G termination and the temperature ramp and emersion/immersion rate does not apply).
- d. Measurement after test: After completion of the cleaning process and following a stabilization period at room temperature the DC resistance shall be measured as specified in [4.8.2](#).

4.8.9 Moisture resistance (see [3.15](#)). Resistors shall be tested in accordance with [MIL-STD-202-106](#). The following details and exceptions shall apply:

- a. Mounting: Chip resistor sample units shall be mounted on a test board as specified in [4.8.1.3](#) - B termination resistors on a fiberglass test board and G termination on a polyimide test board.
- b. Initial measurement: After stabilizing at room temperature following the initial conditioning period DC resistance of each chip on the test board shall be measured as specified in [4.8.2](#).
- c. Polarization and loading voltage: No polarization voltage shall be applied. Loading voltage: a DC voltage equivalent to 0.1 of rated power not to exceed the maximum rated voltage (see [3.1](#)) shall be applied to all samples on test.

MIL-PRF-32663
w/AMENDMENT 1

- d. Subcycle: Step 7b shall not be applicable. Step 7a shall be performed during any five of the first nine cycles only.
- e. Measurements at high humidity: None.
- f. Final measurements: Upon completion of step 6 of the final cycle, the resistors shall be removed from the chamber and air dried at room temperature for 15 minutes to 120 minutes. The DC resistance shall then be measured in accordance with 4.8.2.

4.8.10 Resistance temperature characteristic (see 3.16). Resistors shall be tested in accordance with MIL-STD-202-304. The following details and exceptions shall apply:

- a. Test temperature: In accordance with table XV.
- b. Accuracy of temperature measurement: Resistors shall be maintained for thirty minutes +90 minutes, -15 minutes within 3°C at each of the test temperatures listed in table XV. This tolerance shall be maintained on the established test temperatures.
- c. Mounting: Resistors shall be mounted on a test board as specified in 4.8.1.3 – termination B parts on fiberglass test board and termination G parts on polyimide board.
- d. The DC resistance shall be measured in accordance with 4.8.2.

As an option, the manufacturer may develop a control procedure for minimum stabilization times required for RTC testing. This procedure shall detail specific time elements required to reach thermal and electrical stability for specific part designs. Upon approval by the qualifying activity, the manufacturer may use this procedure for minimum stabilization times for RTC testing.

TABLE XV. Resistance temperature characteristic.

Sequence	Temperature <u>1/</u> °C
1	<u>2/</u> 25 ±3
2	-55 ±3
3	<u>2/</u> 25 ±3
4	125 ±3
5 <u>3/</u>	200 ±3

1/ At the option of the manufacturer, the reverse sequence may be as follows:

- 1- 2/ 25°C ±3°C
- 2 - 200°C ±3°C
- 3 - 125°C ±3°C
- 4 - 2/ 25°C ±3°C
- 5 - -55°C ±3°C

2/ This temperature shall be considered the reference temperature for each of the succeeding temperatures.

3/ This temperature is applicable for resistors with G termination only.

4.8.11 Life test (see 3.17). Resistors shall be tested in accordance with MIL-STD-202-108. The following details and exceptions shall apply:

- a. Method of mounting: Chip resistor sample units shall be mounted as specified in 4.8.1.3 and in accordance with table XVI.

MIL-PRF-32663
w/AMENDMENT 1

b. Test temperature and tolerance:

- (1) Qualification and FR level maintenance +70°C ±5°C
- (2) +125°C power rating +125°C ±5°C

c. Initial resistance measurement of mounted resistors: Measurements may be made inside or outside the chamber. The DC resistance shall be measured in accordance with 4.8.2.

- (1) Inside chamber: When measurements are to be made inside the chamber, the initial DC resistance shall be measured (see 4.8.2) after mounting at the applicable test temperature, after a thirty minutes +90 minutes, -15 minutes stabilization period, and within 8 hours of exposure of the resistors to the test temperature. This initial measurement shall be used as the reference DC resistance for all subsequent measurements under the same condition.
- (2) Outside chamber: When measurements are to be made outside the chamber, the initial DC resistance shall be measured (see 4.8.2) after mounting at room temperature. This initial measurement shall be used as the reference DC resistance for all subsequent measurements under the same condition.

d. Operating conditions: DC continuous working voltage, or filtered or non-filtered full wave rectified ac voltage, in accordance with power conditions in table XVI, shall be applied intermittently, 90 minutes "on" and 30 minutes "off", for the applicable number of hours (see 4.8.11f (2)) and at the applicable test temperature. "On time" shall be three quarters of the total elapsed time. During the "on" cycle, the voltage shall be regulated, and controlled to maintain ±5 percent of the rated continuous working voltage.

TABLE XVI. Test Board and Operating Conditions for Assorted Life Tests.

Termination	Test Type	Temperature	Power	Test board	Hours
B	Qualification	+70°C	100%	Fiberglass	2000
B	FRL	+70°C	100%	Fiberglass	10000
G	Qualification	+70°C	100%	Ceramic	2000
G	FRL	+70°C	100%	Ceramic	10000
G	Qualification	+125°C	60%	Polyimide	2000
G	Qualification	+70°C	see Note 1	Fiberglass	2000

NOTE 1 : For this test only the applied power shall be 100% of the power rating for the B termination of the same chip size/style [For example, a 1206 size "G" termination resistor (0.4 Watts) shall be tested using the "B" termination power rating of 0.25 Watts].

e. Test condition: Two thousand hours elapsed time for qualification inspection (ER only) with all samples continued to 10,000 hours. Ten thousand hours for FRL inspection group C.

f. Measurements during test: The DC resistance shall be measured in accordance with 4.8.2.

- (1) Qualification inspection: DC resistance shall be measured (see 4.8.2) at the end of the 30 minutes "off" periods after 250 hours +72 hours, -24 hours; 500 hours +72 hours, -24 hours; 1,000 hours +72 hours, -24 hours; and 2,000 hours +96 hours, -24 hours have elapsed.
- (2) Extended life testing (as per table XVI): DC resistance shall be measured (see 4.8.2) at the end of the 30 minutes "off" periods after 250 hours +72 hours, -24 hours; 500 hours +72 hours, -24 hours, 1,000 hours +72 hours, -24 hours; and 2,000 hours +96 hours, -24 hours, and every 2,000 hours +96 hours, -24 hours thereafter until the required 10,000 hours +120 hours, -0 hours have elapsed. Measurements shall be made as near as possible to the specified time but may be adjusted so that measurements need not be made during other than normal workdays.

MIL-PRF-32663
w/AMENDMENT 1

- (3) Measurements outside of the chamber: When measurements are made outside the chamber, resistors shall be outside of the chamber, for a minimum of 45 minutes and stabilized at room temperature before measurement.

4.8.12 Solderability (see 3.18). Resistors shall be tested in accordance with [MIL-STD-202-208](#). Both end terminations shall be immersed completely one at a time or both at the same time by dipping the entire chip in the solder pot. The following details and exceptions shall apply:

a. Apparatus:

- (1) A solder pot capable of keeping the solder temperature to $\pm 5^{\circ}\text{C}$ of set point.
- (2) A device to keep the specimen submerged in solder for the required time.
- (3) Optical equipment capable of 30X magnification.
- (4) A laboratory beaker or appropriate laboratory apparatus that is capable of:
 - (a) Supporting a nonmetallic device.
 - (b) Maintaining the test specimens at a distance of 1.50 inches (38.1 mm) to 2.50 inches (63.5 mm) from the surface of the boiling deionized water (DI) or distilled water while, at the same time, exposing them to the full flow of steam generated.

b. The requirement for standard solderable wire application shall not apply.

c. The immersion and emersion rates shall not apply.

d. The specimen shall be totally submerged for at least 5 seconds.

4.8.13 Mounting integrity (see 3.19).

4.8.13.1 Solder mounting integrity (terminations B and G). The resistor chips shall be prepared as specified in [4.8.1.3](#). A force shall be applied to all solderable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The resistor shall be examined for evidence of mechanical damage (see [3.24.2](#)). The pusher width shall be a minimum of 30 percent of the length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table XVII.

TABLE XVII. Solder mounting integrity.

STYLE	FORCE APPLIED (kilograms)
RFB0603 and RFG0603	1.0
RFB0805, RFB1206, RFB1506, RFG0805, RFG1206, and RFG1506	2.0
RFB2010, RFB2512, RFG2010 and RFG2512	3.0

MIL-PRF-32663
w/AMENDMENT 1

4.8.14 Board Flex (see 3.20). Resistors shall be tested in accordance with MIL-STD-202-218 with these exceptions:

- a. Samples. Multiple samples may be tested on a single FR4 board.
- b. Duration of force: 60 seconds minimum while at maximum board deflection.
- c. Measurements during test: After a minimum of 60 seconds at maximum board deflection and while still flexed, DC resistance shall be measured in accordance with 4.8.2.
- d. Measurements after test: After removal of force for board flex test, DC resistance shall be measured again in accordance with 4.8.2.

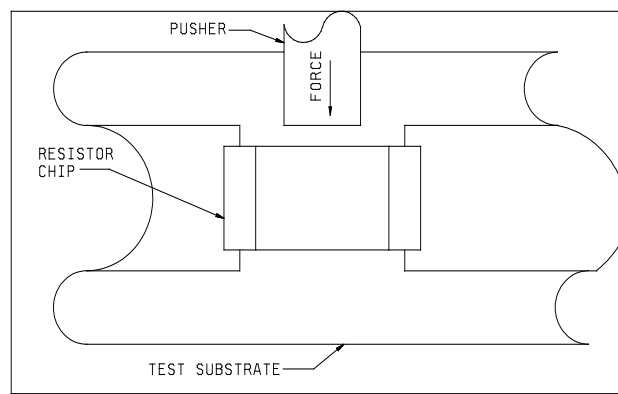


FIGURE 4. Mounting integrity test fixture.

4.8.15 Resistance to solvents (see 3.21). Resistors shall be tested in accordance with MIL-STD-202-215. The following details and exceptions shall apply:

- a. Mounting: Unmounted or mounted.
- b. The marked portion of the resistor shall be brushed.

4.8.16 Laser marking legibility test (see 3.22). Resistors shall be coated with 0.005 inch (0.13 mm) minimum of silicon resin insulated compound, type SR of IPC CC 830. After curing, coated resistors shall be examined for legibility under normal production room lighting by an inspector at 10X magnification.

4.8.17 Outgassing (see 3.25). The resistors organic material shall be tested in accordance with ASTM E595.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military services system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

5.2 Bulk packaging. The use of bulk packaging for chip resistors is prohibited. The use of bulk packaging may cause scratches and/or voids to the terminations, protective coatings, resistive element and/or chipping of the substrate.

MIL-PRF-32663
w/AMENDMENT 1

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The chip resistors covered by this specification are military unique due to the fact that these devices must be able to operate satisfactorily in military systems under the following demanding conditions: 100 cycles of thermal shock at high and low temperature extreme, high temperature for an extended period of time, and low temperature for an extended period of time. In addition, these military requirements are verified under a qualification system and an extended failure rate of 0.001 percent per 1,000 hours. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, date of this specification, the applicable associated specification, and the complete PIN (see [1.2.1](#)).
- b. Unless otherwise specified (see [2.1](#)), the versions of the individual documents referenced will be those in effect on the date of release of the solicitation.
- c. Packaging requirements (e.g., Electrostatic discharge (ESD) sensitivity) (see [5.1](#)).
- d. Allowable substitution (see [3.26.3](#)).
- e. If marking is required (see [3.26](#)).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in Qualified Product List QPL-32663 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products cover by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQP, Post Office Box 3990, Columbus, OH 43218-3990; or by email to vqp.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Application notes.

6.4.1 Mounting of resistors. Resistors may be mounted individually on a test board, and connected to conductor areas by means of solder perform. Users are cautioned that the substrate and chip component must have compatible temperature coefficients of expansion to reduce the strain level imposed on the solder connections.

6.4.2 Stacking of resistors. Stacking is generally discouraged since experience indicates that failure may occur due to electrolytic action in the bonding adhesive. This action occurs from the increase in temperature caused by stacking in conjunction with the operating voltage across the resistor. The bonding adhesive at the resistor chip interface chemically reacts with the active resistor material changing the noise and resistance values and eventually the resistor will open. If stacking resistors, care should be taken to compensate for the lower heat dissipation capabilities by derating the wattage rating.

6.4.3 Close tolerance resistors. Close tolerance resistors (i.e., T and Q) should be mounted on a test board by a method which produces the least heating effect over a short time to avoid permanent changes in resistance.

6.4.4 Resistor element orientation. It is recommended that the element side of resistors with wraparound terminations B and G be mounted up when they are placed onto printed circuit boards.

MIL-PRF-32663
w/AMENDMENT 1

6.4.5 Resistors with gold termination (style RFG).

6.4.5.1 High temperature and/or high power applications. For application temperatures >150°C and /or where the applied power is >50% of the rated power, it is recommended that RFG style resistors with gold (G) terminations be used and solder assembled on polyimide or ceramic boards for better heat dissipation and resistor performance.

6.4.5.2 For use in solder assembly only. The gold termination finish on RFG style resistors is intended for solder assembly only. It is not intended for wire bond or conductive epoxy applications. The amount of gold applied to the terminations is not likely to be sufficient to cause solder joint embrittlement issues in most solder assembly processes. For additional information users may consult their program requirements and applicable workmanship standards, such as [IPC J-STD-001](#).

6.4.6 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of tin containing 3 percent or more lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to [ASTM-B545](#) (Standard Specification for Electrodeposited Coatings of Tin).

6.5 Noise level test. This specification does not include a noise test. If the user requires a noise test, it should be performed in accordance with [MIL-STD-202-308](#).

6.6 Electrostatic charge effects. In general, the bulk metal foil resistors are non-sensitive to electrostatic charge. However, common rules of handling with small electronic components should be followed. Direct shipments to the Government are controlled by [MIL-DTL-39032](#) which specifies a preventive packaging procedure.

6.7 Pulse applications. Designers are CAUTIONED on using these resistors in high power pulse applications. Since they have not been qualified nor tested for such applications, damage and premature failure are possible. These resistors only see a five second short time overload (see [4.8.4](#)) as part of the group A inspection of this specification.

6.8 Subject term (key word) listing.

Failure rate
Hybrid circuits
Surface mount
Termination

APPENDIX A

PROCEDURES FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix covers the procedure for qualification inspection of resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance. This appendix also outlines the procedure for extending qualification to the various product levels as well as the resistance range, characteristics, tolerances, and FRLs.

A.2 APPLICABLE PUBLICATIONS. This section is not applicable to this document.

A.3 SUBMISSION

A.3.1 Product levels. Qualification of the T (space) level is predicated upon meeting the ER qualifications requirements for FRL R or S (see [A.4.1](#)). To obtain qualification to the T (space) level, the manufacturers shall use the existing ER FRL (R, S, U, or V) design, and meet the additional requirements for outgassing and the 100 cycle thermal shock test (see A.3.2) as well as been approved by the qualifying activity on the capability to conduct tests and examinations for the space level product (e.g., production lot formation). The procedure for submitting samples to become qualified to the initial FRL M is specified in A.3.2.

A.3.2 Sample.

A.3.2.1 Qualification of "B" termination resistors. A sample consisting of 162 sample units, 54 of the lowest, 54 of the highest, and 54 of the critical or nearest to critical value (see [table A-I](#)), and in each style and characteristic, termination material, and resistance tolerance for which qualification is sought, shall be submitted to groups II, III, IV, for normal ER qualification of [table VIII](#). In addition, 50 samples of any value (10 for group V, 20 for group VI and 20 for group VII) shall be submitted. If applying for space level qualification an additional 30 samples (10 of the lowest, 10 of the highest, and 10 of the critical) shall be submitted to group VIII of [table VIII](#). If qualification to a tighter resistance tolerance than submitted above is desired, 30 additional sample units of the tighter resistance tolerance shall be subjected to the following tests (see [table A-II](#)). After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification to the qualifying activity.

- Notes:
1. If critical value isn't applicable for the specific product style, the total number of samples in each group shall be divided into 2 equal parts (highest and lowest values).
 2. If manufacturer is qualifying resistors with ink marking and also with laser marking methods, the entire qualification sample will be divided into two equal parts in each testing group, except for groups V and VI, where units marked with one of the methods can be used.
 3. If parts are marked with color dots or screen printed characters, 10 samples shall be submitted to Resistance to solvents (Group VII) test only.

A.3.2.2 Qualification of "G" termination resistors. Sample described in A.3.2.1, shall apply for "G" termination resistors' qualification. The units shall be mounted on a polyimide board or ceramic substrate as described in the relevant test method. Also, 102 sample units mounted on polyimide tests board shall be submitted to group IVa test of [table VIII](#). Additional 162 sample units, 54 of the lowest, 54 of the highest, and 54 of the critical or nearest to critical value, mounted on FR4 test board, shall be submitted to following tests: 102 units to group IVb, 30 units to group VIII of [table VIII](#), and 30 pcs to subgroup 2 of [table XIII](#) Monthly Inspection.

APPENDIX A

A.3.2.3 Qualification to extended resistance ranges. For qualification to the extended resistance ranges of higher resistance tolerances, 54 additional samples of high or low resistance shall be subjected to the tests of group I, group II, group III, and group IV of [table VIII](#).

A.3.3 Outgassing (space level only). Manufacturers shall validate, to the qualifying activity, the outgassing requirements as specified in [3.25](#).

TABLE A-I. Power rating, maximum working voltage, and critical resistance values. [1/](#) [2/](#)

STYLE	SLASH SHEET	CRITICAL RESISTANCE VALUE	RATED POWER (milliwatts) 3/		MAX WORKING VOLTAGE (Volts)
			Ceramic or Polyimide	FR4	
RFB0603	1	N/A	75	75	25
RFB0805	2	N/A	150	150	40
RFB1206	3	N/A	250	250	90
RFB1506	4	N/A	300	300	110
RFB2010	5	N/A	400	400	190
RFB2512	6	N/A	500	500	306
RFG0603	7	N/A	100	75	25
RFG0805	8	N/A	225	150	40
RFG1206	9	N/A	400	250	90
RFG1506	10	N/A	450	300	110
RFG2010	11	N/A	600	400	190
RFG2512	12	N/A	800	500	306

[1/](#) Maximum continuous working voltage shall be applied (see [3.1](#)).

[2/](#) The critical resistance value is the maximum standard resistance value which will dissipate full wattage when the maximum continuous working voltage is applied.

[3/](#) Resistors with G termination shall be mounted on ceramic or polyimide boards in order to carry the specified power. Otherwise, the power rating shall be reduced to that assigned to the "B" termination resistor of the same size.

TABLE A-II. Sample size for qualification inspection.

Inspection	Requirement paragraph	Method paragraph	Number of sample units for inspection	Number of defectives allowed
Visual and mechanical inspection	3.1 , 3.4 , 3.5 , 3.5.1 through 3.5.4 inclusive, 3.24 and 3.27	4.8.1	30 10 highest 10 critical 10 lowest	0
DC resistance	3.8	4.8.2		
Thermal shock	3.9	4.8.3		
Short time overload	3.10	4.8.4		
Power conditioning	3.11	4.8.5		

APPENDIX A

A.4 EXTENT OF QUALIFICATION

A.4.1 Extent of qualification. The resistance range included in the qualification of any one style and tolerance shall be between any two adjacent resistance values which pass the required qualification inspection. The extent of qualification between styles, characteristics, termination's, FRLs, and resistance tolerances shall be as specified in table A-III.

TABLE A-III. Extension of qualification.

Style	Will qualify style <u>1/</u>
RFB2512	RFB2512, RFB2010, RFB1506, RFB1206, RFB0805, RFB0603
RFB2010	RFB2010, RFB1506, RFB1206, RFB0805, RFB0603
RFB1506	RFB1506, RFB1206, RFB0805, RFB0603
RFB1206	RFB1206, RFB0805, RFB0603
RFB0805	RFB0805, RFB0603
RFB0603	RFB0603
RFG2512	RFG2512, RFG2010, RFG1506, RFG1206, RFG0805, RFG0603
RFG2010	RFG2010, RFG1506, RFG1206, RFG0805, RFG0603
RFG1506	RFG1506, RFG1206, RFG0805, RFG0603
RFG1206	RFG1206, RFG0805, RFG0603
RFG0805	RFG0805, RFG0603
RFG0603	RFG0603
Characteristic	Will qualify characteristic
C	C, D, E
D	D, E
E	E
Termination	Will qualify termination
B	B
G	G
Product level	Will qualify product level
T	T
S & V	S, V, R, U, P, M
R & U	R, U, P, M
P	P, M
M	M
Resistance tolerance	Will qualify resistance tolerance
T	T, Q, A, B, C, D, F
Q	Q, A, B, C, D, F
A	A, B, C, D, F
B	B, C, D, F
C	C, D, F
D	D, F
F	F

1/ The same design and technology must be utilized for the style qualified and the styles that the qualification is extended to.

APPENDIX B

VISUAL INSPECTION

B.1 SCOPE

B.1.1 Scope. This appendix details the procedure for visual inspection of chip resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

B.2 APPLICABLE PUBLICATIONS

This section is not applicable to this appendix.

B.3 PRECAP VISUAL INSPECTION

B.3.1 SCOPE. This appendix details the procedure for precap visual inspection of chip resistors covered by this specification.

B.3.2 INSPECTION

B.3.2.1 Manufacturer inspection. Inspection shall be performed using microscope with 50X magnification as an in-process precap visual inspection after trimming and prior to external overcoat application while the resistor element is visible.

B.3.3 Terminal pads defects. Any resistor which exhibits the following defects in the metallization shall not be acceptable.

B.3.3.1 Terminal pads scratches. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.

a. Reject any scratch exposing underlying resistor material or substrate, leaves < 50% of the original width remaining (see figure B-1).	Reject any exposed underlying resistor material or substrate or when $x > \frac{1}{2} w$.  FIGURE B-1. <u>Terminal pads scratches</u>.
--	--

B.3.3.2 Terminal pads voids. A void is defined as any region-where the underlying resistive material or substrate is exposed which is not caused by a scratch.

a. Reject voids which leaves < 50% of the original width (see figure B-2).	Reject voids when $x > \frac{1}{2} w$.  FIGURE B-2. <u>Terminal pads voids</u>.
--	---

APPENDIX B

b. Reject voids larger than 5% of each terminal pad area (see figure B-3).	Reject voids occupying more than 5% of each terminal pad area.  FIGURE B-3. <u>Voids larger than 5% of the terminal pad.</u>
---	--

B.3.4 Resistor element features. Resistor elements are to be examined using microscope with top and bottom illumination.

B.3.4.1 Resistor element nonadherence. Reject any foil lifting and/or peeling.

a. Reject any foil lifting / peeling (see figure B-4).	 FIGURE B-4. <u>Peeling foil exposing substrate.</u>
---	--

B.3.4.2 Features not to be inspected. Features that will not be inspected are voids, notches, bridges, damaged lines, trimming defects. They shall be screened out by in-process screening (see 4.6.3.1.1).

B.3.5 Coating defects. Protective coating is applied over the resistor element for mechanical and environmental protection.

a. Reject any void/crack in the passivation exposing underlying resistor element (see figure B-5).	 FIGURE B-5. <u>Protective coating exposing underlying resistor element.</u>
---	---

APPENDIX B

B.4 FINAL VISUAL INSPECTION

B.4.1 Scope. This appendix details the procedure for visual inspection of terminations (conductor metallization), external overcoat and substrate defects, etc., of chip resistors covered by this specification.

B.4.2 INSPECTION

B.4.2.1 Manufacturer inspection. Inspection shall be performed using microscope with 30X minimum magnification.

B.4.3 Termination defects. Any resistor which exhibits the following defects, in the active circuit metallization, shall not be acceptable. The active circuit metallization is all-metal used for continuity and/or to provide electrical interconnection between distinct elements of the resistor construction.

B.4.3.1 Termination scratches. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.

a. Reject any scratch exposing any of the sublayers of the termination or substrate or leaves < 50% of the original width remaining (see figure B-6). Note: This criteria applies to all surfaces of termination.	Reject any exposed underlying resistor material or when $x > \frac{1}{2} w$.  FIGURE B-6. <u>Termination scratches</u>.
--	--

B.4.3.2 Termination voids. A void is defined as any region-where the sublayers of the termination or substrate are exposed which is not caused by a scratch.

a. Reject voids which leaves < 50% of the original width (see figure B-7). Note: The criteria apply to all termination surfaces.	Reject voids when $x > \frac{1}{2} w$.  FIGURE B-7. <u>Termination voids</u>.
---	---

APPENDIX B

b. Reject voids larger than 5% of the conductor area of each surface (see figure B-8).	Reject voids occupying more than 5% of each terminal pad area.  FIGURE B-8. <u>Voids larger than 5% of the terminal pad.</u>
d. Reject voids that reduce the connection between conductor surfaces to less than 75% of the original width (see figure B-9).	Reject voids reducing the connection between conductor surfaces when $y < \frac{3}{4}d$.  FIGURE B-9. <u>Termination void reduces connection between conductor surfaces.</u>

B.4.3.3 Termination nonadherence. Termination nonadherence is defined as any evidence of metallization lifting, peeling, or blistering.

a. Reject any lifting, peeling, or blistering (see figure B-10).	Reject any lifting, peeling, or blistering.  FIGURE B-10. <u>Termination nonadherence.</u>
---	--

B.4.4 Conductor metallization protrusions. Conductor metallization protrusion defects are defined as extraneous metallization extending beyond the metallization patterns designed edge.

a. Reject protrusions or buildup on the surface of the conductor metallization that extends greater than 3 mils beyond the average thickness of the metallization (see figure B-11).	Reject protrusions or buildup on the surfaces when $y > 3$ mils.  FIGURE B-11. <u>Conductor metallization protrusions or build up on the metallization surface.</u>
---	---

APPENDIX B

B.4.5 Substrate defects.

- a. Reject cracked or chipped substrate. However, small chips on the edges of the substrate are permissible as long as they do not extend under the resistive pattern (see figure B-12).



FIGURE B-12. Substrate crack.

B.4.6 Metal residues or extraneous termination material.

- a. Reject for any metal particle detectable under 30X magnification on the overcoat of resistor chip or on the substrate. (see figure B-13).



FIGURE B-13. Metal particle on the passivation.

B.4.7 Top Coating Defects. Protective top coating is applied over the resistor element for mechanical and environmental protection.

- a. Reject for top coat damage exposing underlying resistor element (see figure B-14).



FIGURE B-14. Top coat exposing underlying resistor element.

APPENDIX C

PROCEDURE FOR FOIL INGOT CLASSIFICATION

C1 SCOPE

C.1.1 Scope. This appendix details the procedure for qualification and verification of “Particle free” foil used for manufacturing of chip resistors covered by this specification (see 3.4). “Particle free” foil is NiCr based foil that doesn’t contain aluminum-based, zirconium-based (Zr) or other embedded particles. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

C.2 APPLICABLE PUBLICATIONS

This section is not applicable to this appendix.

C.3 EQUIPMENT AND PROCEDURES

C.3.1 Equipment.

C.3.1.1 Optical equipment. Microscope 40x, top and bottom light shall be used for chips’ gross visual inspection.

C.3.1.2 Classification. Scanning electron microscope in conjunction with energy dispersive X-ray spectroscopy module (SEM-EDS) shall be used for foil ingot classification.

C.3.2 Sample preparation. The following sample description shall be used. Alternate samples may be used with approval of the qualifying activity.

C.3.2.1 Plates. Produce plates (e.g., 4” x 5”) with resistor patterns of 210 mils x 190 mils size, value 100k ohms from NiCr foil of thickness 100μ” nominal. Manufacturing shall be ended by etching process—no overcoat to be applied.

C.3.2.2 Two plates. Two plates that successfully passed gross visual inspection (general overview) at 40x magnification, shall be submitted to foil ingot classification procedure.

C.3.3 Method.

C.3.3.1 Select. Select 1 of the 2 plates at random for the following inspection. The 2nd plate shall be reserved for inspection only if necessary based on results of inspection of the 1st plate.

C.3.3.2 Analyze. Analyze one region at random in each of eight general areas of a resistor (See Figure C-1). Perform analysis on 40 different resistors for a total of 320 regions. Analyze for embedded particles greater than 1 μm in size.

C.3.4 Qualification steps.

C.3.4.1 Initial Ingot qualification. Prior to use in the product all new bulk metal foil ingots shall be qualified for “Particle-Free” via one-time inspection in accordance with Appendix C.

C.3.4.2 Ingot verification. Each first commercial shipment of new batches of a qualified foil ingot shall undergo the verification process that is identical to the Initial Qualification procedure.

APPENDIX C

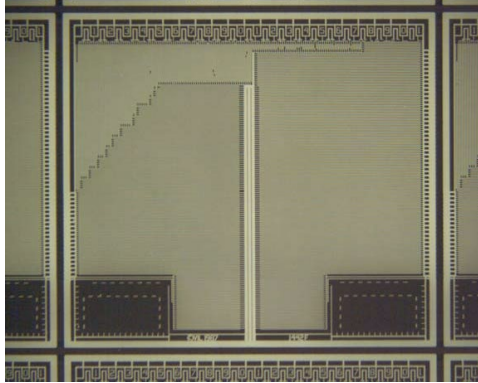


FIGURE C-1. Photograph of one foil resistor on a plate (within dark border).

C.3.5 Procedure. Select 1 of the 2 plates (see [C.3.2.1](#)).

- a. Position the viewing area at a random point within one of the eight general areas of a resistor.
- b. Adjust the magnification of the SEM to a level less than 200X (level at which detail of foil path and particles cannot be observed).
- c. Randomly adjust the X and Y positions of the SEM stage.
- d. Increase the magnification to 3500X without further adjustment of the stage.
- e. Adjust the position of the viewing area in the direction where a greater amount of foil grid line area is observed. Adjust the position such that two adjacent gridlines are centered within the viewing area (see [Figure C-2](#) and [Figure C-3](#)).
- f. Count the number of embedded particles within each of the size ranges 1-2 μm , 2-3 μm , 3-4 μm , 4-5 μm and >5 μm .
- g. Perform EDS analysis to confirm material composition of particles. To minimize analysis time, not every particle will be analyzed if the total number of particles exceeds 10.
- h. Repeat steps a) through f) for the remaining 7 areas (i.e., total of 8 areas) of the resistor.
- i. Repeat steps a) through h) for a total of 40 resistors.

APPENDIX C

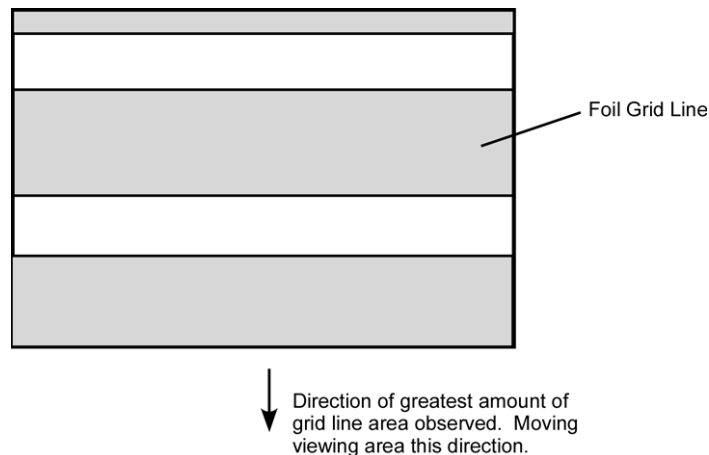


FIGURE C-2. Initial view of foil grid lines when magnification is increased to 3500X.

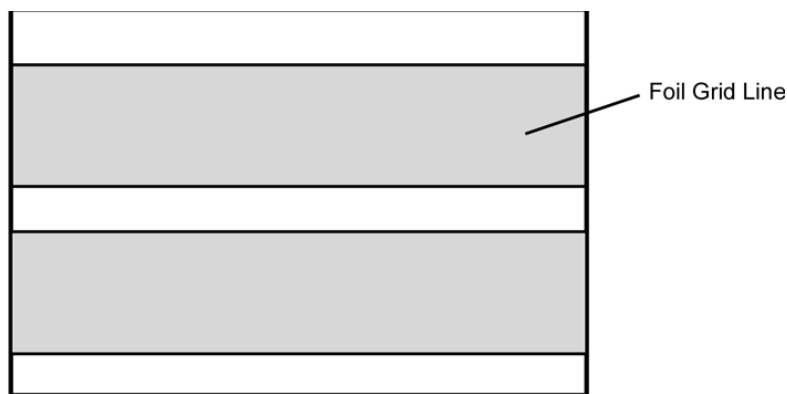


FIGURE C-3. Adjacent foil grid lines centered in viewing area.

C.3.6 Evaluation criteria. When foil is examined for embedded particles of greater than $1\mu\text{m}$ in size, the following acceptance criteria shall apply:

- a. If **No** particles are found, then the Ingot is classified as "Particle Free".
- b. If one particle is found, then the 2nd plate shall be inspected per [C.3.5](#).
- c. If **No** particles are found in the second sample, then the Ingot can be classified as "Particle Free".
- d. If one or more particles are found in the second sample, then the Ingot is not to be classified as "Particle Free" and shall not be used for production of resistors in accordance with this specification.

C.3.7 Records. results of the ingot qualification and verification inspections will be documented and retained in accordance with [MIL-STD-790](#) requirements.

MIL-PRF-32663
w/ Amendment 1

Custodians:

Army - CR
Navy - EC
Air Force - 85
DLA - CC
NASA - NA

Preparing activity:
DLA - CC

Review activities:

Army - AR, AT, CR4, MI
Navy - AS, CG, MC
Air Force - 19
Other - MDA

(Project 5905-2026-007)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.