

The documentation and process conversion measures necessary to comply with this revision shall be completed by 10 August 2023.

INCH-POUND

MIL-PRF-19500/771B
w/AMENDMENT 3
10 May 2023
SUPERSEDING
MIL-PRF-19500/771B
w/AMENDMENT 2
1 February 2022

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY,
DEVICE TYPE 1N7059 (DUAL, CENTER TAP) AND 1N7060 (SINGLE),
QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, Schottky power rectifier diodes in either single or dual center tap configurations. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outlines. The device package outlines are as follows: Bottom pad surface mount device (SMD) TO-276AA (SMD-.5) package in accordance with [figure 1](#) and three terminal flange mount header TO-257AA package in accordance with [figure 2](#).

1.3 Maximum ratings. Unless otherwise specified, maximum ratings ($T_A = +25^\circ\text{C}$).

Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7
Types (1)	V_{RWM}	I_o (1) (2)	I_{FSM} (3) $t_p = 8.3\text{ ms}$, $T_C = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	$R_{\theta JC}$ (3)	T_{STG} and T_J
	V_{dc}	A_{dc}	A (pk)	$^\circ\text{C/W}$	$^\circ\text{C/W}$	$^\circ\text{C}$
1N7059CCT3	60	16	125	1.0	2.0	-65 to +150
1N7060U3	60	30	120	2.0	2.0	-65 to +150

- (1) See temperature-current derating curves in [figures 3](#) and [4](#).
- (2) For each package.
- (3) For each leg, see [figures 5](#) and [6](#).

1.4 Primary electrical characteristics. Unless otherwise indicated, at $T_A = +25^\circ\text{C}$.

$R_{\theta JC} = 1.0^\circ\text{C/W}$ maximum entire package for 1N7059CCT3,
 $R_{\theta JC} = 2.0^\circ\text{C/W}$ maximum entire package for 1N7060U3.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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FSC 5961



MIL-PRF-19500/771B
w/AMENDMENT 3

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN brand and quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet are identified by the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are "7059" and "7060".

1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN for this specification sheet.

1.5.3.1 Schematic designator. The symbol "CC" designates that the circuit schematic for the dual anode, common cathode configuration (1N7059 only). No schematic designator is used for the single anode 1N7060.

1.5.3.2 Package designators. The suffix symbols that designate the package outline for the devices covered by this specification sheet are as follows:

T3	Indicates a three terminal flange mount header TO-257AA package (see figure 2). (1N7059 only).
U3	Indicates a three pad surface mount TO-276AA package (see figure 1). (1N7060 only).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections [3](#) and [4](#) of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections [3](#) and [4](#) of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

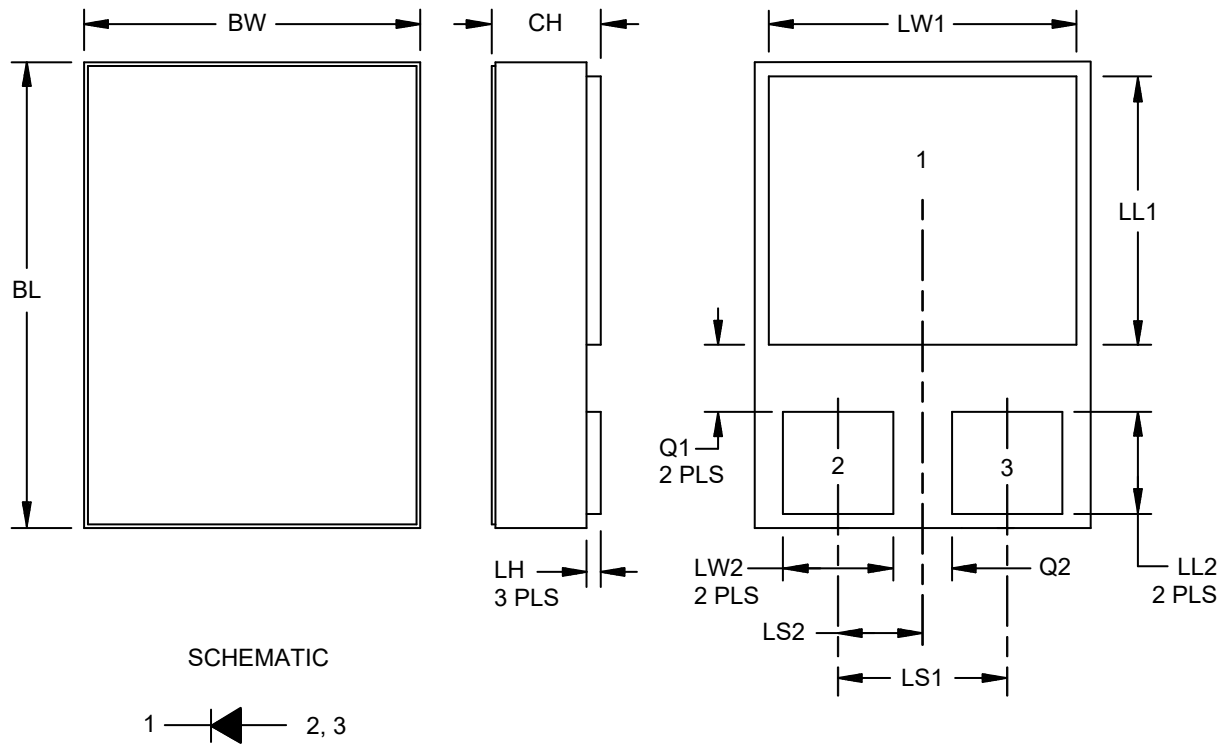
DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

MIL-PRF-19500/771B
w/AMENDMENT 3



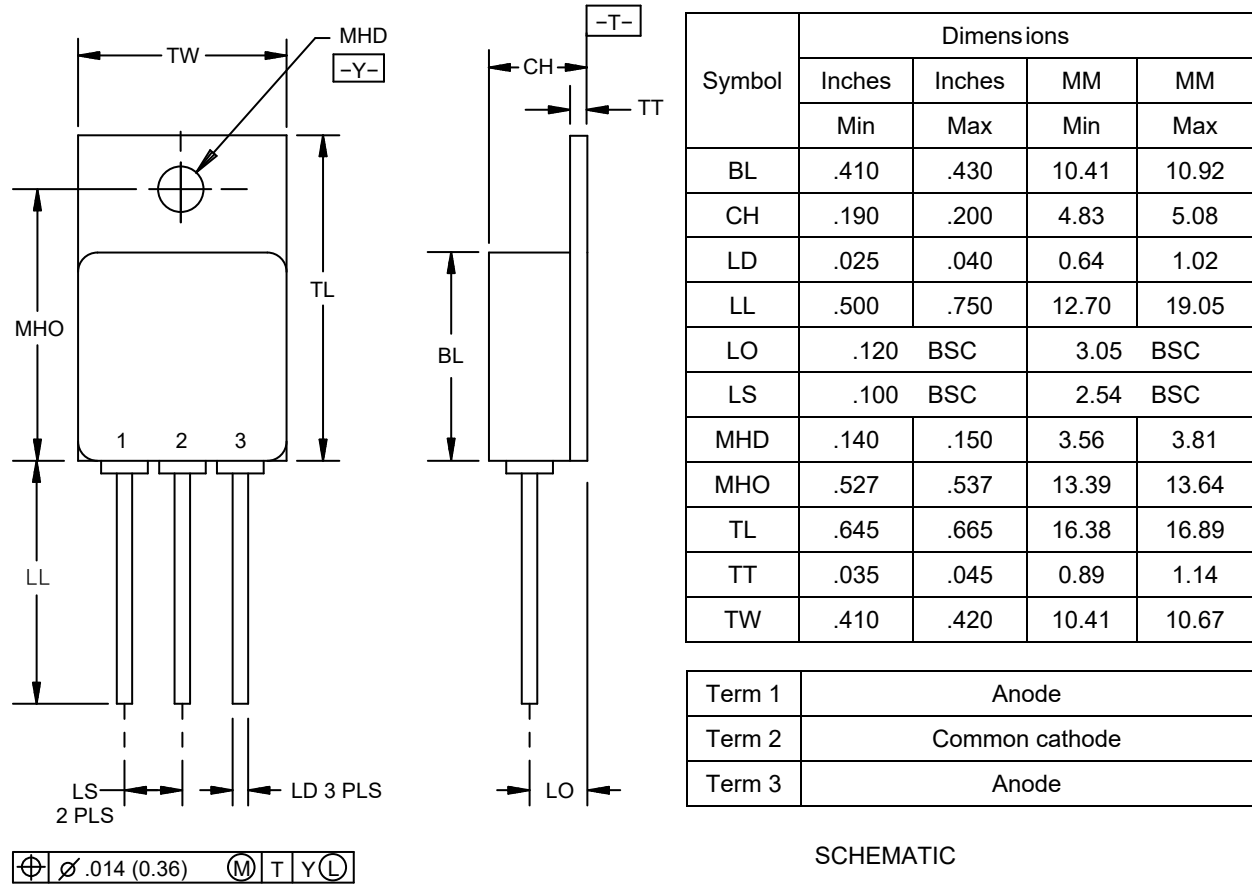
Symbol	Dimensions				Symbol	Dimensions			
	Inches	Inches	MM	MM		Inches	Inches	MM	MM
	Min	Max	Min	Max		Min	Max	Min	Max
BL	.395	.405	10.03	10.29	LS1	.150	BSC	3.81	BSC
BW	.291	.301	7.39	7.65	LS2	.075	BSC	1.91	BSC
CH	.108	.124	2.74	3.15	LW1	.281	.291	7.14	7.39
LH	.010	.020	0.25	0.51	LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84	Q1	.030		0.76	
LL2	.115	.125	2.92	3.18	Q2	.030		0.76	

NOTES:

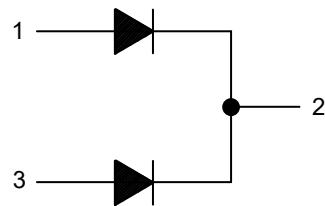
1. Dimensions are in inches. Millimeters are given for general information only.
2. Terminal 1 is cathode. Terminals 2 and 3 are common anode.

FIGURE 1. Dimensions and configuration of TO-276AA (SMD-0.5) package.

MIL-PRF-19500/771B
w/AMENDMENT 3



SCHEMATIC



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Protrusion of ceramic eyelets included in dimension LL.
3. All terminals are isolated from case.

FIGURE 2. Dimensions and configuration of three terminal flange mount header TO-257AA package.

MIL-PRF-19500/771B
w/AMENDMENT 3

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (TO-276AA) and [figure 2](#) (TO-257AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-STD-750](#), [MIL-PRF-19500](#) and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Lead formation (TO-257AA package only). Where a choice of lead formation is desired, it shall be specified in the acquisition document (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of [MIL-PRF-19500](#) and 100 percent dc testing in accordance with [table I](#), subgroup 2 herein after the formation.

3.4.3 Lead isolation (TO-257AA package only). Methods used for electrical isolation of the terminal feed through shall employ materials that contain a minimum of 90 percent ceramic Al_2O_3 or equivalent. Examples of such construction techniques are metalized ceramic eyelets or ceramic walled packages.

3.4.4 Polarity. Polarity and terminal configuration shall be in accordance with [figures 1](#) and [2](#) herein.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#) and herein.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#) and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [tables I](#) and [II](#) herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I](#) and [II](#) herein).

MIL-PRF-19500/771B
w/AMENDMENT 3

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANS, JANTXV and JANTX only). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTX and JANTXV levels
3b	Surge current (see 4.3.1).	Surge current (see 4.3.1).
(1) 3c	Thermal impedance (see 4.3.2).	Thermal impedance (see 4.3.2).
3d	Avalanche energy test (see 4.3.3).	Avalanche energy test (see 4.3.3).
9, 10	Not applicable.	Not applicable.
11	V_{F1} and I_{R1} .	V_{F1} and I_{R1} .
12	See 4.3.4 , 240 hours, minimum.	See 4.3.4 , 48 hours minimum.
13	Subgroups 2 and 3 of table I herein excluding thermal impedance; V_{F1} and I_{R1} , $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 300 μ A, whichever is greater.	Subgroup 2, of table I herein excluding thermal impedance; V_{F1} and I_{R1} ; $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 300 μ A, whichever is greater.
14	Required.	Required.
15	Required.	Not applicable.
16	Required.	Not applicable.

- (1) Thermal impedance and surge current shall be performed any time after screen 3a and before screen 13. Quality levels JANTX and JANTXV do not need to be repeated in screening requirements.
- (2) Surge current shall precede thermal impedance.

4.3.1 Surge current. The surge current test shall be performed in accordance with condition A of method 4066 of [MIL-STD-750](#). The following details shall apply: $I_O = 0$; $V_{RMW} = 0$, one pulse. $I_{FSM} =$ see [1.3](#); $T_A = 25^\circ\text{C}$, $t_p = 8.3$ ms, one minute minimum time between each surge.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , and t_{MD} . See [table III](#), subgroup 4, and [figures 5](#) and [6](#).

4.3.3 Avalanche energy test. The avalanche energy test is to be performed in accordance with method 4064 of [MIL-STD-750](#) using the circuit as shown on [figure 7](#) or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: $I_{AS} = 1\text{A}$, $V_{BR} = 60\text{ V}$ minimum.

4.3.4 Power burn-in conditions. The power burn-in conditions shall be in accordance with condition A of Method 1038 of [MIL-STD-750](#). The following details shall apply: $T_J = +100^\circ\text{C}$; $V_R = 48\text{ V}$ dc.

MIL-PRF-19500/771B
w/AMENDMENT 3

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table E-V of [MIL-PRF-19500](#), and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in 4.4.2.1 for quality level JANS and 4.4.2.2 for quality levels JAN, JANTX, and JANTXV. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.4.2.1 Quality level JANS (table E-VIA of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2\text{ A}$ minimum for 2,000 cycles.
B5	1038	Condition A, $V_R = 48\text{ V dc}$, $T_J = +100^\circ\text{C}$, $t = 340\text{ hours}$ minimum; heat sinking allowed.
As an alternative method a five (5) dice sample from each individual wafer from the wafer lot shall be qualified for 1,000 hours minimum then each conformance inspection lot requires 340 hours minimum when selected from qualified wafers. This option must be approved by the qualifying activity based on data from at least 3 wafer lots. Any change to the die design, or a conformance inspection failure of the alternate method, requires the 3 wafer lot qualification prior to using this alternative method.		

4.4.2.2 Quality levels JAN, JANTX, and JANTXV (table E-VIB of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2\text{ A}$ minimum for 2,000 cycles.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#). Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with [table II](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Condition A, weight = 10 lbs (4.5.4 kg), $t = 15\text{ seconds}$. Not applicable to U3 package.
C5	4081	Limit for thermal resistance for 1N7059CCT3 is 2.0°C/W for each diode. Limit for thermal resistance for 1N7060U3 is 2.0°C/W .
C6	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2\text{ A}$ minimum for 6,000 cycles.
C6	1038	Condition A, $V_R = 48\text{ V dc}$, $T_J = +100^\circ\text{C}$, $t = 1,000\text{ hours}$ minimum (for TX, TXV only); heat sinking allowed.
As an alternative method a five (5) dice sample from each individual wafer from the wafer lot shall be qualified for 1,000 hours minimum then each conformance inspection lot requires 340 hours minimum when selected from qualified wafers. This option must be approved by the qualifying activity based on data from at least 3 wafer lots. Any change to the die design, or a conformance inspection failure of the alternate method, requires the 3 wafer lot qualification prior to using this alternative method.		

MIL-PRF-19500/771B
w/AMENDMENT 3

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table III](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

MIL-PRF-19500/771B
w/AMENDMENT 3

TABLE I. Group A inspection.

Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>3/</u>	3101	See <u>4.3.2</u>	$Z_{\theta JX}$			°C/W
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 8$ A (pk) $I_F = 30$ A (pk)	V_{F1}		.59 .92	V V
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 16$ A (pk) $I_F = 60$ A (pk)	V_{F2}		.81 1.32	V V
Reverse current 1N7059CCT3 1N7060U3	4016	Condition A or B $V_R = 60$ V $V_R = 60$ V	I_{R1}		.68 .6	mA mA
<u>Subgroup 3</u>						
High temperature operation:		$T_C = +125$ °C				
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 8$ A (pk) $I_F = 30$ A (pk)	V_{F3}		.57 .88	V V
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 16$ A (pk) $I_F = 60$ A (pk)	V_{F4}		.79 1.24	V V
Reverse current 1N7059CCT3 1N7060U3	4016	Condition A or B $V_R = 60$ V $V_R = 60$ V	I_{R2}		150 100	mA mA
Low temperature operation:		$T_C = -55$ °C				
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 8$ A (pk) $I_F = 30$ A (pk)	V_{F5}		.63 .83	V V
Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B; pulsed test (see <u>4.5.1</u>) $I_F = 16$ A (pk) $I_F = 60$ A (pk)	V_{F6}		.79 1.18	V V

See footnotes at end of table.

MIL-PRF-19500/771B
w/AMENDMENT 3

TABLE I. Group A inspection – Continued.

Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> Junction capacitance	4001	$V_R = 5 \text{ V dc}$, $f = 1 \text{ MHz}$, $V_{SIG} = 50 \text{ mV (p-p)}$	C_J		700	pF
<u>Subgroup 5</u> Not applicable						
<u>Subgroup 6</u> Surge current	4066	Condition A, see column 4 of 1.3 . Ten surges for each diode; 60 seconds between surges. (see 4.5.1)				
Electrical measurements		See table I , subgroup 2 herein.				
<u>Subgroup 7</u> Dielectric withstanding voltage	1081	$V_R = 500 \text{ V dc}$; All leads shorted; Measure from leads to case	I_{LKG}		10	μA
Scope display evaluation	4023	Condition A, stable only				
Electrical measurements		See table I , subgroup 2 herein.				

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Each individual diode.

*3/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
Group C, subgroups 2, and 6.
Group E, subgroup 1.

MIL-PRF-19500/771B
w/AMENDMENT 3

* TABLE II. Delta measurements for groups B, C, and E. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits	Unit
		Method	Conditions			
1.	Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B, pulsed (see 4.5.1) $I_F = 8 \text{ A (pk)}$ $I_F = 30 \text{ A (pk)}$	ΔV_{F1}	$\pm 50 \text{ mV dc}$ from initial reading.	
2.	Forward voltage 1N7059CCT3 1N7060U3	4011	Condition B, pulsed (see 4.5.1) $I_F = 16 \text{ A (pk)}$ $I_F = 60 \text{ A (pk)}$	ΔV_{F2}	$\pm 50 \text{ mV dc}$ from initial reading.	
3.	Reverse current	4016	Condition A or B, $V_R = 60 \text{ V}$	ΔI_{R1}	± 100 percent from initial reading or $\pm 300 \mu\text{A}$ whichever is greater.	

1/ Each individual diode.

2/ The delta electrical measurements taken during group B inspection for quality level JANS (table E-VIA of MIL-PRF-19500) are as follows:

- * a. In addition to the measurements specified for subgroup 3, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- * b. In addition to the measurements specified for subgroup 4, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- c. In addition to the measurements specified for subgroup 5, the measurements of steps 1, 2, and 3 of this table shall also be taken.

3/ The delta electrical measurements taken during group B inspection for quality levels JANTX and JANTXV (table E-VIB of MIL-PRF-19500) are as follows:

- * a. In addition to the measurements specified for subgroup 2, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- * b. In addition to the measurements specified for subgroup 3, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- c. In addition to the measurements specified for subgroup 6, the measurements of steps 1, 2, and 3 of this table shall also be taken.

4/ The delta electrical measurements taken during group C inspection for all quality levels (table E-VII of MIL-PRF-19500) are as follows:

- * a. In addition to the measurements specified for subgroup 2, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- b. In addition to the measurements specified for subgroup 3, the measurements of steps 1, 2, and 3 for of this table shall also be taken.
- * c. In addition to the measurements specified for subgroup 6, the measurements of steps 1, 2, and 3 of this table shall also be taken.

5/ The delta electrical measurements taken during group E inspection for all quality levels (table E-IX of MIL-PRF-19500) are as follows:

- * a. In addition to the measurements specified for subgroup 1, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- b. In addition to the measurements specified for subgroup 2, the measurements of steps 1, 2, and 3 of this table shall also be taken.

6/ Devices which exceed the table I, limits for this test shall not be accepted.

MIL-PRF-19500/771B
w/AMENDMENT 3

TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			n = 45, c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55 °C to +150 °C.	
Electrical measurements		See table I subgroup 2 and table II herein.	
<u>Subgroup 2</u>			n = 45, c = 0
Blocking life	1048	t = 1,000 hours, T _J = +100 °C, V _R = 80 percent rated voltage (see 1.3 , column 2 herein).	
Electrical measurements		See table I subgroup 2 and table II herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10 1/</u>			n = 5, c = 0
Surge current 1N7059CCT3	4066	Condition A, T _A = +25 °C; I _{FSM} = 125 A, ten surges of 8.3 ms V _R = 0. I _O = 10 A pk half sine wave, continuous.	
1N7060U3		Condition A, T _A = +25 °C; I _{FSM} = 120 A, ten surges of 8.3 ms V _R = 0. I _O = 10 A pk half sine wave, continuous.	
Electrical measurements		See table I subgroup 2 (V _F and I _R only).	

1/ Each individual diode.

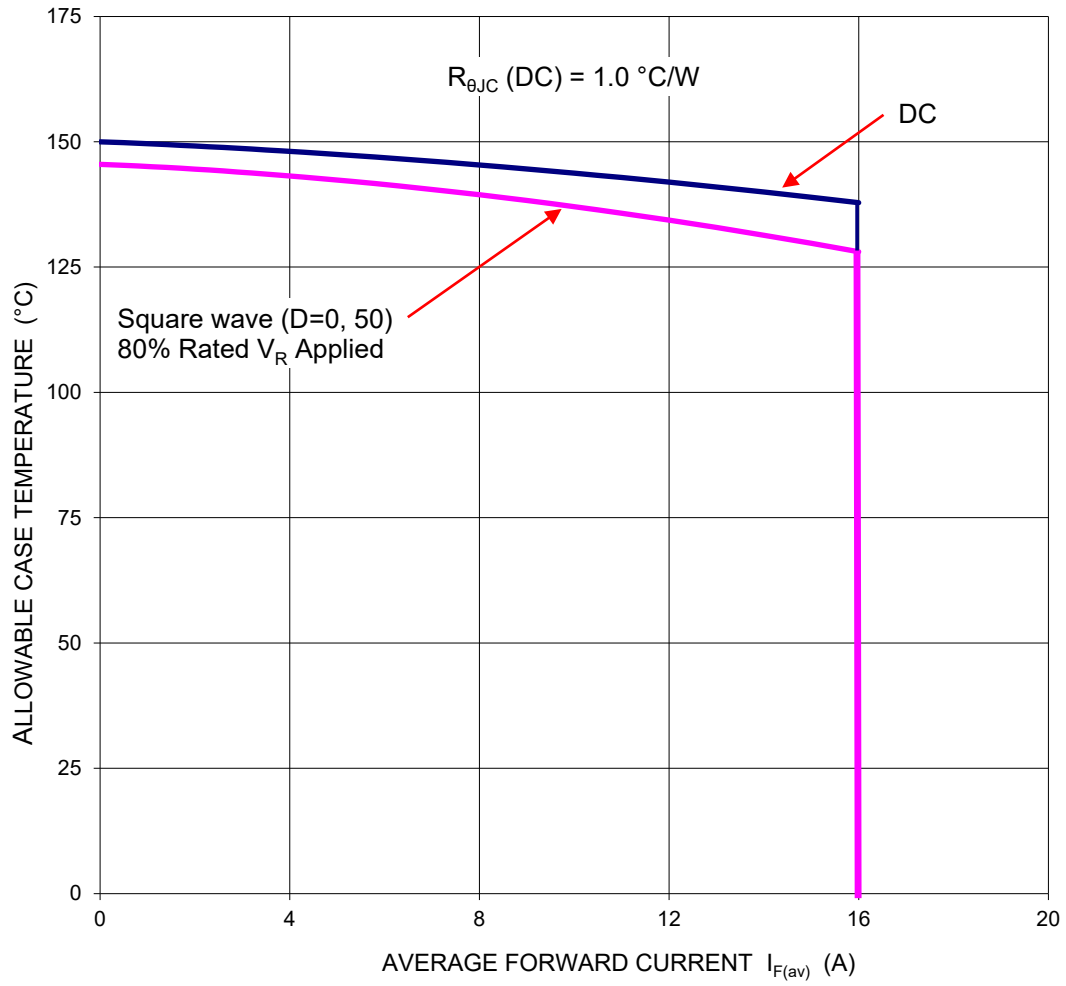


FIGURE 3. Temperature-current derating curve 1N7059CCT3 (entire package).

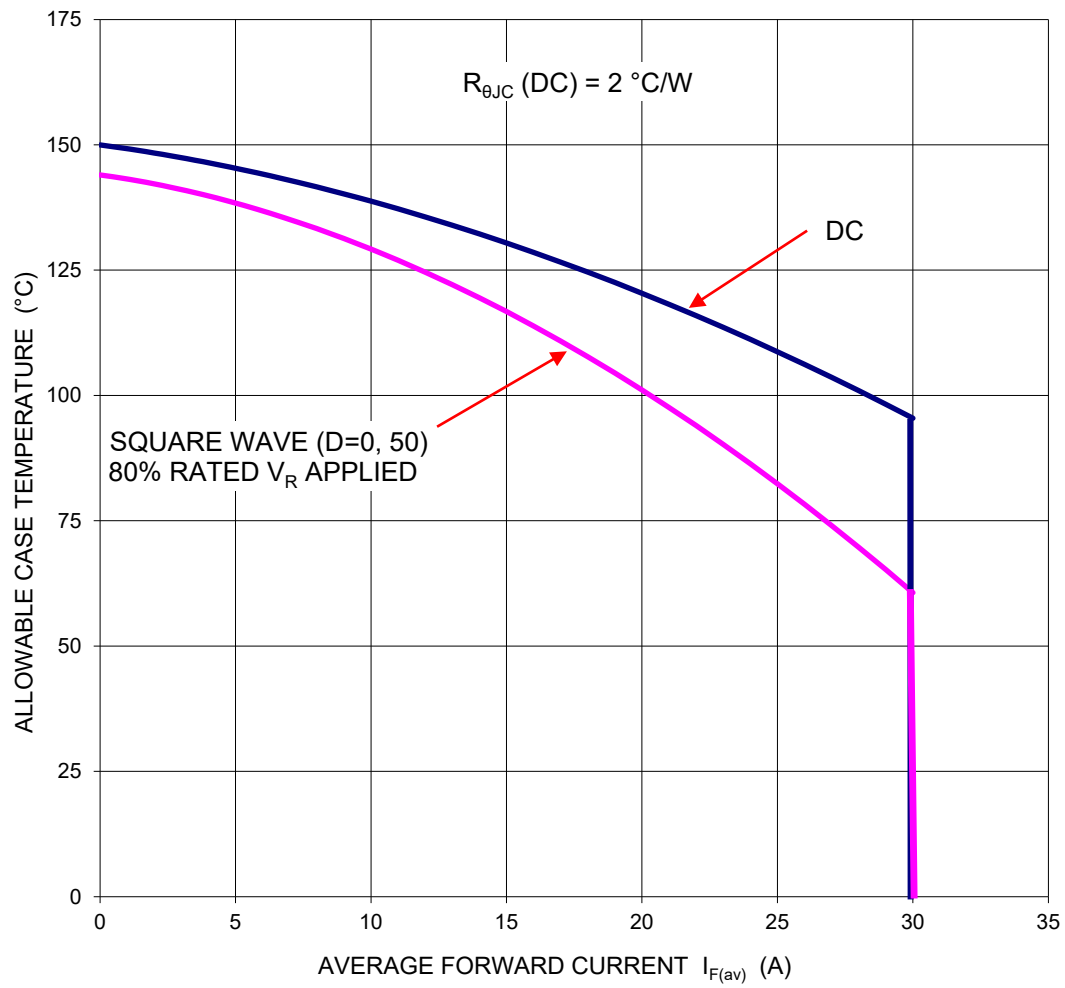


FIGURE 4. Temperature-current derating curve 1N7060U3 (entire package).

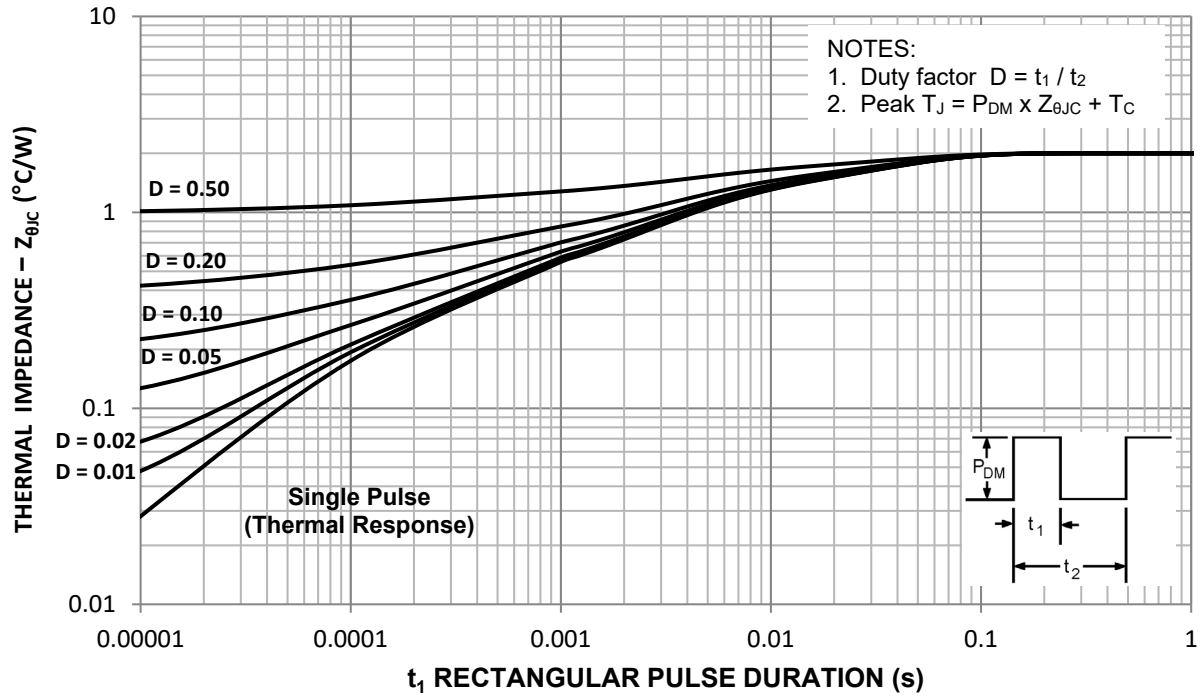


FIGURE 5. Thermal impedance 1N7059CCT3 (for each leg).

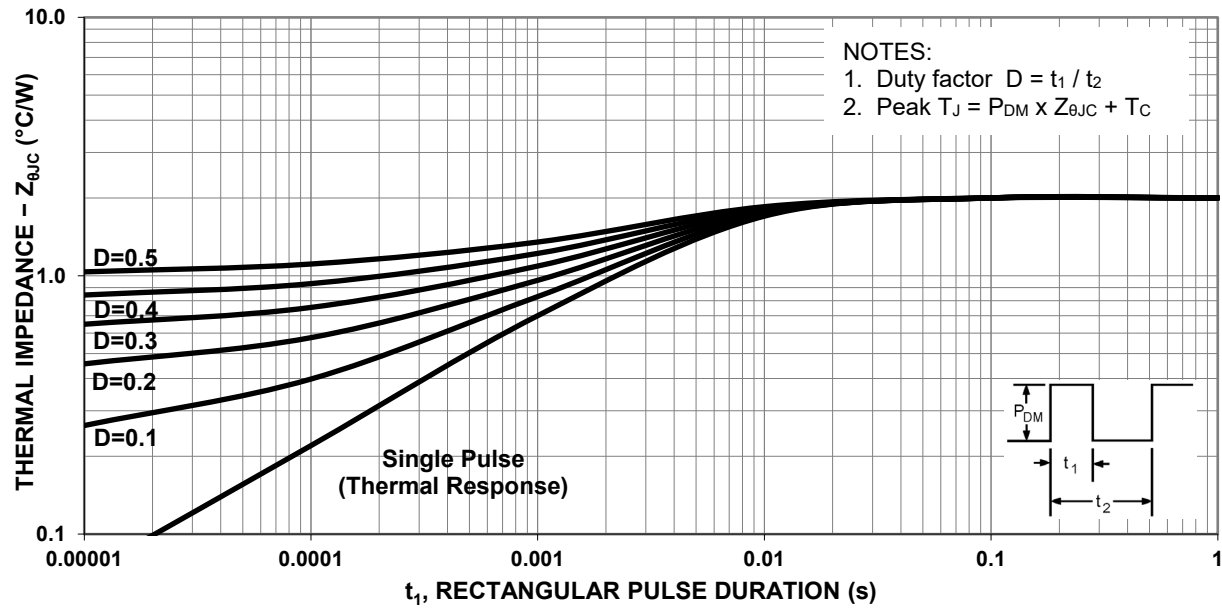
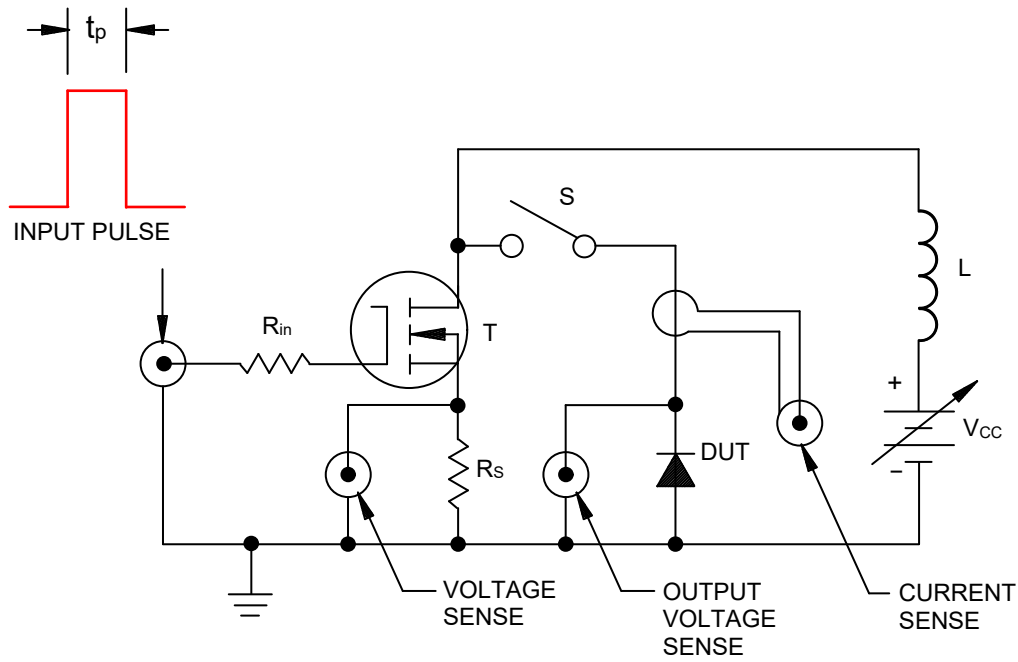


FIGURE 6. Thermal impedance 1N7060U3.



PROCEDURE:

1. With S open, adjust pulse width to test current of 1 A through R_s .
2. Close S, verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

NOTES:

- * 1. The following input pulse details shall apply: $V_G = 10$ Volts, P.W. $t_p \approx 30 \mu s$, duty cycle ≤ 1 percent.
2. The following test circuit component values shall apply: $L = 100 \mu H$, $Z_G = 50$ ohms, $R_{in} = 50$ ohms, 1 watt, $R_s = 0.1$ ohms, 1 watt, T = 2N6766 (IRF250 or equivalent).
3. The supply voltage $V_{cc} \approx 10$ volts.

FIGURE 7. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

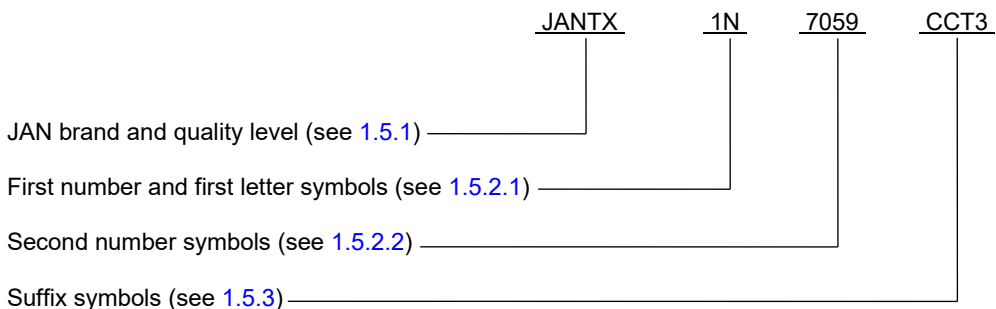
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1) and if applicable, any needed lead formation (TO-257 package only) (see 3.4.2).
- d. The complete PIN, see 1.5 and 6.4.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form:



MIL-PRF-19500/771B
w/AMENDMENT 3

6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

Base quality level	Quality level "TX"	Quality level "TXV"	Quality level "S"
JAN1N7059CCT3	JANTX1N7059CCT3	JANTXV1N7059CCT3	JANS1N7059CCT3
JAN1N7060U3	JANTX1N7060U3	JANTXV1N7060U3	JANS1N7060U3

6.6 Cross reference substitution list. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
16SCYQ060C	JAN, JANTX, JANTXV, JANS1N7059CCT3
30SLJQ060	JAN, JANTX, JANTXV, JANS1N7060U3

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army – CR
Navy – SH
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:
DLA – CC

(Project 5961-2023-043)

Review activities:
Army – AV, MI
Navy – AS
Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.