

The documentation and process conversion measures necessary to comply with this revision shall be completed by 16 September 2025.

INCH-POUND

MIL-PRF-19500/756A
w/AMENDMENT 3
16 June 2025
MIL-PRF-19500/756A
w/AMENDMENT 2
17 November 2022

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED,
N-CHANNEL, SILICON, THROUGH HOLE AND SURFACE MOUNT, TYPES 2N7606 AND 2N7607
QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, radiation hardened (total dose and single event effects (SEE)), low-threshold logic level, MOSFET, transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}).

* 1.2 Package outlines. The device packages outlines are as follows: Three terminal flange mount header TO-257AA (T3) package in accordance with [figure 1](#), surface mount device (SMD) TO-276AA (SMD.5, U3) package in accordance with [figure 2](#), and a SMD similar to TO-276AA (U3CE) in accordance with [figure 3](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) T_C $=+25^\circ\text{C}$	P_T T_A $=+25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{GS}	I_{D1} $T_C = +25^\circ\text{C}$ (3) (4)	I_{D2} $T_C = +100^\circ\text{C}$ (3) (4)	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>
2N7607T3	75	1.56	1.67	60	± 10	20	20	20	80	-55 to +150
2N7606U3, U3CE	57	1.00	2.20	60	± 10	22	20	22	88	

(1) Derate linearly by 0.60 mW/ $^\circ\text{C}$ (T3) for $T_C > +25^\circ\text{C}$, 0.45mW/ $^\circ\text{C}$ (U3) for $T_C > +25^\circ\text{C}$.

(2) See [figure 4](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D limit: I_D is limited by product design & construction (package, internal wires and pin diameter) to 20A (T3) and 22A (U3).

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See [figure 5](#), maximum drain current graph.

(5) $I_{DM} = 4 \times I_{D1}$ as calculated in note (3).

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AMSC N/A

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- * 1.4 Primary electrical characteristics. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)} \text{ DSS}$	$V_{GS} \text{ (th)}^1$	Max I_{DSS1}	Max $r_{DS(on)} \text{ (1)}$ $V_{GS} = 4.5 \text{ V dc}$		E_{AS}	I_{AS}
	$V_{GS} = 0 \text{ V}$ $I_D = 250 \mu\text{A}$ dc	$V_{DS} \geq V_{GS}$ $I_D = 250 \mu\text{A}$ dc	$V_{GS} = 0 \text{ V}$ $V_{DS} = 80\% \text{ rated}$ V_{DS}	at I_{D2} $T_J = +25^\circ\text{C}$	$T_J =$ $+150^\circ\text{C}$		
	<u>V dc</u>	<u>V dc</u> <u>Min</u> <u>Max</u>		<u>μA dc</u>	<u>Ohm</u>	<u>Ohm</u>	<u>mJ</u>
2N7607T3	60	1.0	2.0	1.0	0.045	0.076	98
2N7606U3	60	1.0	2.0	1.0	0.035	0.057	63
2N7606U3CE	60	1.0	2.0	1.0	0.039	0.064	63
							<u>A dc</u>

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "TXV" and "S".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7606" and "7607".

- * 1.5.4 Suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

T3	Indicates a through-hole mount package similar to a TO-257AA (see figure 1).
U3	Indicates a 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 2).
U3CE	Indicates a ceramic lidded 3 pad surface mount package with enhanced PCB mount features, similar to a TO-276AA (SMD-0.5) (see figure 3).

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML 19500.

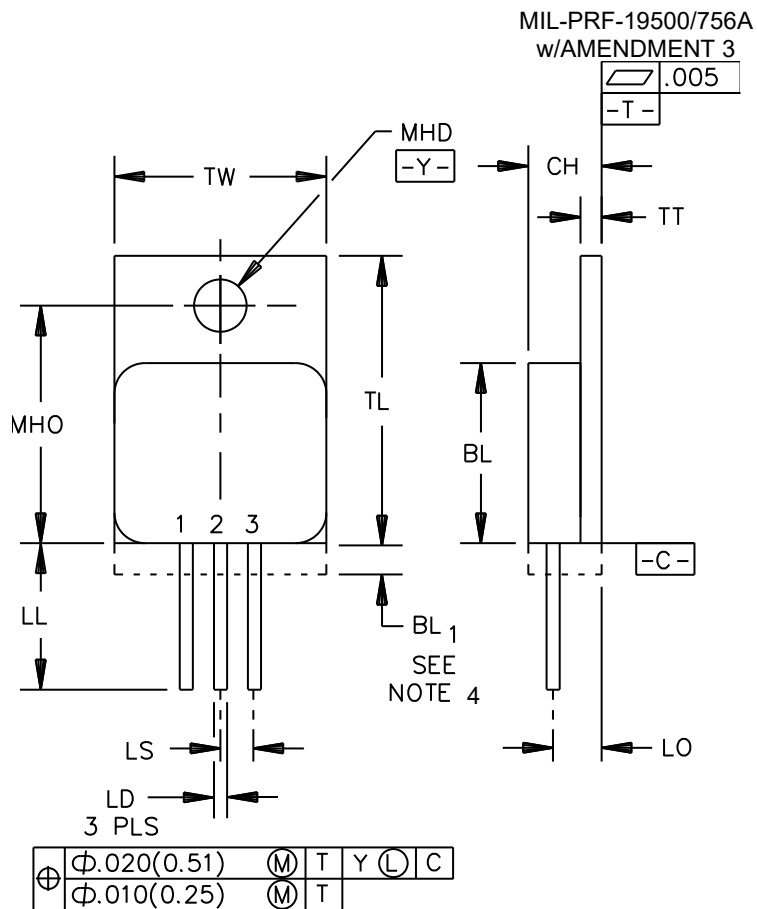
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1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of [MIL-STD-750](#) are as follows:

For device type 2N7607T3, 2N7606U3:..... 300 krad(Si) 1/

- 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of [MIL-STD-750](#). The radiation end point limits are guaranteed only to a maximum TID level of 300 krad(Si).



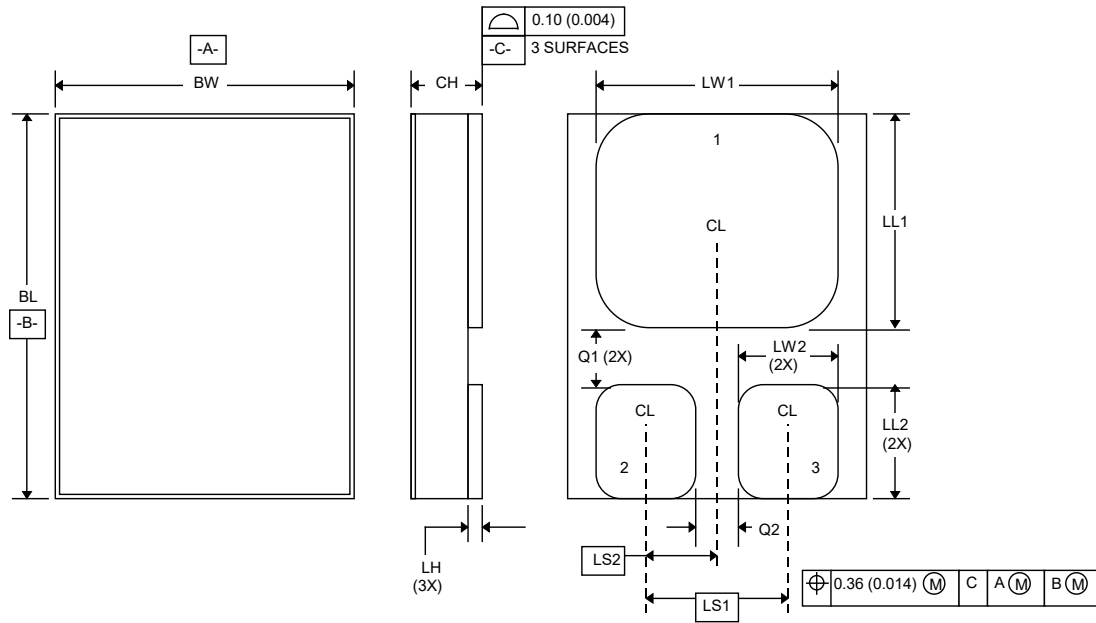
Ltr	Inches	Inches	mm	mm
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL ₁		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05	BSC
LS	.100 BSC		2.54	BSC
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).

FIGURE 1. Dimensions and configuration, TO-257AA (T3).

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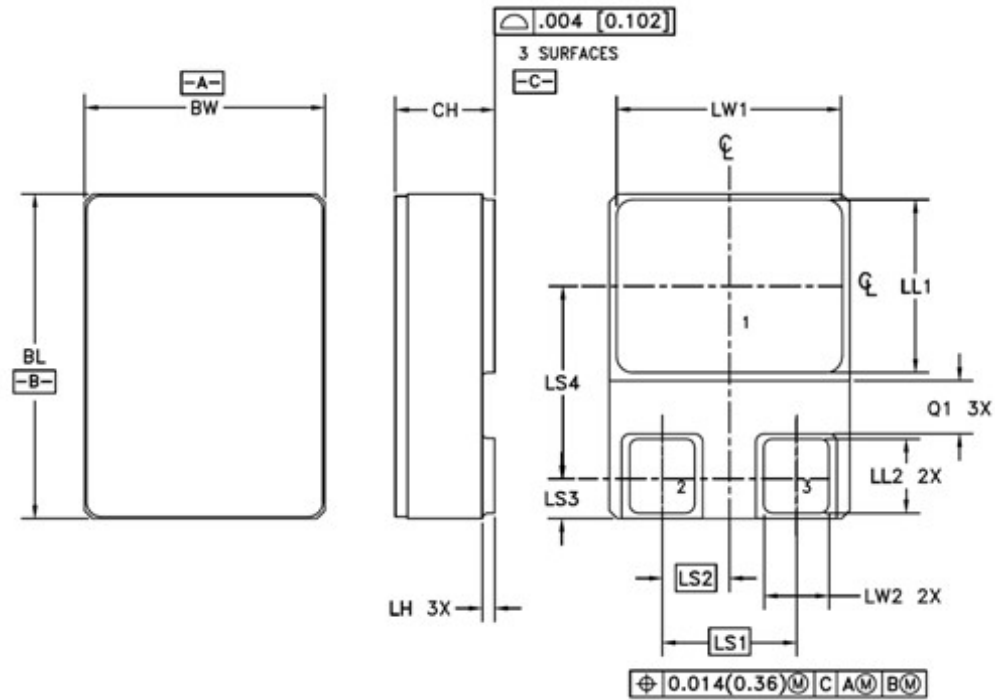
Symbol	Dimensions			
	Inches	Inches	Millimeters	Millimeters
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.124		3.15
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

* NOTES:

1. Dimension are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.

FIGURE 2. Dimensions and configuration TO-276AA, SMD-0.5 (U3).

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.122		3.09
LH	.008	.022	0.20	0.55
LW1	.271	.281	6.88	7.14
LW2	.075	.085	1.91	2.16
LL1	.208	.218	5.28	5.54
LL2	.087	.097	2.21	2.46
LS1	.165 BSC		4.19 BSC	
LS2	.083 BSC		2.10 BSC	
LS3	.053 BSC		1.35 BSC	
LS4	.234 BSC		5.93 BSC	
Q1	.060		1.52	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches, Millimeters are given for information only.
2. Dimension tolerances $\pm .005$.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. Dimensions are pre solder finish.

* FIGURE 3. Dimensions and configuration (Similar to TO-276AA, SMD-0.5), with ceramic lid U3CE.

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in **MIL-PRF-19500** and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in **MIL-PRF-19500**.

* 3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in **MIL-PRF-19500** and on figure 1 (T3), figure 2 (U3), and figure 3 (U3CE).

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with **MIL-PRF-19500**, **MIL-STD-750**, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Pin-out. The pin-out of the device shall be as shown on figures 1, 2, and 3.

3.4.3 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with **MIL-PRF-19500**.

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3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced (see [table II](#)). End-point measurements shall be in accordance with [table II](#).

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

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4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS	Measurements for JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein I _{DSS1} , I _{GSSF1} , I _{GSSR1} as minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 0.5 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)1} , V _{GS(TH)1} Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 0.5 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(ON)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(TH)1} = \pm 20 \text{ percent of initial value.}$	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 0.5 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(ON)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(TH)1} = \pm 20 \text{ percent of initial value.}$
17	For TO-257AA and U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For TO-257AA and U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, V_{GS(th)1}, and r_{DS(ON)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

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* 4.3.1 Gate stress test. Apply $V_{GS} = \pm 15$ V minimum for $t = 250$ μ s minimum.

* 4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS})..... I_{D1} .
- b. Peak gate voltage (V_{GS})..... 10 V dc (up to max rated V_{GS}).
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature+25°C, +10°C, -5°C.
- e. Inductance: $\left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 25 V dc (up to max V_{DS}).

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). See [table III](#), group E, subgroup 4 herein.

* 4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage..... 800 V dc (TO-257AA), 600V dc (U3 and U3CE).
- b. Duration of application of test voltage 15 seconds (min).
- c. Points of application of test voltage All leads to case (bunch connection).
- d. Method of connection..... Mechanical.
- e. Kilovolt-ampere rating of high voltage source 1,200 V/1.0 mA (min).
- f. Maximum leakage current..... 1.0 mA.
- g. Voltage ramp up time..... 500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#). Alternate flow is allowed for quality conformance inspection in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#) herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and herein.

4.4.2.1 Quality level JANS (table E-VIA of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS} ; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS} ; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.

4.4.2.2 Quality level JANTXV (table E-VIB of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition C, 25 cycles.
B3	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS} ; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum; and accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS} ; T_A = +175°C, t = 170 hours minimum; or T_A = +150°C, t = 340 hours minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test Condition A, weight = 10 lbs (4.54 Kg), t = 10 s (applicable to TO-257AA only).
C5	3161	See 4.3.3 , $R_{\theta JC}$ = (see 1.3).
C6	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS} ; T_A = +175°C, t = 48 hours minimum; or T_A = +150°C, t = 96 hours minimum. and accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS} ; T_A = +175°C, t = 500 hours minimum; or T_A = +150°C, t = 1,000 hours minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JA}$			°C/W
Breakdown voltage drain to source	3407	$V_{GS} = 0$, $I_D = 250 \mu A$ dc, bias condition C	$V_{(BR)DSS}$	60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)1}$	1.0	2.0	V dc
Gate current	3411	$V_{GS} = +10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80\%$ of rated V_{DS}	I_{DSS1}		1.0	μA dc
Static drain to source on-state resistance 2N7607T3 2N7606U3 2N7606U3CE	3421	$V_{GS} = 4.5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.045 0.035 0.039	Ω Ω Ω
* Forward voltage	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2	V (pk)
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ C$				
Gate current	3411	$V_{GS} = \pm 10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		10	μA dc
Static drain to source on-state resistance 2N7607T3 2N7606U3 2N7606U3	3421	$V_{GS} = 4.5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$		0.070 0.055 0.079	Ω Ω Ω
* Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)2}$	0.5		V dc
Low temperature operation:		$T_C = T_J = -55^\circ C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)3}$		3.0	V dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/ 	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u>						
Forward transconductance 2N7607T3 2N7606U3 2N7606U3CE	3475	$V_{DS} = 15 \text{ V dc}$, $I_D = I_{D2}$, pulsed (see 4.5.1)	g_{FS}	19 24 15		S S S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 5.0 \text{ V dc}$, $R_G = 7.5 \Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time 2N7607T3 2N7606U3, U3CE			$t_{D(on)}$		26 26	ns ns
Rise time 2N7607T3 2N7606U3, U3CE			t_r		110 145	ns ns
Turn-off delay time 2N7607T3 2N7606U3, U3CE			$t_{D(off)}$		60 54	ns ns
Fall time 2N7607T3 2N7606U3, U3CE			t_f		28 30	ns ns
<u>Subgroup 5</u>						
Safe operating area test	3474	$V_{DS} = 80$ percent of rated V_{DS} (see 1.3), $t_P = 10 \text{ ms}$, I_D as specified in figure 6				
Electrical measurements		See table I, subgroup 2				
<u>Subgroups 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{GS} = 4.5 \text{ V dc}$, $V_{DD} = 50$ percent of rated V_{DS}				
On-state gate charge			Q_G		34	nC
and turn-off gate charge						
Gate to source charge			Q_{GS}		8	nC
(turn-on and turn-off)						
On Gate to drain charge			Q_{GD}		16	nC
(turn-on and turn-off)						
Reverse recovery time	3473	$di/dt = -100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 50 \text{ V}$, $I_D = I_{D1}$	t_{rr}		160	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

Group B, subgroups 3 and 4 (JANS).

Group B, subgroups 2 and 3 (JANTXV).

Group C, subgroup 2 and 6.

Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R & F		R		F		
				Min	Max	Min	Max	Min	Max	
Subgroup 1 Not applicable										
Subgroup 2 Steady-state total dose irradiation (V _{GS} bias) 4/	1019	T _C = + 25°C Condition A, V _{GS} = 6 V; V _{DS} = 0								
Steady-state total dose irradiation (V _{DS} bias) 4/	1019	Condition A, V _{GS} = 0; V _{DS} = 80 percent of rated V _{DS} (preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V _{GS} = 0; I _D = 250 μA; bias condition C	V _{(BR)DSS}	60		60		60		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} I _D = 250 μA	V _{GS(th)1}	1.0	2.0	1.0	2.0	1.0	2.0	V dc
Gate current	3411	V _{GS} = +10 V, V _{DS} = 0, bias condition C	I _{GSSF1}		100		100		100	nA dc
Gate current	3411	V _{GS} = -10 V, V _{DS} = 0, bias condition C	I _{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V _{GS} = 0, bias condition C V _{DS} = 80 percent of rated V _{DS} (preirradiation)	I _{DSS}		1.0		1.0		1.0	μA dc
Static drain to source on-state voltage	3405	V _{GS} = 4.5 V; condition A, pulsed (see 4.5.1), I _{D1} = I _{D2}	V _{DS(on)}							
2N7607T3					0.900		0.900		0.900	V dc
2N7606U3					0.600		0.600		0.600	V dc
2N7606U3CE					0.780		0.780		0.780	V dc
Forward voltage source drain diode	4011	V _{GS} = 0; I _D = I _{D1} bias condition A	V _{SD}		1.2		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

* 5/ Group D samples are built and tested in T0-3 packages. The equivalent pre-radiation and post radiation limit for V_{DS(on)} in the T0-3 package is also 0.900 V dc for the 2N7606U3, U3CE, and 2N7607T3 devices.

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TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

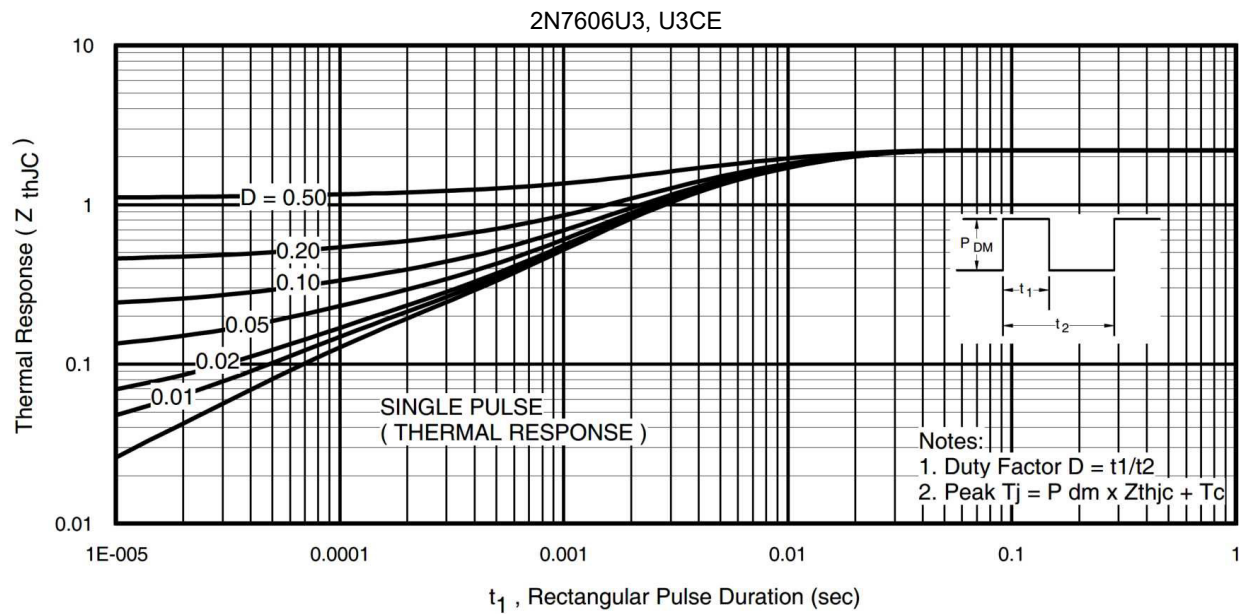
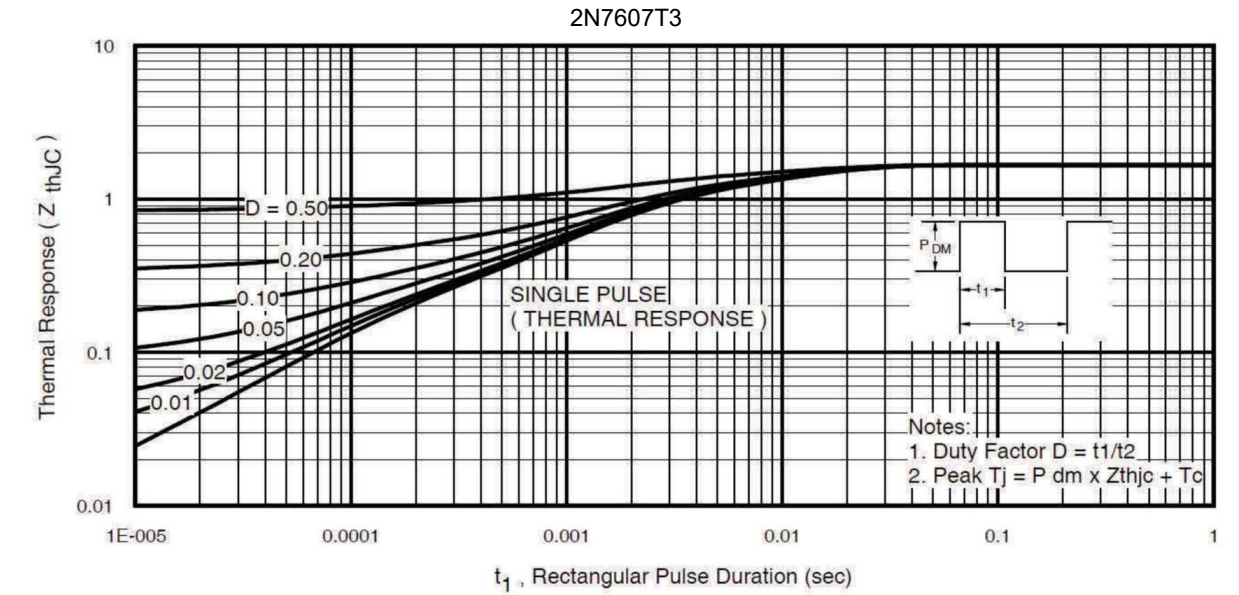
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal	1071	As applicable	
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves	3161	See MIL-PRF-19500	
<u>Subgroup 5</u>		Not applicable	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2 .	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET values of SEB and SEGR is sufficient to qualify all lower level LETs.

4/ The sampling plan applies to each bias condition.

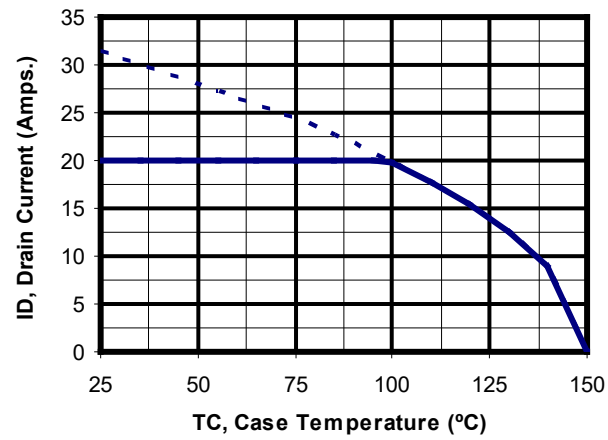


* FIGURE 4. Thermal impedance graph.

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2N7607T3

Maximum Current Rating



2N7606U3, U3CE

Maximum Current Rating

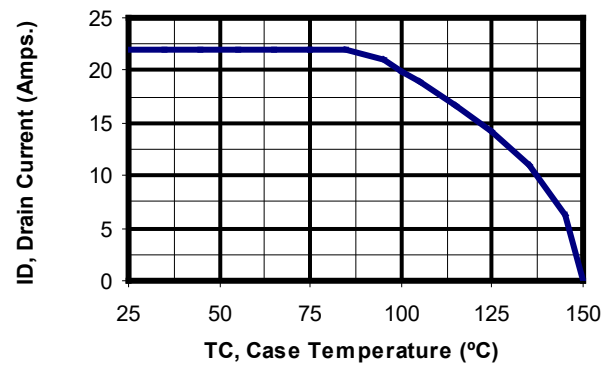
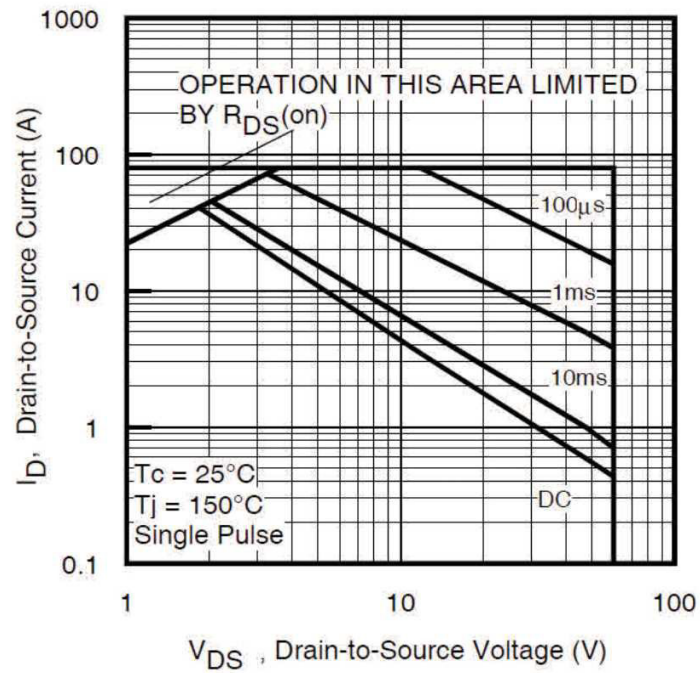
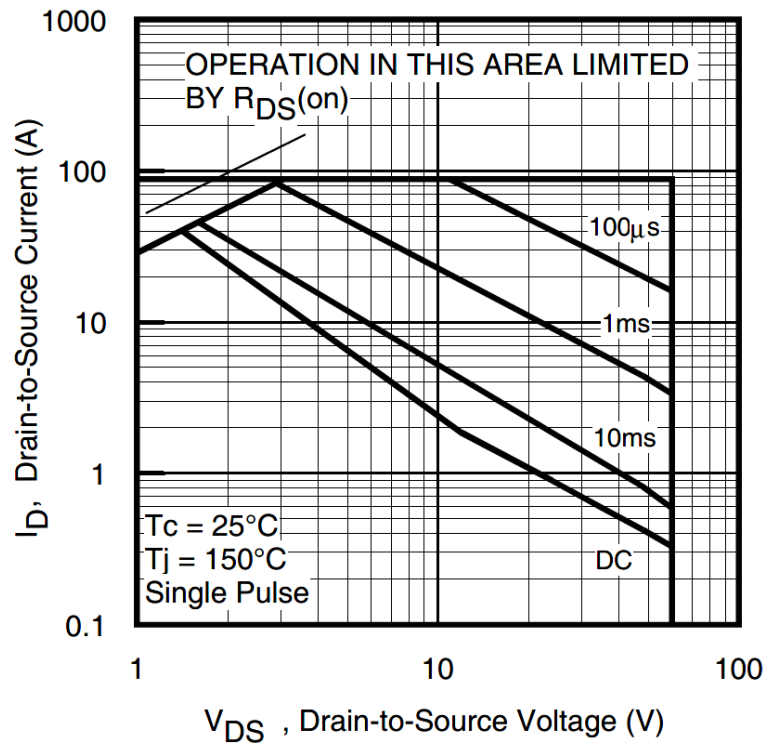


FIGURE 5. Maximum drain current vs case temperature graphs.

2N7607T3



2N7606U3



* FIGURE 6. Safe-operating-area graph

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of material is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see [3.4.1](#)).
- d. The complete PIN, see [1.5](#) and [6.5](#).
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If SEE testing data is desired, it should be specified in the contract or order.

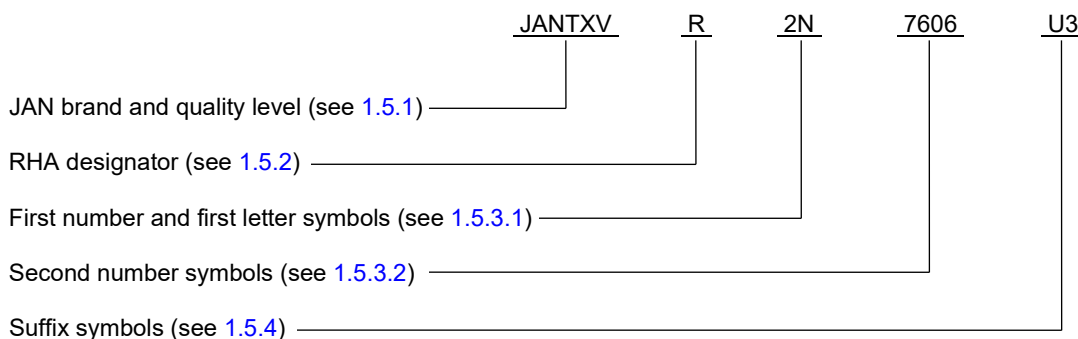
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHLYS77034CM	2N7607T3
IRHLNJ77034CM	2N7606U3
IRHNKC77034	2N7606U3CE

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6.5 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices in a TO-276AA package	PINs for devices in a U3CE package (Similar to TO-276AA)	PINs for devices in a TO-257AA package
JANTXVR2N7606U3	JANTXVR2N7606U3CE	JANTXVR2N7607T3
JANTXVF2N7606U3	JANTXVF2N7606U3CE	JANTXVF2N7607T3
JANSR2N7606U3	JANSR2N7606U3CE	JANSR2N7607T3
JANSF2N7606U3	JANSF2N7606U3CE	JANSF2N7607T3

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil.

6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2025-066)

Review activity:
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.