

The documentation and process conversion measures necessary to comply with this revision shall be completed by 15 September 2026.

INCH-POUND
MIL-PRF-19500/752A
w/AMENDMENT 2
15 June 2026
SUPERSEDING
MIL-PRF-19500/752A
w/AMENDMENT 1
22 August 2018

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL, LOGIC-LEVEL SILICON, ENCAPSULATED (THROUGH HOLE AND SURFACE MOUNT PACKAGES), TYPE 2N7608, 2N7609 JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), low-threshold logic level, MOSFET, transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANS product assurance levels.

* 1.2 Package outlines. The device package outlines are as follows: TO-39 (TO-205AF) in accordance with [figure 1](#) surface mount SMD-0.2, U8CE (ceramic lid) suffix in accordance with [figure 2](#), for all encapsulated device types.

* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) T_C $=+25^\circ\text{C}$	P_T T_A $=+25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{GS}	I_{D1} $T_C = +25^\circ\text{C}$ (3) (4)	I_{D2} $T_C = +100^\circ\text{C}$ (3) (4)	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u> -55 to +150
2N7608T2	21	0.63	6.0	100	± 10	6.0	3.7	6.0	24	
2N7609U8CE	23.2	.8	5.4	100	± 10	6.5	4.1	6.5	26	

(1) Derate linearly for 2N7608T2 by 0.168 W/ $^\circ\text{C}$ and 0.185 W/ $^\circ\text{C}$ for the 2N7609U8CE for $T_C > +25^\circ\text{C}$.

(2) See [figure 3](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D limit. I_D is limited to 12 A by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See [figure 4](#), maximum drain current graph.

(5) $I_{DM} = 4 \times I_{D1}$ as calculated in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

AMSC N/A

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

FSC 5961



MIL-PRF-19500/752A
w/AMENDMENT 2

* 1.4 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)} DSS$ $V_{GS} = 0\text{ V}$ $I_D = 250\text{ }\mu\text{A dc}$	$V_{GS} (th)1$ $V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A dc}$	Max I_{DSS1} $V_{GS} = 0\text{ V}$ $V_{DS} = 80\%$ rated V_{DS}	Max $r_{DS(on)} (1)$ $V_{GS} = 4.5\text{ V dc}$		E_{AS}	I_{AS}
				$T_J = +25^\circ\text{C}$ at I_{D2}	$T_J = +150^\circ\text{C}$ at I_{D2}		
	<u>V dc</u>	<u>V dc</u> Min Max	<u>$\mu\text{A dc}$</u>	<u>Ohm</u>	<u>Ohm</u>	<u>mJ</u>	<u>A dc</u>
2N7608T2	100	1.0 2.0	1.0	0.32	0.70	37	6
2N7609U8CE	100	1.0 2.0	1.0	0.29	0.55	21	6.5

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7608", "7609".

* 1.5.3.3 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

T2	Indicates the package is a TO-205AF (see figure 1).
U8CE	Indicates a ceramic lidded 3 pad surface mount package with enhanced PCB mount features, similar to a SMD-0.2 (see figure 2)

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

MIL-PRF-19500/752A
w/AMENDMENT 2

* 1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

* 1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of [MIL-STD-750](#) are as follows:

For device type 2N7608T2, 2N7609U8CE:.....300 Krad(Si) 1/

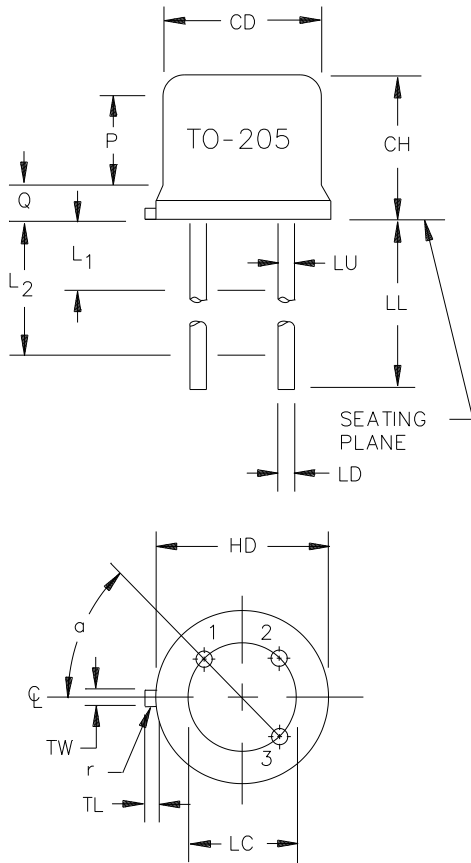
* 1.6.2 Heavy ion irradiation SEE. SEE testing includes Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR) tests at the specified linear energy transfer (LET) units. See [6.7](#) for the specific RHA SEE characterization testing details. The following characterization conditions were used for the testing to the requirements herein:

For device type 2N7608T2, 2N7609U8CE:

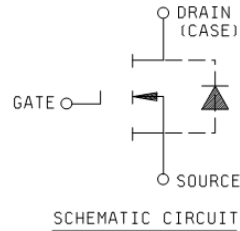
No SEB or SEGR were observed at surface LET (see [table IV](#)) $\leq 85 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ 2/
(In-situ Bias $V_{DS} = 100 \text{ V}$ and $V_{GS} = -5 \text{ V}$)

- * 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of [MIL-STD-750](#). The radiation end point limits are guaranteed only to a maximum TID level of 300 Krad(Si).
- * 2/ The manufacturers have performed SEE tests at Texas A&M University (TAMU) Radiation Effects Facility in accordance with method 1080 of [MIL-STD-750](#). For more information on SEE testing and results, customers should contact the qualified manufacturer.

MIL-PRF-19500/752A
w/AMENDMENT 2



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.315	.355	8.01	9.01	
CH	.160	.180	4.06	4.57	
HD	.340	.370	8.64	9.39	
LC	.200 TP		5.08 TP		6
LD	.016	.019	0.41	0.48	7, 8
LL	.500	.750	12.7	19.05	7, 8
LU	.016	.019	0.41	0.48	7, 8
L ₁		.050		1.27	7, 8
L ₂	.250		6.35		7, 8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	9
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	2
α	45° TP		45° TP		6



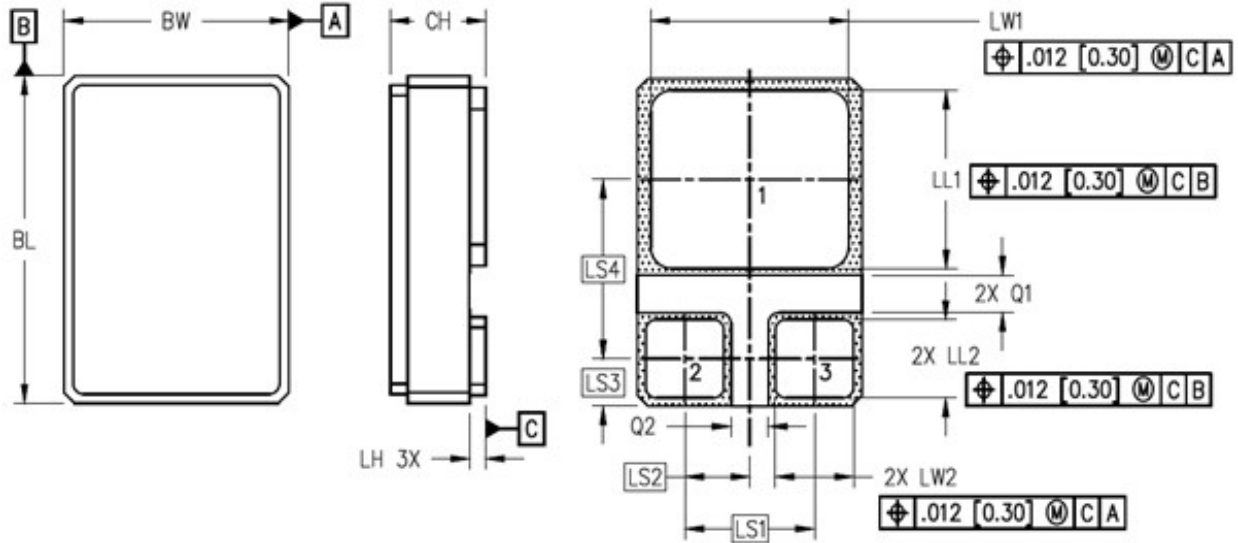
* NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 +.001, -.000 inch (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. LU applies between L₁ and L₂. LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
10. Drain is electrically connected to the case.

*

FIGURE 1. Physical dimensions for TO-205AF (2N7608T2).

MIL-PRF-19500/752A
w/AMENDMENT 2



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.300	.310	7.62	7.87
BW	.205	.215	5.21	5.46
CH		.097		2.46
LH	.010	.020	0.25	0.51
LW1	.180	.190	4.57	4.83
LW2	.068	.078	1.73	1.98
LL1	.161	.171	4.09	4.34
LL2	.068	.078	1.73	1.98
LS1	.121	BSC	3.07	BSC
LS2	.061	BSC	1.55	BSC
LS3	.044	BSC	1.12	BSC
LS4	.167	BSC	4.24	BSC
Q1	.030		0.76	
Q2	.030		0.76	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Lid is isolated.

*

FIGURE 2. Dimensions and configuration (Similar to SMD-0.2), with ceramic lid (U8CE).

MIL-PRF-19500/752A
w/AMENDMENT 2

* 2. APPLICABLE PUBLICATIONS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-750 - Test Methods for Semiconductor Devices.
- * MIL-STD-883 - Test Method Standard for Microcircuits.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

IAS Rated avalanche current, non-repetitive.
nC nano Coulomb.

- * 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500 and figure 1, and figure 2 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2) and should be specified by the PIN (see 1.5).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

- * 3.4.3 Silicone die coating. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883 on each lot of silicone die coating for its intended applications.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

MIL-PRF-19500/752A
w/AMENDMENT 2

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#) herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#) and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of [MIL-STD-750](#) that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table II](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.2.2 Silicone die coating. When silicone die coating is used, method 5011 of [MIL-STD-883](#) shall be performed on that coating in the full [MIL-PRF-19500](#) qualification process.

MIL-PRF-19500/752A
w/AMENDMENT 2

4.3 Screening (JANS, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS	Measurements for JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 1 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$	Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 1 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(ON)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(TH)1} = \pm 20 \text{ percent of initial value.}$	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = \pm 20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 1 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(ON)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(TH)1} = \pm 20 \text{ percent of initial value.}$

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $V_{GS(th)1}$, and $r_{DS(ON)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

MIL-PRF-19500/752A
w/AMENDMENT 2

4.3.1 Gate stress test. Apply $V_{GS} = 15 \text{ V}$ minimum for $t = 250 \text{ } \mu\text{s}$ minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS})..... I_{D1} .
- b. Peak gate voltage (V_{GS})..... 10 V dc, up to rated V_{GS} .
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \text{ } \Omega$.
- d. Initial case temperature $+25^{\circ}\text{C}$, $+10^{\circ}\text{C}$, -5°C .
- e. Inductance: $\left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right] \text{ mH minimum.}$
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}).....25 V dc.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). See [table III](#), group E, subgroup 4 herein.

* 4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, and JANTXV) of [MIL-PRF-19500](#), and herein.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
* B3	2052	PIND, required if not performed in screening. (22 devices, $c = 0$ for large lots, 12 devices, $c = 0$ for small lots).
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated } V_{GS}$; $T_A = +175^{\circ}\text{C}$, $t = 24$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated } V_{DS}$; $T_A = +175^{\circ}\text{C}$, $t = 120$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 240$ hours minimum.
B5	2037	Test condition D.

MIL-PRF-19500/752A
w/AMENDMENT 2

4.4.2.2 Quality levels and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition C, 25 cycles.
B3	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS} ; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum; and accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS} ; T_A = +175°C, t = 170 hours minimum; or T_A = +150°C, t = 340 hours minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
* C2	2036	Test condition E, not applicable to the SMD-0.2 (U8CE) package.
* C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, $c = 0$ for large lots, 12 devices, $c = 0$ for small lots).
C5	3161	See 4.5.2 , $R_{\theta JC}$ = (see 1.3).
C6	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated V_{GS} ; T_A = +175°C, t = 48 hours minimum; or T_A = +150°C, t = 96 hours minimum. and accelerated steady-state reverse bias, condition A, V_{DS} = rated V_{DS} ; T_A = +175°C, t = 500 hours minimum; or T_A = +150°C, t = 1,000 hours minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} (and V_H where appropriate). See table E-IX of [MIL-PRF-19500](#), group E, subgroup 4.

* 4.5.3 SEM exception. For devices with die using a repeating grid design, the oxide step coverage acceptance criteria provided in MIL-STD-750, test method 2077, paragraph 3.7.1.2 shall not apply. Instead, the minimum active metal thickness (cross section) shall provide for the maximum allowable current density of 5×10^5 amps/cm² in accordance with MIL-PRF-19500 paragraph H.3.6. The source metallization thickness at the oxide step shall be verified for the overall thickness, which corresponds to the applicable device channel width at the maximum rated continuous current ($I_{D\text{MAX}}$). The maximum allowable current density may be found using the following equation; Current Density (A/cm²) = I_D current max / Step metal thickness (cm) * Channel width (cm).

MIL-PRF-19500/752A
w/AMENDMENT 2
TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	$V_{GS} = 0$, $I_D = 250 \mu A$ dc, bias condition C	$V_{(BR)DSS}$	100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)1}$	1.0	2.0	V dc
Gate current	3411	$V_{GS} = +10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		1.0	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 4.5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7608T2					0.32	Ω
2N7609U8CE					0.29	Ω
Forward voltage	4011	$V_{GS} = 0$, condition A, $I_D = I_{D1}$	V_{SD}		1.2	V (pk)
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ C$				
Gate current	3411	$V_{GS} = \pm 10$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		10	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 4.5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$			
2N7608T2					0.60	Ω
2N7609U8CE					0.46	Ω
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)2}$	0.5		V dc
Low temperature operation:		$T_C = T_J = -55^\circ C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu A$ dc	$V_{GS(TH)3}$		3.0	V dc

See footnotes at end of table.

MIL-PRF-19500/752A
w/AMENDMENT 2
TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u>						
Forward transconductance	3475	$V_{DS} = 15 \text{ V dc}$, $I_D = I_{D2}$, pulsed (see 4.5.1)	g_{FS}	3.0		S
2N7608T2				3.5		S
2N7609U8CE						
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 5.0 \text{ V dc}$, $R_G = 7.5 \Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		18	ns
2N7608T2					18	ns
2N7609U8CE						
Rise time			t_r		90	ns
2N7608T2					75	ns
2N7609U8CE						
Turn-off delay time			$t_{D(off)}$		45	ns
2N7608T2					50	ns
2N7609U8CE						
Fall time			t_f		32	ns
2N7608T2					42	ns
2N7609U8CE						
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 5</u>						
Safe operating area test	3474	$V_{DS} = 80$ percent of rated V_{DS} (see 1.3) $t_P = 10 \text{ ms}$, I_D as specified in figure 5				
Electrical measurements		See table I, subgroup 2				
<u>Subgroups 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{DD} = 50$ percent rated V_{DS}				
On-state gate charge and turn-off gate charge			$Q_{G(ON)}$ $Q_{G(OFF)}$		13.5	nC
2N7608T2					11	nC
2N7609U8CE						
Gate to source charge (turn-on and turn-off)			Q_{GS1} Q_{GS2}		3.6	nC
2N7608T2					4	nC
2N7609U8CE						

See footnotes at end of table.

MIL-PRF-19500/752A
w/AMENDMENT 2

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 7</u> -Continued						
Gate to drain charge (turn-on and turn-off) 2N7608T2 2N7609U8CE			Q_{GD1} Q_{GD2}		8 6	nC nC
Reverse recovery time 2N7608T2 2N7609U8CE	3473	Condition A, $di/dt = -100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 25 \text{ V}$, $I_D = I_{D1}$	t_{rr}		260 215	ns ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

MIL-PRF-19500/752A
w/AMENDMENT 2
TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F		R		F		
				Min	Max	Min	Max	Min	Max	
Subgroup 1										
Not applicable										
Subgroup 2										
Steady-state total dose irradiation (V _{GS} bias) 4/	1019	T _C = + 25°C V _{GS} = 10V; V _{DS} = 0								
Steady-state total dose irradiation (V _{DS} bias) 4/	1019	V _{GS} = 0; V _{DS} = 80 percent of rated V _{DS} (preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V _{GS} = 0; I _D = 250 μA; bias condition C	V _{(BR)DSS}	100		100		100		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} I _D = 250 μA	V _{GS(th)1}	1.0	2.0	1.0	2.0	1.0	2.0	V dc
Gate current	3411	V _{GS} = +10 V, V _{DS} = 0, bias condition C	I _{GSSF1}		100		100		100	nA dc
Gate current	3411	V _{GS} = -10 V, V _{DS} = 0, bias condition C	I _{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V _{GS} = 0, bias condition C V _{DS} = 80 percent of rated V _{DS} (preirradiation)	I _{DSS}		1.0		1.0		1.0	μA dc
Static drain to source on-state voltage	3405	V _{GS} = 4.5 V; condition A, pulsed (see 4.5.1), I _{D1} = I _{D2}	V _{DS(on)}							
2N7608T2					1.184		1.184		1.184	V dc
2N7609U8CE					1.189		1.189		1.189	V dc
Forward voltage source drain diode	4011	V _{GS} = 0; I _D = I _{D1} , bias condition A	V _{SD}		1.2		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

5/ Group D samples are built and tested in T0-3 packages. The equivalent pre-radiation and post radiation limit for V_{DS(on)} in the T0-3 package is different than the reported limits. For the 2N7608T2, it is 1.110 Vdc and for the 2N7609U8CE, it is 1.066 Vdc.

MIL-PRF-19500/752A
w/AMENDMENT 2

TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

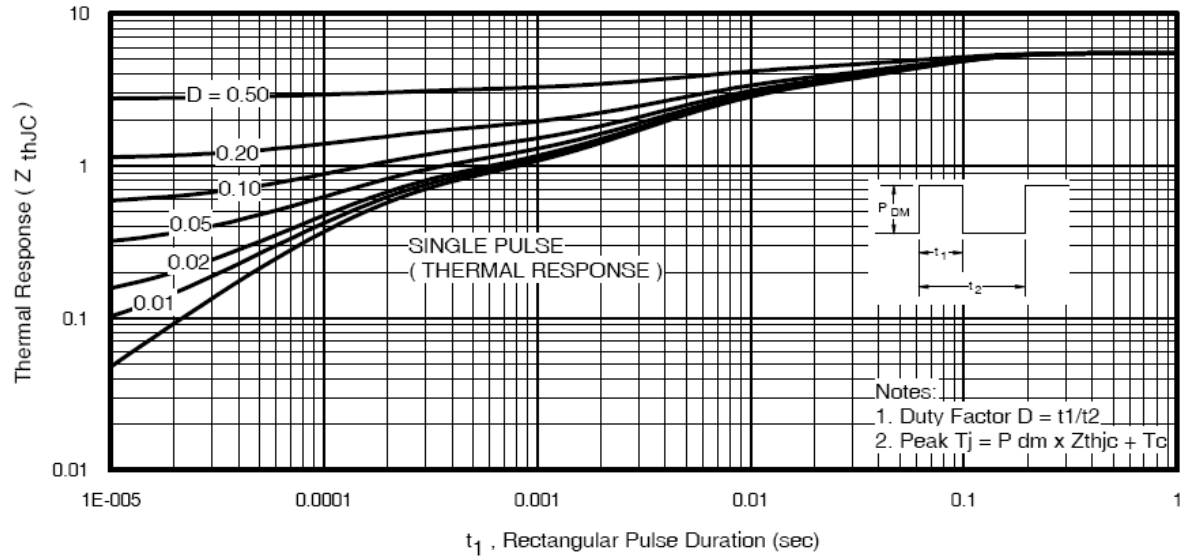
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal	1071	As applicable	
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves	3161	See MIL-PRF-19500	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
<u>Subgroup 11</u>			
SEE <u>2/ 3/</u>	1080	See method 1080 of MIL-STD-750 .	

1/ A separate sample for each test shall be pulled.

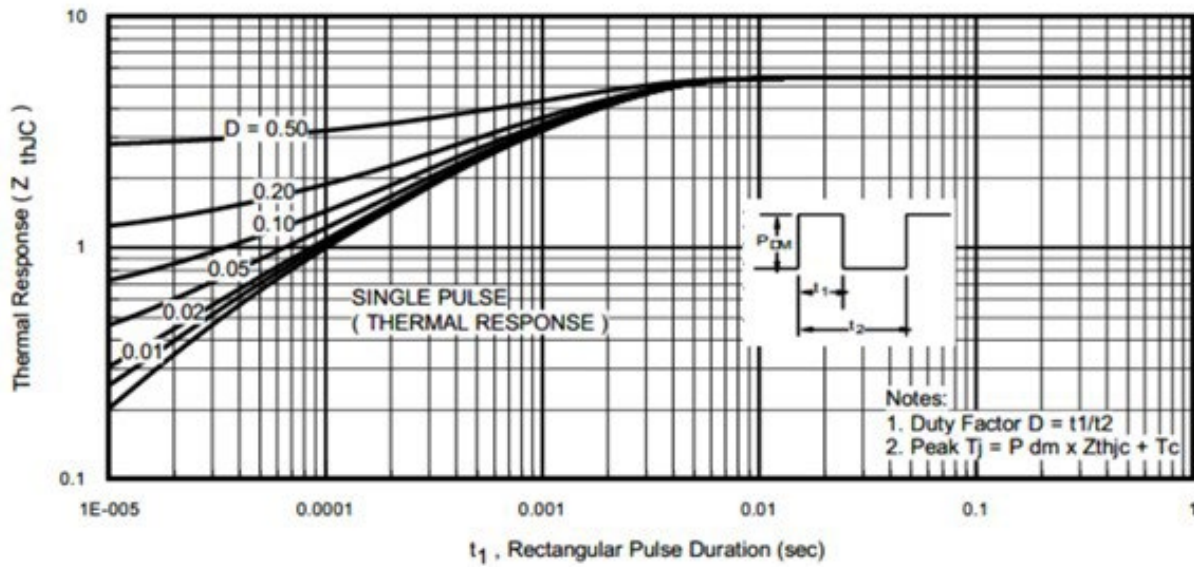
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ The sampling plan applies to each bias condition.

MIL-PRF-19500/752A
w/AMENDMENT 2



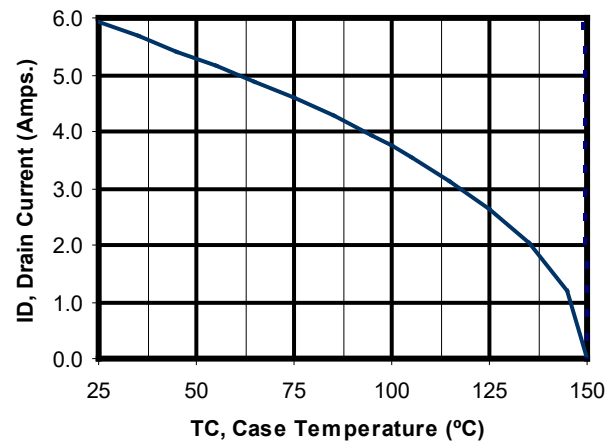
2N7608T2



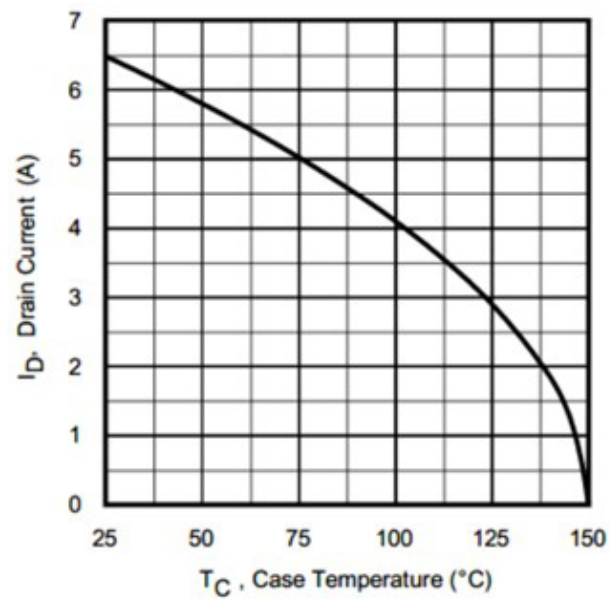
2N7609U8CE

* FIGURE 3. Thermal impedance graph.

Maximum Current Rating



2N7608T2



2N7609U8CE

* FIGURE 4. Derating drain current.

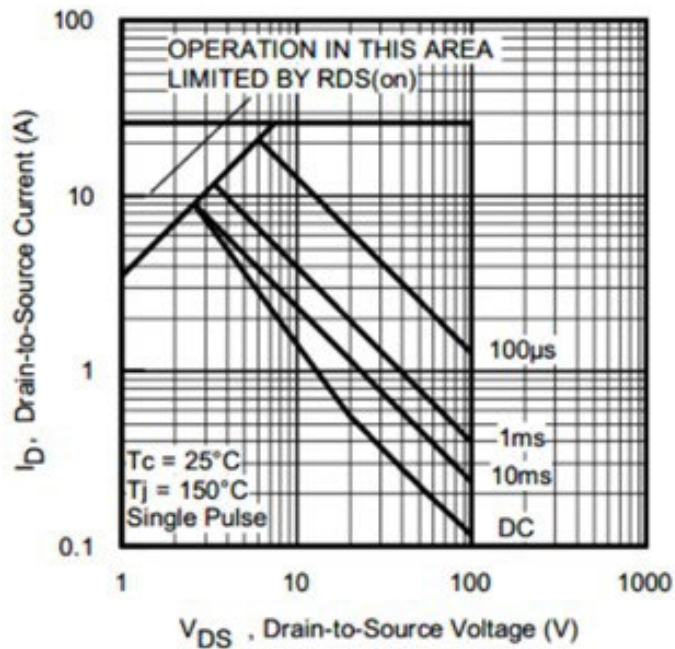
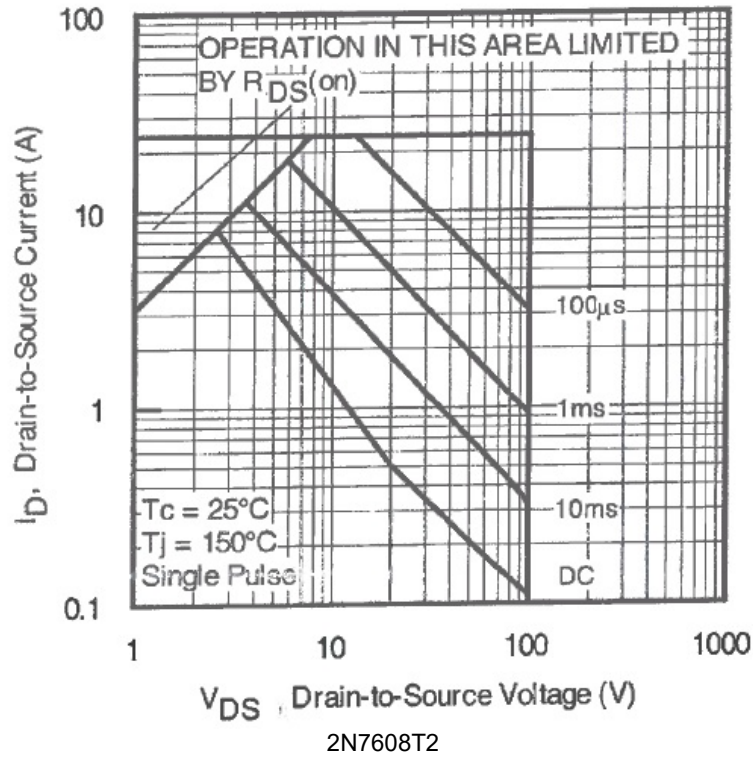


FIGURE 5. Safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

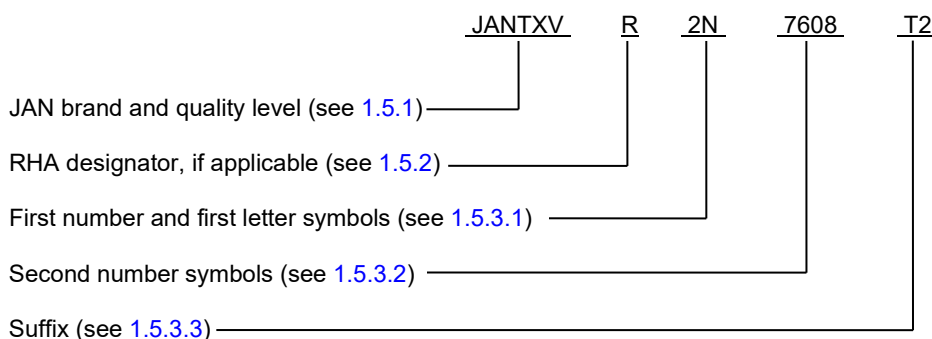
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see 6.7 and table IV), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Weapons Support, Columbus, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <http://qpldocs.dla.mil>.

MIL-PRF-19500/752A
w/AMENDMENT 2

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7608T2	JANTXV#2N7608T2	JANS2N7608T2	JANS#2N7608T2
JANTXV2N7608U8CE	JANTXV#2N7608U8CE	JANS2N7608U8CE	JANS#2N7608U8CE

(1) The number sign (#) represent one of two RHA designators available on this specification sheet ("R" or "F").

* 6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN) (without JAN and RHA prefix). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Generic P/N	Military P/N
IRHLF77110	2N7608T2
IRHLNME77110	2N7609U8CE

6.7 Application data.

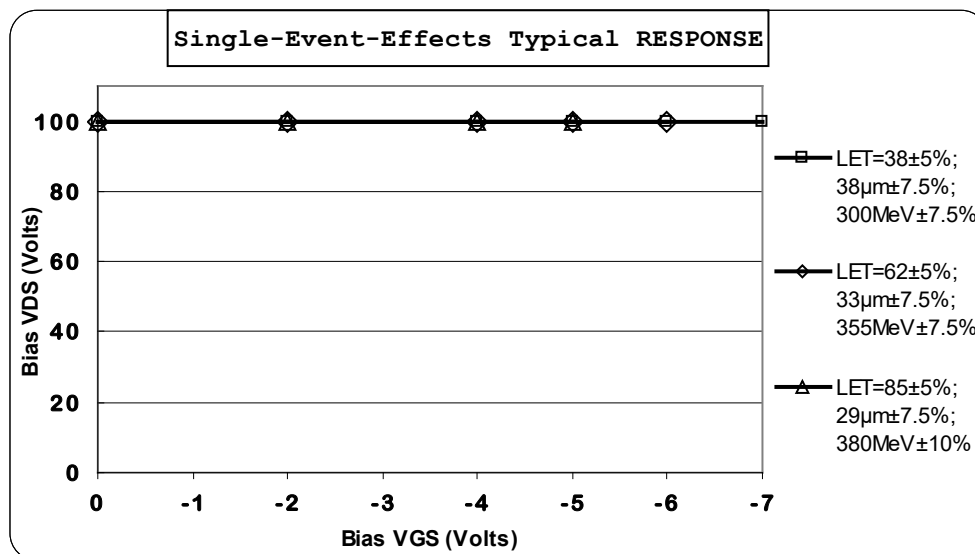
6.7.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

MIL-PRF-19500/752A
w/AMENDMENT 2

TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	Method	MIL-STD-750	Sample plan
			Conditions	
69210 (Applicable to devices with a date code of February 2009 and older)	SEE <u>1/</u>	1080	See figure 6 . IGSSF1, IGSSR1, and IDSS1 in accordance with table I , subgroup 2.	3 devices
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25^\circ \pm 5^\circ \text{C}$	
	2N7608T2, 2N7609U8CE		Surface LET = $38 \text{ MeV-cm}^2/\text{mg} \pm 5.0 \%$, range = $38 \mu\text{m} \pm 7.5\%$, Kr energy = $300 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -7 \text{ V}$ (typical 3.58 MeV/nucleon at Texas A & M Cyclotron) Surface LET = $62 \text{ MeV-cm}^2/\text{mg} \pm 5.0 \%$, range = $33 \mu\text{m} \pm 7.5\%$, Xe energy = $355 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -6 \text{ V}$ (typical 2.75 MeV/nucleon at Texas A & M Cyclotron) Surface LET = $85 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $29 \mu\text{m} \pm 7.5\%$, Au energy = $380 \text{ MeV} \pm 10\%$ In situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -5 \text{ V}$ (typical 1.93 MeV/nucleon at Texas A & M Cyclotron)	
	Electrical measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I , subgroup 2	
			Upon qualification, all manufacturers shall provide the verification test conditions to be added to this table.	

1/ IGSSF1, IGSSR1, and IDSS1 was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option



2N7608T2, 2N7609U8CE

*

FIGURE 6. Typical single event effects safe operating area graph.

* 6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Weapons Support, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil.

* 6.9 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2026-050)

Review activity:
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.