The documentation and process conversion measures necessary to comply with this revision shall be completed by 21 November 2025.

INCH-POUND

MIL-PRF-19500/703E
w/AMENDMENT 3
21 August 2025
SUPERSEDING
MIL-PRF-19500/703E
w/AMENDMENT 2
8 May 2024

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, N-CHANNEL, RADIATION HARDENED, SILICON, ENCAPSULATED (SURFACE MOUNT PACKAGE), TYPES 2N7479, 2N7480, AND 2N7481, JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-Channel, enhancement-mode, MOSFET, radiation hardened, power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.7 for JANHC and JANKC die versions. Provisions for radiation hardness assurance (RHA) to four radiation levels ("R", "F", "G" and "H") are provided for JANTXV and JANS product assurance levels.

1.2 Package outlines. The device package outline is as follows: SMD-0.5 TO-276AA (U3) in accordance with figure 1 for all encapsulated device types.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C =+25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7479U3	75	1.0	1.67	30	30	±20	22	22	22	88	-55 to +150
2N7480U3	75	1.0	1.67	60	60	±20	22	21	22	88	
2N7481U3	75	1.0	1.67	100	100	±20	22	16	22	88	

(1) Derate linearly by 0.6 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

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1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80% of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 12V, I_D = I_{D2}		E_{AS}
					T_J = +25°C	T_J = +150°C	
	V dc	V dc Min	V dc Max	µA dc	Ω	Ω	mJ
2N7479U3	30				0.020	0.040	155
2N7480U3	60	2.0	4.0	10	0.030	0.068	100
2N7481U3	100				0.060	0.115	70

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7479", "7480", and "7481".

1.5.3.3 Suffix letters. The suffix letters "U3" are used on devices that are packaged in the TO-276AA package of figure 1.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

* 1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

For device type 2N7479U3, 2N7480U3, AND 2N7481U3:.....500 krad(Si) 1/

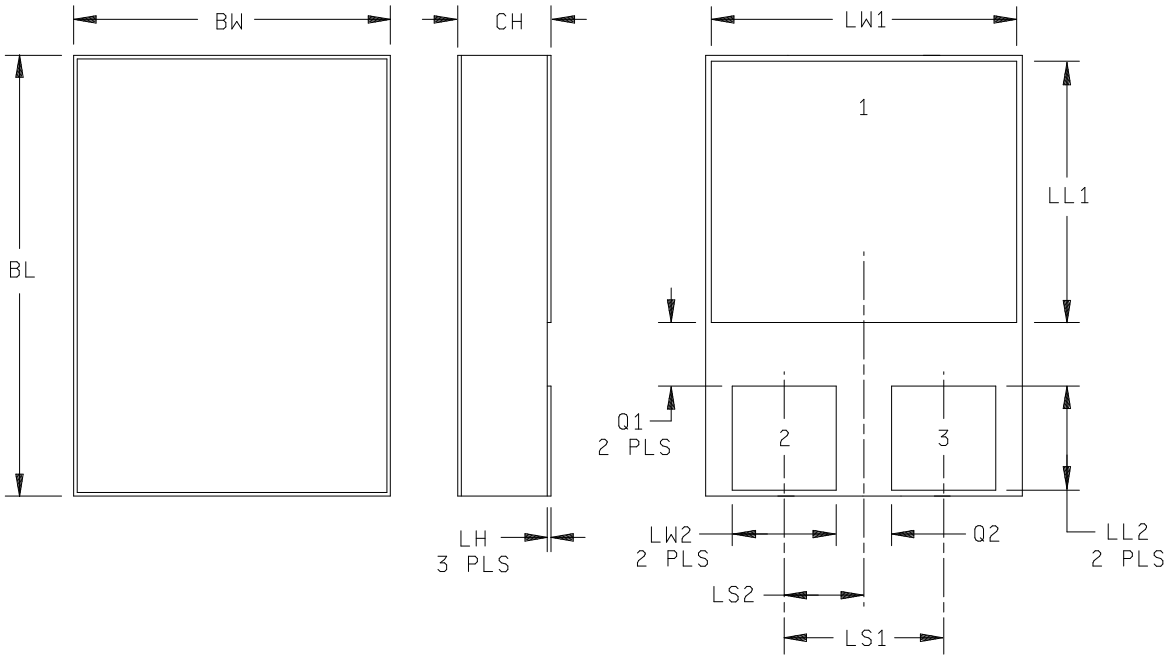
1.6.2 Heavy ion irradiation SEE. SEE testing includes Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR) tests at the specified linear energy transfer (LET) units. See 6.8 for the specific RHA SEE characterization testing details. The following characterization conditions were used for the testing to the requirements herein:

For device type 2N7479:
No SEB and SEGR were observed at surface LET (see table IV) ..... ≤ 84 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 20 V and V_{GS} = -10 V)

For device type 2N7480:
No SEB and SEGR were observed at surface LET (see table IV) ..... ≤ 84 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 14 V and V_{GS} = -20 V)

For device type 2N7481:
No SEB and SEGR were observed at surface LET (see table IV) ..... ≤ 84 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 25 V and V_{GS} = -15 V)

* 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 500 krad(Si).
2/ The manufacturers have performed SEE tests at Brookhaven National Lab Accelerator in accordance with method1080 of MIL-STD-750. For more information on SEE testing and results, customers should contact the qualified manufacturer.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.03	10.29
BW	.291	.301	7.39	7.65
CH	.1085	.124	2.76	3.15
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.92	3.18
LS1	0.150 BSC		3.81 BSC	
LS2	0.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

FIGURE 1. Physical dimensions for TO-276AA (SMD-0.5), U3.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Method Standard Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS}	Rated avalanche current, nonrepetitive
nC	nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-276AA, SMD-0.5, U3) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Multiple chip construction. Multiple chip construction is not permitted to meet the requirements of this specification.

* 3.4.3 Silicone die coat. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883, on each lot of silicone die coating for its intended applications.

* 3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single Event Effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.2.2 Silicone die coating. When silicone die coating is used, method 5011 of MIL-STD-883 shall be performed on that coating in the full MIL-PRF-19500 qualification process.

4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) (4) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.5	Not applicable
9	Subgroup 2 of table I herein, I_{GSSF1}, I_{GSSR1}, I_{DSS1} as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value
17	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $V_{GS(th)1}$, and $r_{DS(ON)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a;
(4) JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V, minimum for t = 250 μS, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance ..... $L = \left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

c. Gate to source resistor R_{GS}..... $25\ \Omega \leq R_{GS} \leq 200\ \Omega$.

d. Supply voltage ..... V_{DD} = 25 V dc, except V_{DD} = 50 V dc for 2N7481U3.

e. Initial case temperature..... T_C = +25° C, -5° C, +10° C.

f. Gate voltage ..... V_{GS} = 12 V dc.

g. Number of pulses to be applied ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage..... 600 V dc.

b. Duration of application of test voltage..... 15 seconds (min).

c. Points of application of test voltage ..... All pads to case.

d. Method of connection..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).

f. Maximum leakage current..... 1.0 mA.

g. Voltage ramp up time..... 500 V/second

4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) or table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM).
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Bond strength, test condition D.

4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5 and B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Terminal strength is not applicable.
C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	Thermal resistance, see 4.3.3, $R_{\theta JC(max)}$ = 1.67ºC/W.
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.4.5.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figure. End-point measurements shall be in accordance with table III.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	Bias condition C, V_{GS} = 0, I_D = 1 mA dc	$V_{(BR)DSS}$			
2N7479U3				30		V dc
2N7480U3				60		V dc
2N7481U3				100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS},	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$			
2N7479U3					0.020	Ω
2N7480U3					0.030	Ω
2N7481U3					0.060	Ω
Forward voltage source drain diode	4011	V_{GS} = 0, condition A, pulsed (see 4.5.1), I_D = I_{D1}	V_{SD}			
2N7479U3					1.2	V dc
2N7480U3					1.2	V dc
2N7481U3					1.2	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7479U3					0.035	Ω
2N7480U3					0.060	Ω
2N7481U3					0.110	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, V_{DD} = 15 V dc (see 4.5.1)	g_{FS}			
2N7479U3				16		S
2N7480U3				16		S
2N7481U3				13		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc, R_G = 2.35 Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		25	ns
Rise time			t_r		100	ns
Turn-off delay time			$t_{D(off)}$		35	ns
Fall time			t_f		30	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4 t_p = 10 ms min. V_{DS} = 80 percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B. $I_D = I_{D1}$, V_{GS} = 12 V dc V_{DD} = 50 percent of rated V_{DS}				
On-state gate charge			$Q_{G(ON)}$			
2N7479U3					65	nC
2N7480U3					45	nC
2N7481U3					50	nC
Gate to source charge			Q_{GS}			
2N7479U3					20	nC
2N7480U3					10	nC
2N7481U3					7.4	nC
Gate to drain charge			Q_{GD}			
2N7479U3					10	nC
2N7480U3					15	nC
2N7481U3					20	nC
Reverse recovery time	3473	Condition A, di/dt = -100 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $I_D = I_{D1}$	t_{rr}			
2N7479U3					102	ns
2N7480U3					125	ns
2N7481U3					250	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point measurements, this test is required for the following subgroups (not intended for 4.3, screen 9 or 11):
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
1/ 2/ 3/	Method	Conditions		R, F, G and H		R, F and G		H 4/		
				Min	Max	Min	Max	Min	Max	
Subgroup 1 Not applicable										
Subgroup 2		T_C = + 25°C								
Steady-state total dose irradiation (V_{GS} bias) 5/	1019	V_{GS} = 12 V; V_{DS} = 0								
Steady-state total dose irradiation (V_{DS} bias) 5/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS}(preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V_{GS} = 0 V; I_D = 1 mA; bias condition C	$V_{(BR)DSS}$							
2N7479U3				30		30		30		V dc
2N7480U3				60		60		60		V dc
2N7481U3				100		100		100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = 1 mA	$V_{GS(th)1}$	2.0	4.0	2.0	4.0	1.5	4.0	V dc
Gate current	3411	V_{GS} = +20 V; V_{DS} = 0 bias condition C	I_{GSSF1}		100		100		100	nA dc
Gate current	3411	V_{GS} = -20 V; V_{DS} = 0 bias condition C	I_{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V_{GS} = 0, V_{DS} = 80 percent of rated V_{DS} (preirradiation) bias condition C	I_{DSS}		10		10		25	µA dc
Static drain to source on-state voltage	3405	V_{GS} = 12 V; I_D = I_{D2} condition A pulsed (see 4.5.1)	$V_{DS(on)}$							
2N7479U3					0.440		0.440		0.550	V dc
2N7480U3					0.630		0.630		0.903	V dc
2N7481U3					0.960		0.960		1.200	V dc
Forward voltage source drain diode	4011	V_{GS} = 0; I_D = I_{D1} bias condition A	V_{SD}		1.2		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
* 4/ The H designation represents devices which pass end-points at all 100k, 300k, 500k and 1000k rad (Si).
5/ Separate samples shall be pulled for each bias.
6/ Group D samples are built and tested in T0-3 packages. The equivalent pre-radiation and post radiation limit for VDS(on) in the T0-3 package is 0.528 V dc for the 2N7479U3 (R ,F, and G), 0.714 V dc for the 2N7480U3 (R ,F, and G), 1.024 V dc for the 2N7481U3 (R ,F, and G). The equivalent 1,000kRad (H) post radiation limit for VDS(on) in the T0-3 package 0.660 V dc for the 2N7479U3, 0.903 V dc for the 2N7480U3, and 1.280 V dc for the 2N7481U3.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		Table I, subgroup 2 herein.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Not applicable			
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
Subgroup 11			3 devices
SEE 2/ 3/	1080	See FIGURE 5.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level linear energy transfer (LET) is sufficient to qualify all lower level LET's.

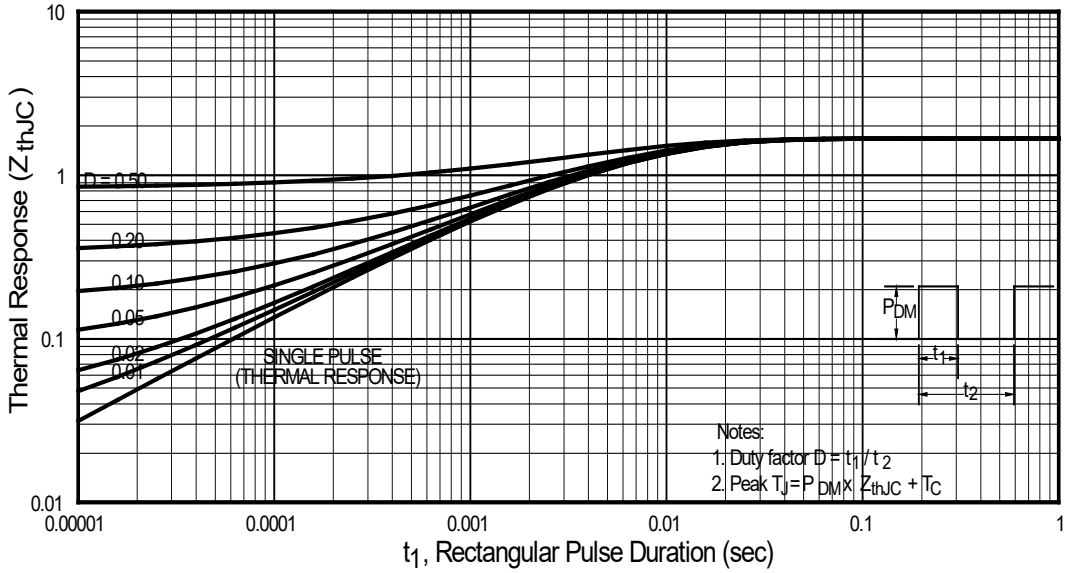
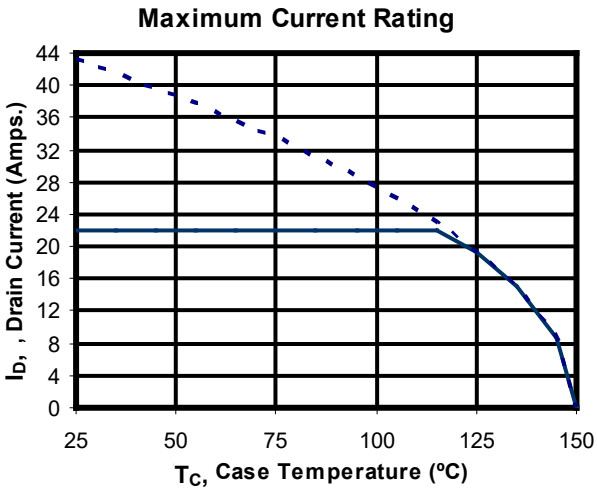
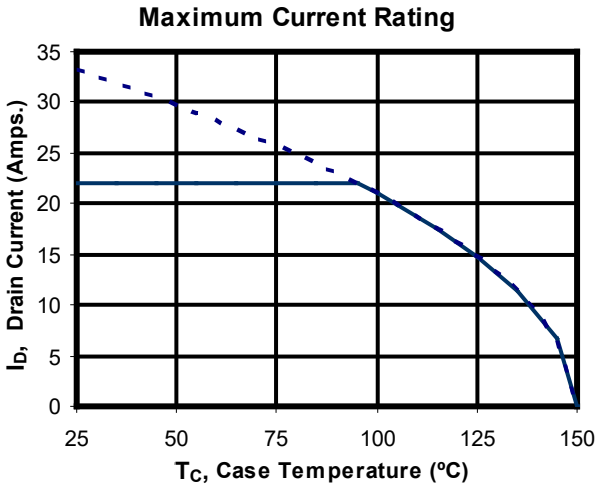


FIGURE 2. Thermal response curve.

2N7479U3



2N7480U3



2N7481U3

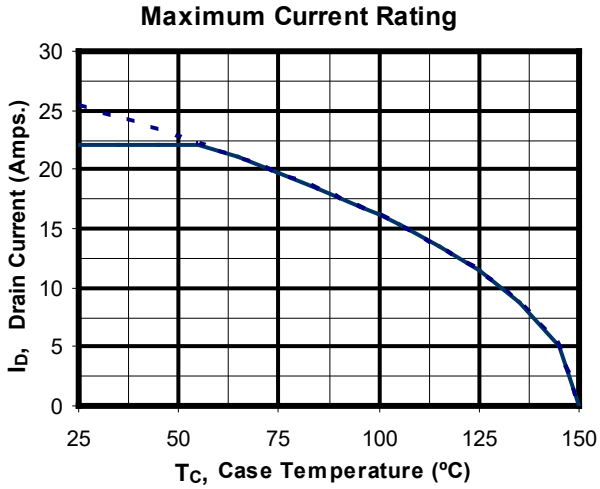
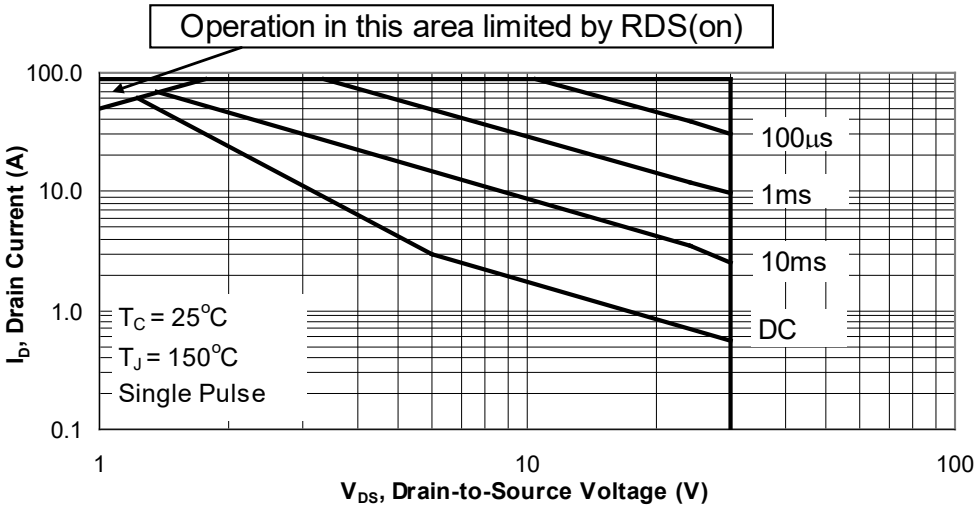
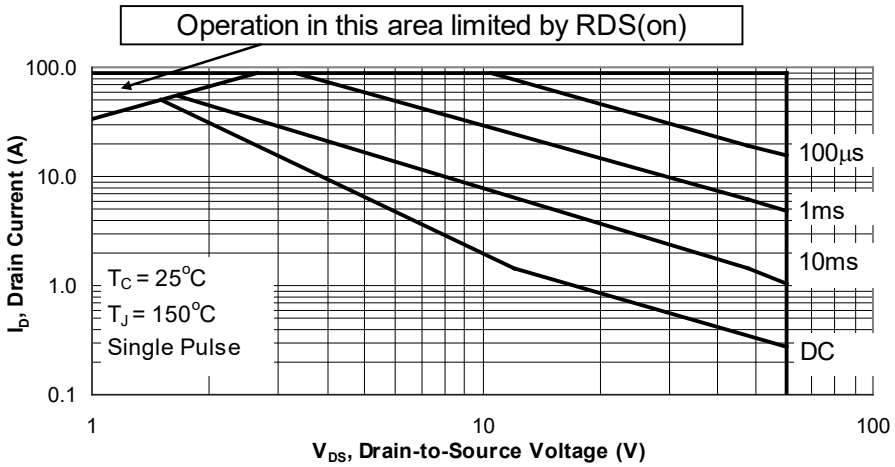


FIGURE 3. Maximum drain current versus case temperature graphs.

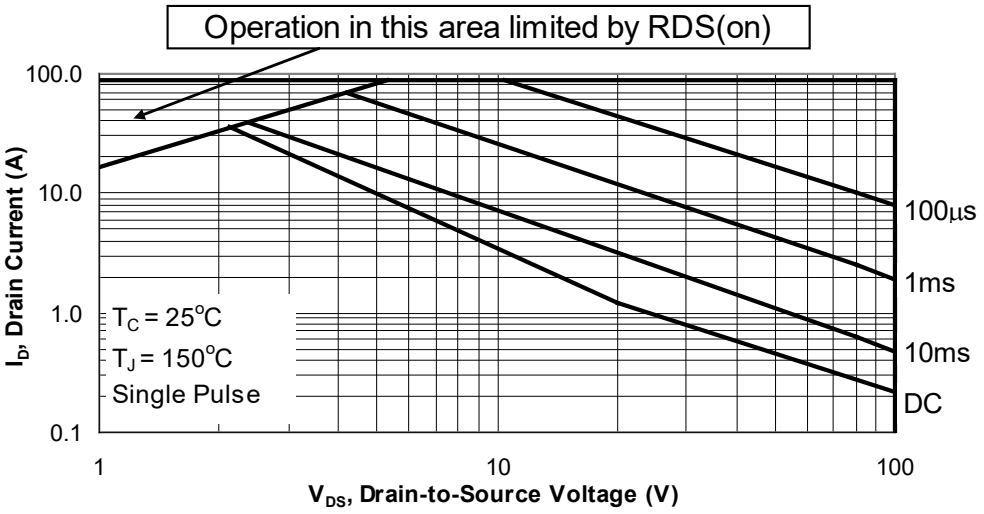


2N7479U3



2N7480U3

FIGURE 4. Safe operating area graph.



2N7481U3

FIGURE 4. Safe operating area graphs - continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

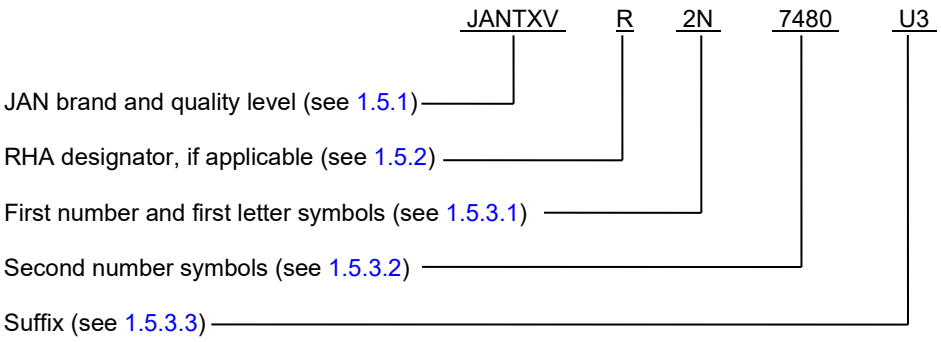
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

f. If SEE testing data is desired, it should be specified in the contract or order.

g. If specific SEE characterization conditions are desired (see section 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7479U3	JANTXV#2N7479U3	JANS2N7479U3	JANS#2N7479U3
JANTXV2N7480U3	JANTXV#2N7480U3	JANS2N7480U3	JANS#2N7480U3
JANTXV2N7481U3	JANTXV#2N7481U3	JANS2N7481U3	JANS#2N7481U3

(1) The number sign (#) represents one of four RHA designators available on this specification sheet ("R", "F", "G" or "H").

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHNJ57Z30	2N7479U3
IRHNJ57034	2N7480U3
IRHNJ57130	2N7481U3

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

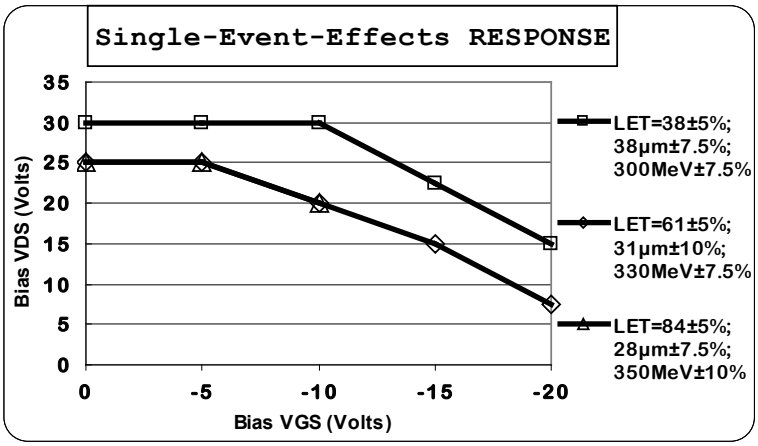
Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5.	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C Surface LET = 38 MeV-cm^2/mg ±5%, range = 38 µm ±7.5%, Br ion energy = 300 MeV ±7.5%	
	2N7479U3		In-situ bias conditions: V_{DS} = 30 V and V_{GS} = -10 V V_{DS} = 22.5 V and V_{GS} = -15 V V_{DS} = 15 V and V_{GS} = -20 V (nominal 3.80 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7480U3		In-situ bias conditions: V_{DS} = 60 V and V_{GS} = -15 V V_{DS} = 30 V and V_{GS} = -20 V (nominal 3.80 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7481U3		In-situ bias conditions: V_{DS} =100 V and V_{GS} = -20 V (nominal 3.80 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 61 MeV-cm2/mg ±5%, range = 31 µm ±10%, I ion energy = 330 MeV ±7.5%	
	2N7479U3		In-situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V V_{DS} = 20 V and V_{GS} = -10 V V_{DS} = 15 V and V_{GS} = -15 V V_{DS} = 7.5 V and V_{GS} = -20 V (nominal 2.60 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7480U3		In-situ bias conditions: V_{DS} = 46 V and V_{GS} = -5 V V_{DS} = 35 V and V_{GS} = -10 V V_{DS} = 25 V and V_{GS} = -15 V V_{DS} = 15 V and V_{GS} = -20 V (nominal 2.60 MeV/nucleon at Brookhaven National Lab Accelerator)	

See footnotes at end of table.

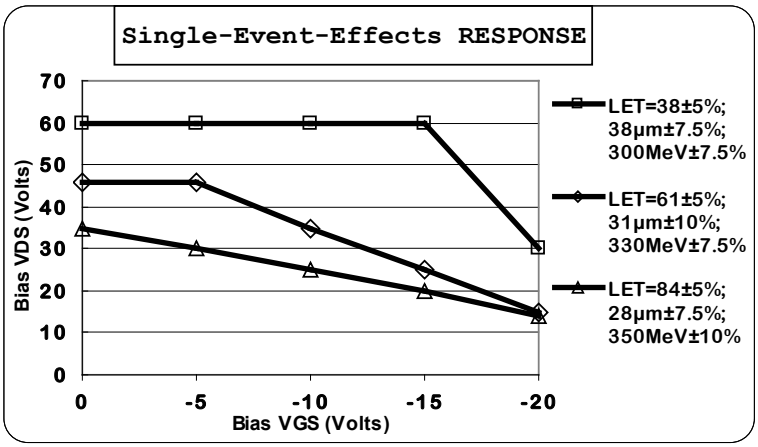
TABLE IV. Manufacturers characterization conditions - Continued.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
	2N7481U3		In-situ bias conditions: V_{DS} = 100 V and V_{GS} = -10 V V_{DS} = 35 V and V_{GS} = -15 V V_{DS} = 25 V and V_{GS} = -20 V (nominal 2.60 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 84 MeV-cm2/mg ± 5%, range = 28 µm ±7.5%, Au ion energy = 350 MeV ±10%	
	2N7479U3		In-situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V V_{DS} = 20 V and V_{GS} = -10 V (nominal 1.78 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7480U3		In-situ bias conditions: V_{DS} = 35 V and V_{GS} = 0 V V_{DS} = 30 V and V_{GS} = -5 V V_{DS} = 25 V and V_{GS} = -10 V V_{DS} = 20 V and V_{GS} = -15 V V_{DS} = 14 V and V_{GS} = -20 V (nominal 1.78 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7481U3		In-situ bias conditions: V_{DS} = 100 V and V_{GS} = -5 V V_{DS} = 80 V and V_{GS} = -10 V V_{DS} = 25 V and V_{GS} = -15 V (nominal 1.78 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers should provide the verification test conditions to be added to this table.				

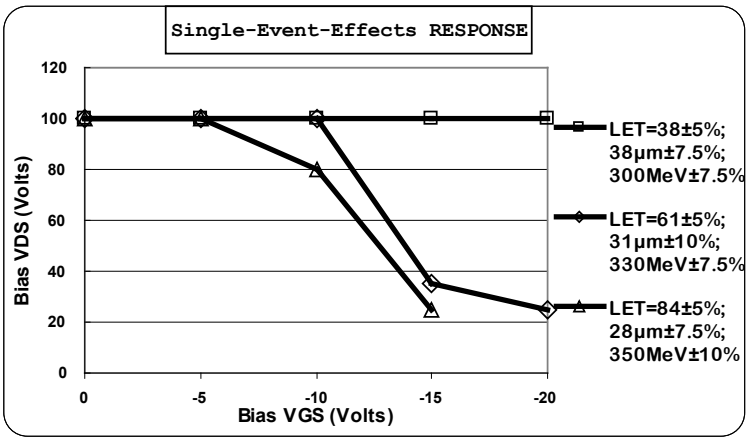
1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.



2N7479U3



2N7480U3



2N7481U3

FIGURE 5. SEE safe operating area graph.

* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil.

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AV, MI
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2025-078)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.