

The documentation and process conversion measures necessary to comply with this revision shall be completed by 3 May 2012.

INCH-POUND

MIL-PRF-19500/688B
3 February 2012
SUPERSEDING
MIL-PRF-19500/688A
10 August 2007

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT TRANSISTOR, N-CHANNEL,
SILICON, TYPES 2N7002, 2N7002T2, AND 2N7002UB,
JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, low-threshold logic level, high frequency, high switching speed MOSFET, transistor. Four levels of product assurance are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Physical dimensions. See [figure 1](#) (TO-18), [figure 2](#) (TO-205AD), and [figure 3](#) (UB).

* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^{\circ}\text{C}$.

Types	P_T $T_A = +25^{\circ}\text{C}$	P_T $T_C = +25^{\circ}\text{C}$	P_T (1) $T_{SP(1S)} = +25^{\circ}\text{C}$	$R_{\theta JA}$	$R_{\theta JC}$	$R_{\theta JSP(1S)}$
	<u>mW</u>	<u>W</u>	<u>W</u>	<u>$^{\circ}\text{C/W}$</u>	<u>$^{\circ}\text{C/W}$</u>	<u>$^{\circ}\text{C/W}$</u>
2N7002	(1) 500	1.0	N/A	(2) 325	150	N/A
2N7002T2	800	(1) 5	N/A	(2) 175	(2) 30	N/A
2N7002UB	(1) 500	N/A	1.5	325	N/A	(2) 90

Type	V_{DS}	V_{GS}	I_{D1} (3) $T_C = +25^{\circ}\text{C}$	I_{D2} (3) $T_C = +100^{\circ}\text{C}$	I_{DM}	T_J and T_{STG}
	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>$^{\circ}\text{C}$</u>
2N7002	60	± 40	0.2	0.073	0.8	-65 to +200
2N7002T2			1.2	0.49	4	
2N7002UB			0.7	0.29	2.4	

- (1) For derating, see [figures 4, 5, and 6](#).
- (2) For thermal curves, see [figures 7, 8, 9, and 10](#).
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil/>.

1.4 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)} \text{ DSS}$ $V_{GS} = 0 \text{ V}$ $I_D = 10 \mu\text{A dc}$	$V_{GS} \text{ (th)1}$ $V_{DS} = V_{GS}$ $I_D = 0.25 \text{ mA dc}$	Max I_{DSS1} $V_{GS} = 0 \text{ V}$ $V_{DS} = 60$ percent of rated V_{DS}	Max $r_{DS(on)} \text{ (1)}$ $V_{GS} = 10 \text{ V dc}$	
				$T_J = +25^\circ\text{C}$ at I_{D1}	$T_J = +125^\circ\text{C}$ at I_{D2}
2N7002, T2, UB	<u>V dc</u>	<u>V dc</u> <u>Min</u> <u>Max</u>	<u>$\mu\text{A dc}$</u>	<u>Ohm</u>	<u>Ohm</u>
	60	1 2.5	0.1	4	13.5

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

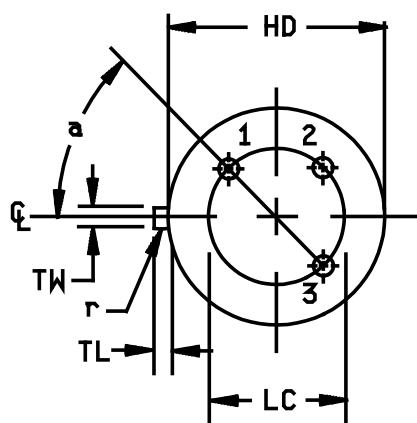
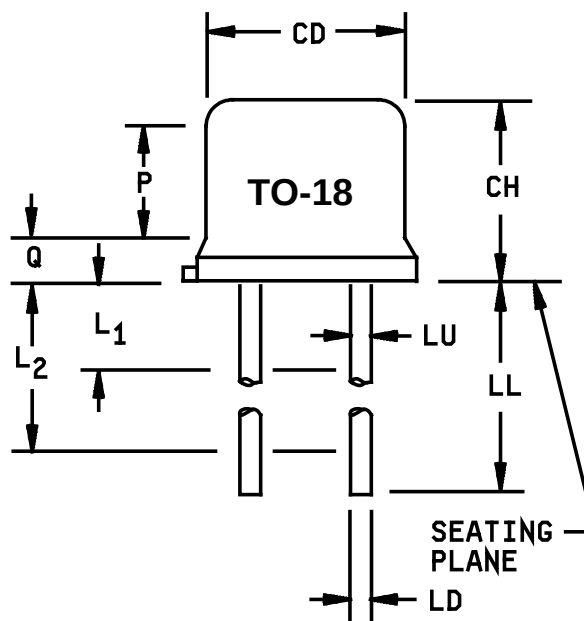
DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or <https://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L ₁		.050		1.27	7,8
L ₂	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12					



NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
- * 6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. The drain shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
12. Lead 1 = source, lead 2 = gate, lead 3 = drain.

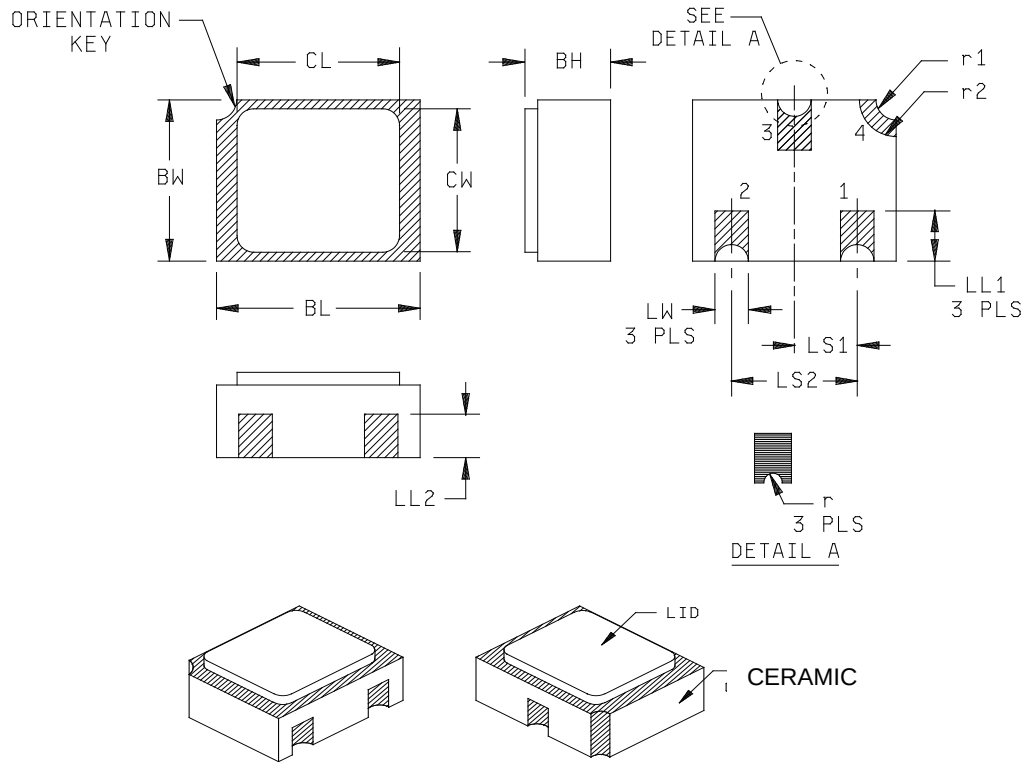
* FIGURE 1. Physical dimensions, 2N7002, TO-206AA (formerly TO-18).

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
TW	.028	.034	0.71	0.86	2
TL	.029	.045	0.74	1.14	3
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LC	.200 TP		5.08 TP		6
LU	.016	.019	0.41	0.48	7,8
L ₁		.050		1.27	7,8
L ₂	.250		6.35		7,8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	9
α	45 TP		45 TP		6

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, TW shall be held for a minimum length of .011 (0.028 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 + .001, - .000 (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 (0.18 mm) radius of true position (TP) at MMC relative to tab at MMC.
7. LU applies between L₁ and L₂. LD applies between L₂ and L minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
10. Drain is electrically connected to the case.
11. Lead 1 = source, lead 2 = gate, lead 3 = drain.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 2. Physical dimensions 2N7002T2, (TO-205AD) - Continued.



Symbol	Dimensions				Note 1,2,3,4
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		0.20	
r1		.012		0.31	
r2		.022		0.56	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas. Lid on package is a metallized area.
4. Pad 1 = Gate, Pad 2 = Source, Pad 3 = Drain, Pad 4 = shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 3. Physical dimensions, 2N7002UB, surface mount (UB version).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and [figure 1](#) (TO-205AD), [figure 2](#), and [figure 3](#) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#) herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTX and JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.2)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.2)
9	I_{DSS1} , I_{GSSF1} , I_{GSSR1} , subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ of subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 1$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ of subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ of subgroups 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 1$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value, or 0.5 ohm, whichever is greater.. $\Delta V_{GS(TH)1} = \pm 10$ percent of initial value or ± 0.3 V dc.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ of subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 1$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value, or 0.5 ohm, whichever is greater.. $\Delta V_{GS(TH)1} = \pm 10$ percent of initial value or ± 0.3 V dc.

(1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.

(2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.

* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 24$ V minimum for $t = 250$ μ s minimum.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table III](#), group E, subgroup 4 herein.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#), and herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein. Delta measurements shall be in accordance with [table III](#) herein.

4.4.2.1 Group B inspection table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition C.
B4	1042	Test condition D; 2,000 cycles. The heating cycle shall be 1 minute minimum.
B5	1042	Accelerated steady-state reverse bias power; test condition A, $V_{DS} = \text{rated}$ $T_A = +175^\circ\text{C}$ minimum, $t = 120$ hours.
B5	1042	Accelerated steady-state gate stress; condition B, $V_{GS} = \text{rated}$, $T_A = +175^\circ\text{C}$ minimum, $t = 24$ hours.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX and JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition C, 25 cycles.
B3	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum; accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with table III herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, (not applicable for surface mount devices).
C5	3161	See 4.3.2, $R_{\theta JA}$ and $R_{\theta JC}$ = (see 1.3).
C6	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 48 hours minimum; or T_A = +150°C, t = 96 hours minimum. and accelerated steady-state reverse bias, condition A, V_{DS} = rated;

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3161	See 4.3.2	$Z_{\theta JC}$			$^{\circ}\text{C/W}$
Breakdown voltage drain to source	3407	$V_{GS} = 0$, $I_D = 10 \mu\text{A}$ dc, bias condition C	$V_{(BR)DSS}$	60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 250 \mu\text{A}$ dc	$V_{GS(TH)1}$	1	2.5	V dc
Gate current	3411	$V_{GS} = +15$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+10	nA dc
Gate current	3411	$V_{GS} = -15$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-10	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 60$ V	I_{DSS1}		100	nA dc
Drain to source on-state voltage	3405	$V_{GS} = 10$ V dc, condition A, $I_D = 0.8$ A, pulsed (see 4.5.1)	$V_{DS(ON)1}$		7.5	V
Drain to source on-state voltage	3405	$V_{GS} = 5.5$ V dc, condition A, $I_D = 0.3$ A, pulsed (see 4.5.1)	$V_{DS(ON)2}$		10	V
Static drain to source on-state resistance	3421	$V_{GS} = 10$ V dc, condition A, pulsed (see 4.5.1), $I_D = 0.250$ A dc	$r_{DS(ON)1}$		4	Ω
Static drain to source on-state resistance	3421	$V_{GS} = 5.5$ V dc, condition A, pulsed (see 4.5.1), $I_D = 0.200$ A dc	$r_{DS(ON)2}$		6	Ω
Forward voltage	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}	0.7	1.2	V (pk)

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation		T _C = T _J = +125°C				
Gate current	3411	V _{GS} = ±20 V dc, bias condition C, V _{DS} = 0	I _{GSS2}		±500	nA dc
Drain current	3413	V _{GS} = 0, bias condition C, V _{DS} = 60 V	I _{DSS2}		10	µA dc
Drain to source on-state voltage	3405	V _{GS} = 10 V dc, condition A; pulsed (see 4.5.1), I _D = 0.5 A dc	V _{DS(ON)3}		6.5	V
Static drain to source on-state resistance	3421	V _{GS} = 10 V dc, condition A, pulsed (see 4.5.1), I _D = 0.5 A dc	r _{DS(ON)3}		13.5	Ω
Gate to source voltage (threshold)	3403	V _{DS} = V _{GS} , I _D = 250 mA dc	V _{GS(TH)2}	1.0	2.5	V dc
Low temperature operation		T _C = T _J = -55°C				
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS(TH)3} , I _D = 1 mA dc	V _{GS(TH)3}		2.5	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	V _{DS} = V _{GS} = 10 V dc, I _D = 0.2 A, pulsed (see 4.5.1)	g _{FS}	80		mS
Switching time test	3472	R _{gen} = 50 Ω, R _{GS} = 50 Ω,				
Turn-on delay time		V _{DD} = 30 V dc, I _D = 200 mA dc	t _{D(on)}		20	ns
Turn-off delay time		V _{DD} = 30 V dc, I _D = 200 mA dc	t _{D(off)}		20	ns
Small signal common source short-circuit input capacitance	3431	V _{DS} = 25 V dc, V _{GS} , = 0 V; f = 1 MHz	C _{iss}		50	pF
Small signal common source short-circuit output capacitance		V _{DS} = 25 V dc, V _{GS} , = 0 V; f = 1 MHz	C _{oss}		25	pF
Small signal common source short-circuit reverse transfer capacitance		V _{DS} = 25 V dc, V _{GS} , = 0 V; f = 1 MHz	C _{rss}		5	Pf

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 5</u> Safe operating area test Electrical measurements <u>Subgroups 6 and 7</u> Not applicable	3474	$V_{DS} = 80$ percent of rated V_{DS} (see 1.3) See table I , subgroup 2				

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:

Group B, subgroups 3 and 4 (JANS).

Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).

Group C, subgroup 2 and 6.

Group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Electrical measurements		See table I , subgroup 2. see table III herein.	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A; 1,000 hours.	
Electrical measurements		See table I subgroup 2.	
Steady-state gate bias	1042	Condition B; 1,000 hours.	
Electrical measurements		See table I subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			22 devices, c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

1/ A separate sample may be pulled for each test condition.

TABLE III. Group B, C, and E delta measurements. 1/ 2/ 3/ 4/

Step	Inspection <u>5/</u>	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
1.	Gate current	3411	Bias condition C; $V_{DS} = 0$ V $V_{GS} = +15$ V dc and -15 V dc	ΔI_{GSS}	± 10 nA dc or 100 percent of initial value, whichever is greater.		
2.	Drain cut off current	3413	Bias condition C; $V_{DS} = +60$ V, $V_{GS} = 0$ V dc	ΔI_{DSS}	± 1 μ A dc or 100 percent of initial value, whichever is greater.		
3.	Small signal, drain to source on-state resistance	3423	$V_{GS} = 5$ V dc; condition A, pulsed (see 4.5.1); $I_D = .2$ mA dc	$\Delta r_{DS(on)}$	± 0.5 ohm or ± 20 percent of initial value, whichever is greater.		
4.	Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$; $I_D = 0.25$ mA dc	$\Delta V_{GS(th)}$	± 10 percent of initial value or ± 0.3 V dc, whichever is greater.		
5.	Thermal impedance	3161	See 4.3.1	$\Delta Z_{\theta JX}$	± 10 percent of initial value, see figures 7, 8, 9, and 10		

1/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows:

- Subgroup 3, see table III herein, step 1, 2, 3, 4, and 5.
- Subgroup 4, see table III herein, step 1, 2, 3, 4, and 5.

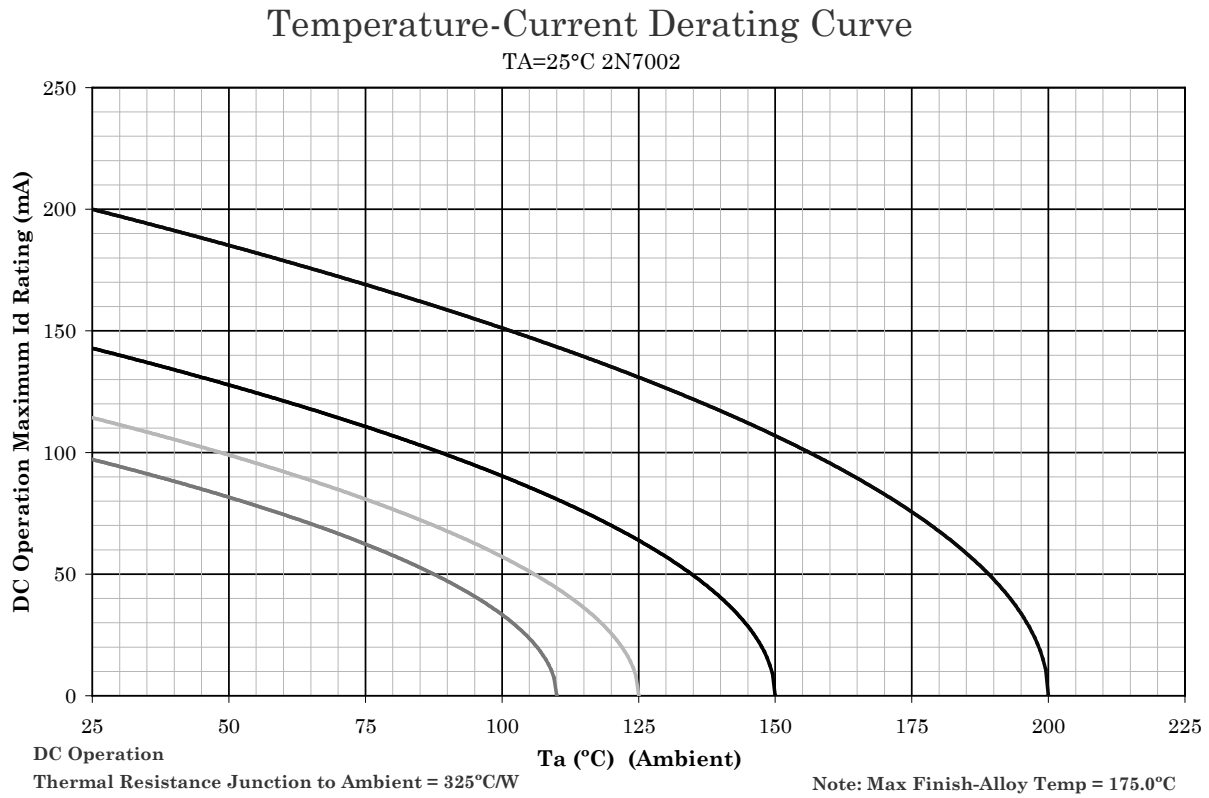
2/ The delta measurements for table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500 are as follows:

- Subgroup 3, see table III herein, step 1, 2, 3, 4, and 5.

3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, see table III herein, step 5.

4/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows: Subgroup 1, see table III herein, step 1, 2, 3, 4, and 5.

5/ See MIL-PRF-19500 for sampling plan.



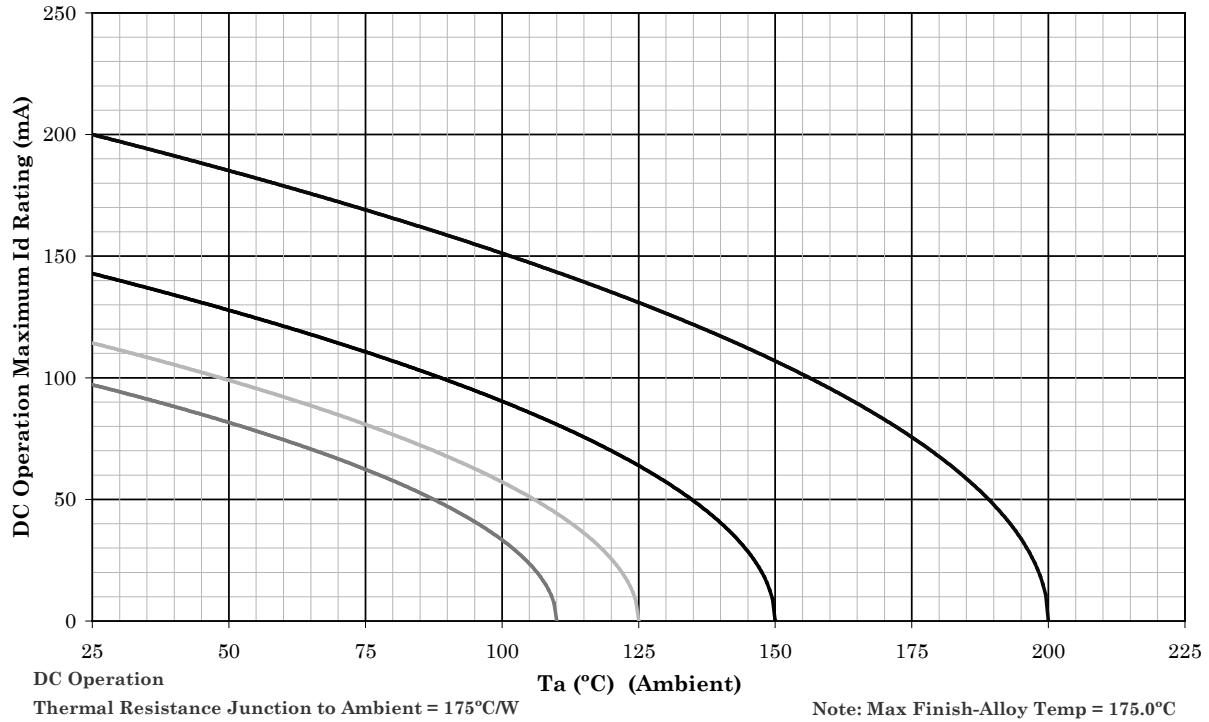
NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$ and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 4. Derating for 2N7002 ($R_{\theta JA}$) TO-18.

Temperature-Current Derating Curve

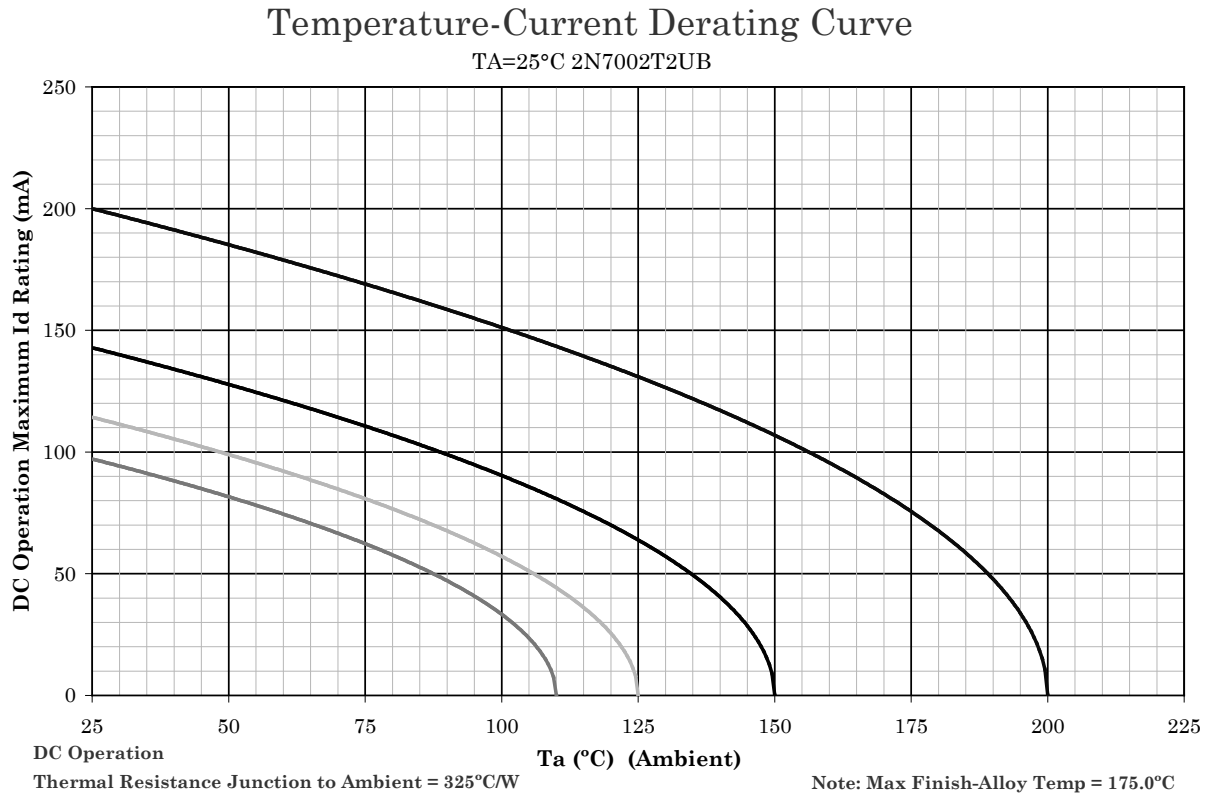
TA=25°C 2N7002T2



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$ and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 5. Derating for 2N7002T2 ($R_{\theta JA}$) TO-39.



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$ and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 6. Derating for 2N7002UB ($R_{\theta JA}$).

MAXIMUM THERMAL IMPEDANCE
2N7002 TO-18 WITH 0.125" LEAD MOUNT TO PCB, $P_t = 500\text{mW}$.

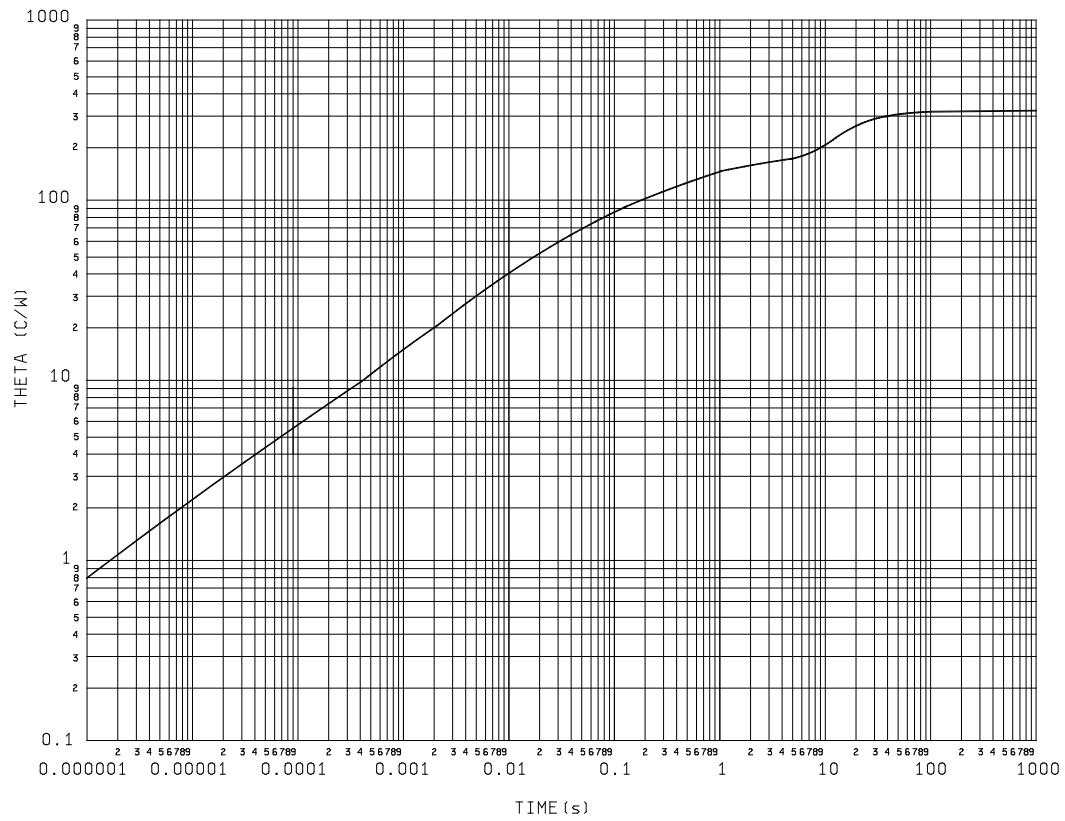


FIGURE 7. Thermal impedance graph ($R_{\theta JA}$) for 2N7002 (TO-18).

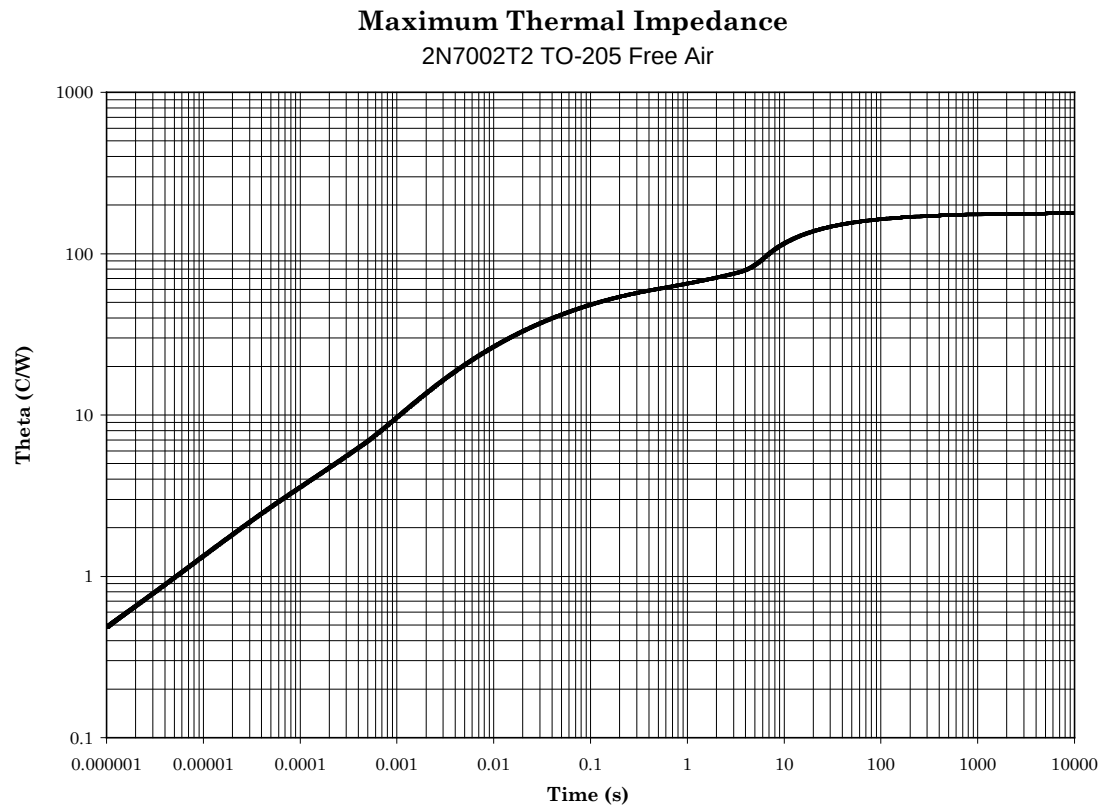


FIGURE 8. Thermal impedance graph ($R_{\theta JA}$) for 2N7002T2 (TO-205AD).

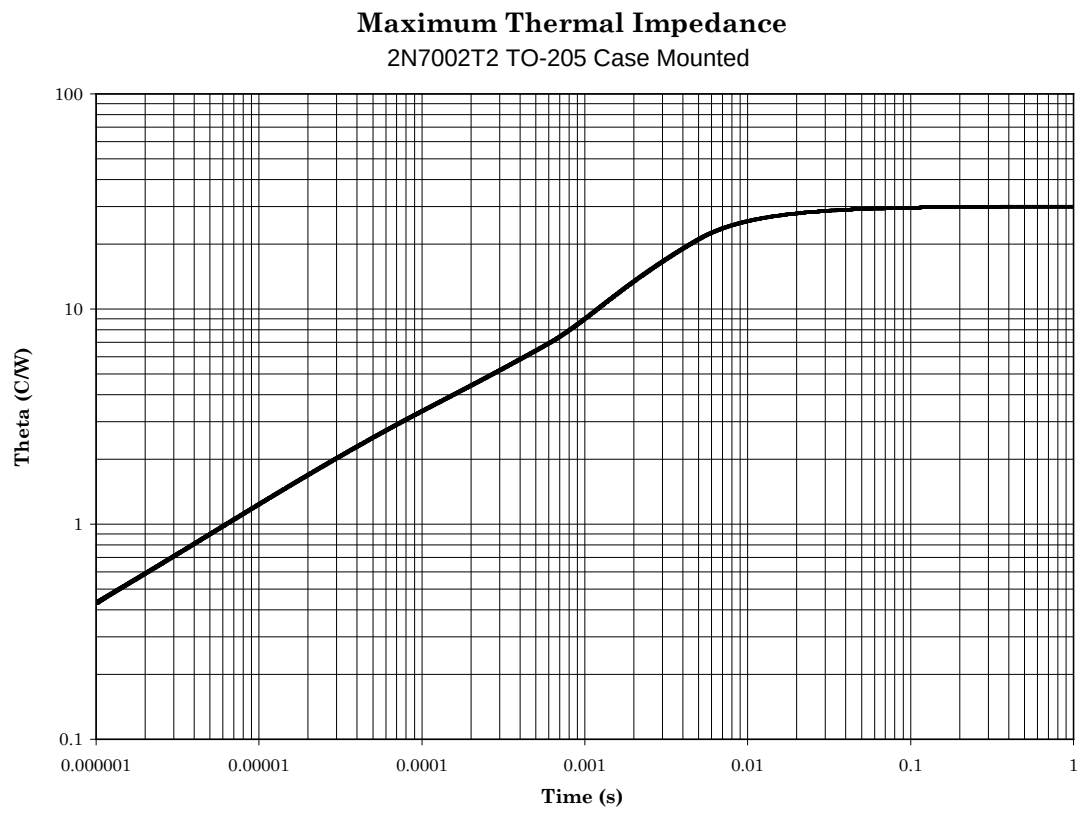


FIGURE 9. Thermal impedance graph ($R_{\theta JC}$) for 2N7002T2 (TO-205AD).

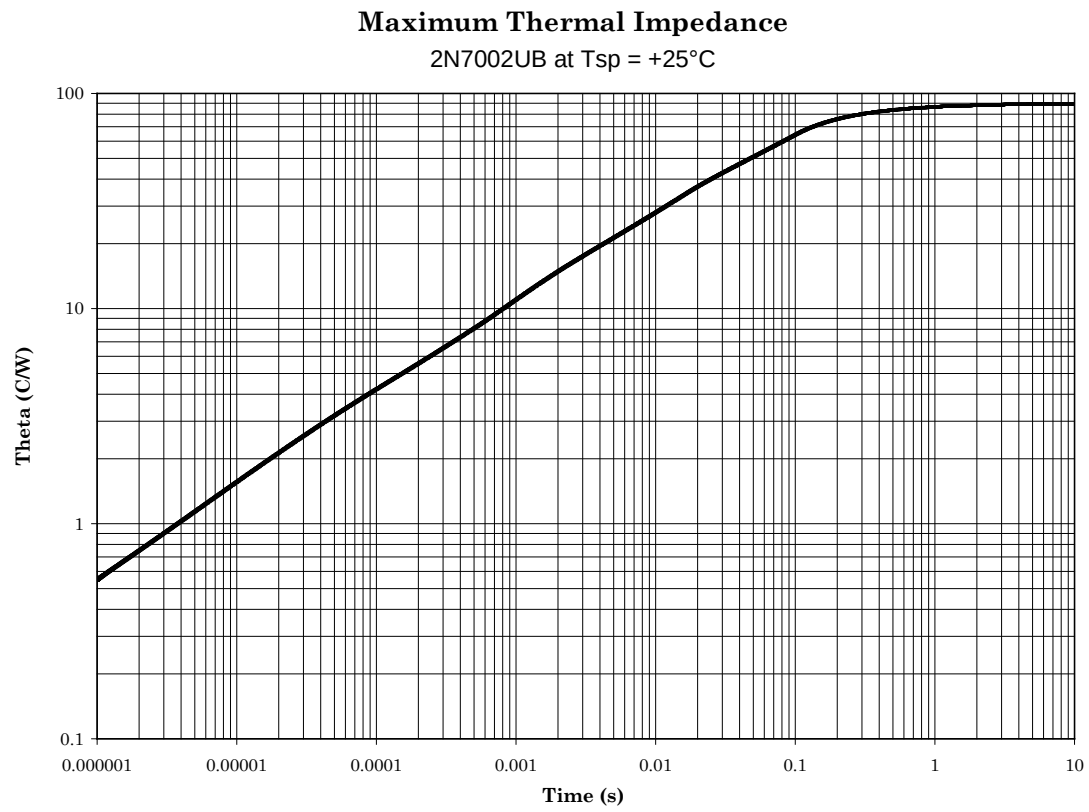


FIGURE 10. Thermal impedance graph ($R_{\theta JSP(tS)}$) for 2N7002UB (UB).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

* 6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2011-077)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil/> .