The documentation and process conversion measures necessary to comply with this revision shall be completed by 23 November 2022.

INCH-POUND

MIL-PRF-19500/663G
w/AMENDMENT 1
23 August 2022
SUPERSEDING
MIL-PRF-19500/663G
14 July 2017

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED,
N-CHANNEL, SILICON, TYPES 2N7431, 2N7432, AND 2N7433,
JANTXVR, F, G, AND H; AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Provisions for radiation hardness assurance (RHA) to four radiation levels ("R", "F", "G" and "H") are provided for JANS and JANTXV product assurance levels. See 6.7 for and JANHC and JANKC die versions. See 6.8 for surface mount versions.

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with figure 1 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4)	I_{D2} T_C = +100°C (3) (4)	I_S	I_{DM}	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7431	250	3.0	0.5	60	60	±20	35.0	35.0	35.0	140	-55
2N7432	250	3.0	0.5	100	100	±20	35.0	35.0	35.0	140	to
2N7433	250	3.0	0.5	200	200	±20	35.0	25.0	35.0	140	+150

(1) Derate linearly by 2.0 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A
FSC 5961

* DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc T_J = +25°C at I_{D2}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc T_J = +150°C at I_{D2}	E_{AS} at I_{D1}	I_{AS}
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7431	60	2.0	4.0	25	0.021	0.040	500	35.0
2N7432	100	2.0	4.0	25	0.045	0.105	500	35.0
2N7433	200	2.0	4.0	25	0.070	0.175	500	35.0

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JANTXV” and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7431", "7432", and "7433".

1.5.3.3 Suffix letters. No suffix letters are used on devices that are packaged in the TO-254AA package of figure 1.

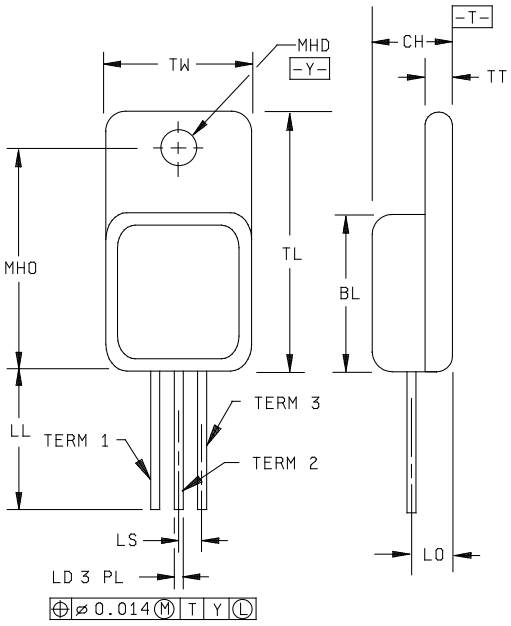
1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

* 1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

For device type 2N7431, 2N7432, 2N7433: ..... 500 krads(Si) 1/

* 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 500 krads(Si).



Ltr	Inches	Inches	mm	mm	Notes
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
* 5. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-254AA.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
* MIL-STD-883 - Test Method Standard for Microcircuits

* (Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS} ..... Rated avalanche current, nonrepetitive
nC ..... nano Coulomb.

3.4 Interface and physical dimensions. The Interface and physical dimensions shall be as specified in MIL-PRF-19500, figure 1 (TO-254AA) herein. Methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction is not permitted in this specification.

* 3.4.3 Silicone die coating. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each silicone lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

* 3.7 Electrostatic discharge sensitive (ESDS). The devices covered by this specification have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.2.2 Silicone die coating. The successful completion of method 5011 of MIL-STD-883 on silicon die coating shall be part of the full MIL-PRF-19500 qualification process.

* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
* 5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, I_{GSSR1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
17	Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $V_{GS(th)1}$, and $r_{DS(on)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy E_{AS}.

a. Peak current (I_{AS}) ..... $I_{AS} = I_{D1}$.

b. Peak gate voltage (V_{GS})..... 12 V.

c. Gate to source resistor (R_{GS})..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance ..... $L = (2E_{AS}/(I_{D1})^2)*((V_{BR}-V_{DD})/V_{BR})$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V (50 V for 2N7433).

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table III, group E, subgroup 4 herein.

* 4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

a. Magnitude of test voltage……900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……All leads to case (bunch connection).

d. Method of connection……Mechanical.

e. Kilovolt-ampere rating of high voltage source……..1,200V /1.0 mA (min).

f. Maximum leakage current……1.0 mA.

g. Voltage ramp up time……500V /second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

	Subgroup	Method	Condition
	B3	1051	Test condition G, 100 cycles.
	B3	2075	See 3.4.2.
	B3	2077	SEM qualification may be performed anytime prior to lot formation.
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	B4	1042	Test condition D. The heating cycle shall be 30 seconds minimum.
	B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours minimum.
	B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours minimum.
	B5	2037	Bond strength; test condition D.

4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Test condition D, 2,000 cycles. The heating cycle shall be 30 seconds minimum.
B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

	Subgroup	Method	Condition
*	C2	2036	Test condition A, weight = 10 pounds (4.54 kg); t = 15 s.
*	C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	C5	3161	See 4.3.3, $R_{\theta JC(max)}$ = 0.50°C/W.
	C6	1042	Test condition D. The heating cycle shall be 30 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0 V, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7431				60		V dc
2N7432				100		V dc
2N7433				200		V dc
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+ 100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		- 100	nA dc
Drain current	3413	V_{GS} = 0 V dc, Bias condition C V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(on)1}$			
2N7431					0.021	ohm
2N7432					0.045	ohm
2N7433					0.070	ohm
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), I_D = I_{D1}	$r_{DS(on)2}$			
2N7431					0.021	ohm
2N7432					0.045	ohm
2N7433					0.077	ohm
Forward voltage	4011	Pulsed (see 4.5.1), condition A, I_D = I_{D1}, V_{GS} = 0 V dc	V_{SD}			
2N7431					1.5	V dc
2N7432					1.8	V dc
2N7433					1.8	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate current	3411	V_{GS} = +20 and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V; bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		0.25	mA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7431					0.034	ohm
2N7432					0.089	ohm
2N7433					0.140	ohm
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7431				18		S
2N7432				16		S
2N7433				9		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc, R_G = 2.35 Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7431					27	ns
2N7432					35	ns
2N7433					50	ns
Rise time			t_r			
2N7431					120	ns
2N7432					150	ns
2N7433					200	ns
Turn-off delay time			$t_{d(off)}$			
2N7431					120	ns
2N7432					150	ns
2N7433					200	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Fall time			t_f			
2N7431					100	ns
2N7432					130	ns
2N7433					130	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figures 4, 5, and 6; t_p = 10 ms minimum, V_{DS} = 80 percent of maximum rated V_{DS}, ($V_{DS} \leq 200$)				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7431					270	nC
2N7432					310	nC
2N7433					290	nC
Gate to source charge			Q_{gs}			
2N7431					60	nC
2N7432					53	nC
2N7433					42	nC
Gate to drain charge			Q_{gd}			
2N7431					110	nC
2N7432					110	nC
2N7433					120	nC
Reverse recovery time	3473	di/dt $\leq$ 100 A/µs, $V_{DD} \leq$ 50 V, condition A. $I_D = I_{D1}$	t_{rr}			
2N7431					360	ns
2N7432					520	ns
2N7433					820	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

	Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits				Post-irradiation limits				Unit
		Method	Conditions		R		F, G, and H 4/		R		F, G, and H 4/		
					Min	Max	Min	Max	Min	Max	Min	Max	
	Subgroup 1 Not applicable												
	Subgroup 2		T_C = +25°C										
*	Steady-state total dose irradiation (V_{GS} bias) 5/	1019	Condition A, V_{GS} = 12 V, V_{DS} = 0										
*	Steady-state total dose irradiation (V_{DS} bias) 5/	1019	Condition A, V_{DS} = 80 percent of rated V_{DS} (pre-irradiation) V_{GS} = 0										
	Pre and post electricals:												
*	Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0, I_D = 1 mA	$V_{(BR)DSS}$									
	2N7431				60		60		60		60		V dc
	2N7432				100		100		100		100		V dc
	2N7433				200		200		200		200		V dc
	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$									
	2N7431				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
	2N7432				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
	2N7433				2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
	Gate current	3411	Bias condition C, V_{GS} = 20 V, V_{DS} = 0	I_{GSSF1}		100		100		100		100	nA dc
	Gate current	3411	Bias condition C, V_{GS} = -20 V, V_{DS} = 0	I_{GSSR1}		-100		-100		-100		-100	nA dc
	Drain current	3413	Bias condition C, V_{GS} = 0, V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		25		25		25		50	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

	Inspection 1/ 2/ 3/	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Pre-irradiation limits R Min	Pre-irradiation limits R Max	Pre-irradiation limits F, G, and H 4/ Min	Pre-irradiation limits F, G, and H 4/ Max	Post-irradiation limits R Min	Post-irradiation limits R Max	Post-irradiation limits F, G, and H 4/ Min	Post-irradiation limits F, G, and H 4/ Max	Unit
	Static drain to source on-state voltage	3405	V_{GS} = 12 V, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$V_{DS(on)1}$									
	2N7431					.735		.735		.735		1.050	V dc
	2N7432					1.575		1.575		1.575		2.170	V dc
	2N7433					1.750		1.750		1.750		2.750	V dc
*	Forward voltage source to drain diode	4011	Condition A V_{GS} = 0, $I_D = I_{D1}$	V_{SD}									
	2N7431					1.5		1.5		1.5		1.5	V dc
	2N7432					1.8		1.8		1.8		1.8	V dc
	2N7433					1.8		1.8		1.8		1.8	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The H designation represents devices which pass end-points at all R, F, G, and H designated total-ionizing-dose (TID) levels.
5/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
Subgroup 11			
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

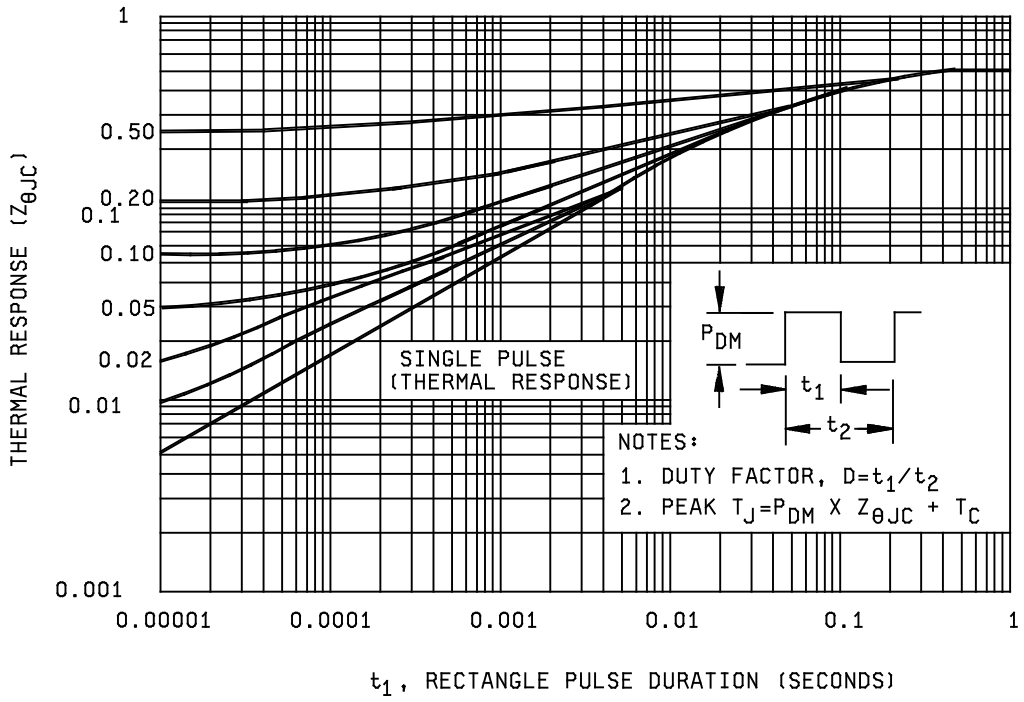


FIGURE 2. Thermal impedance curves.

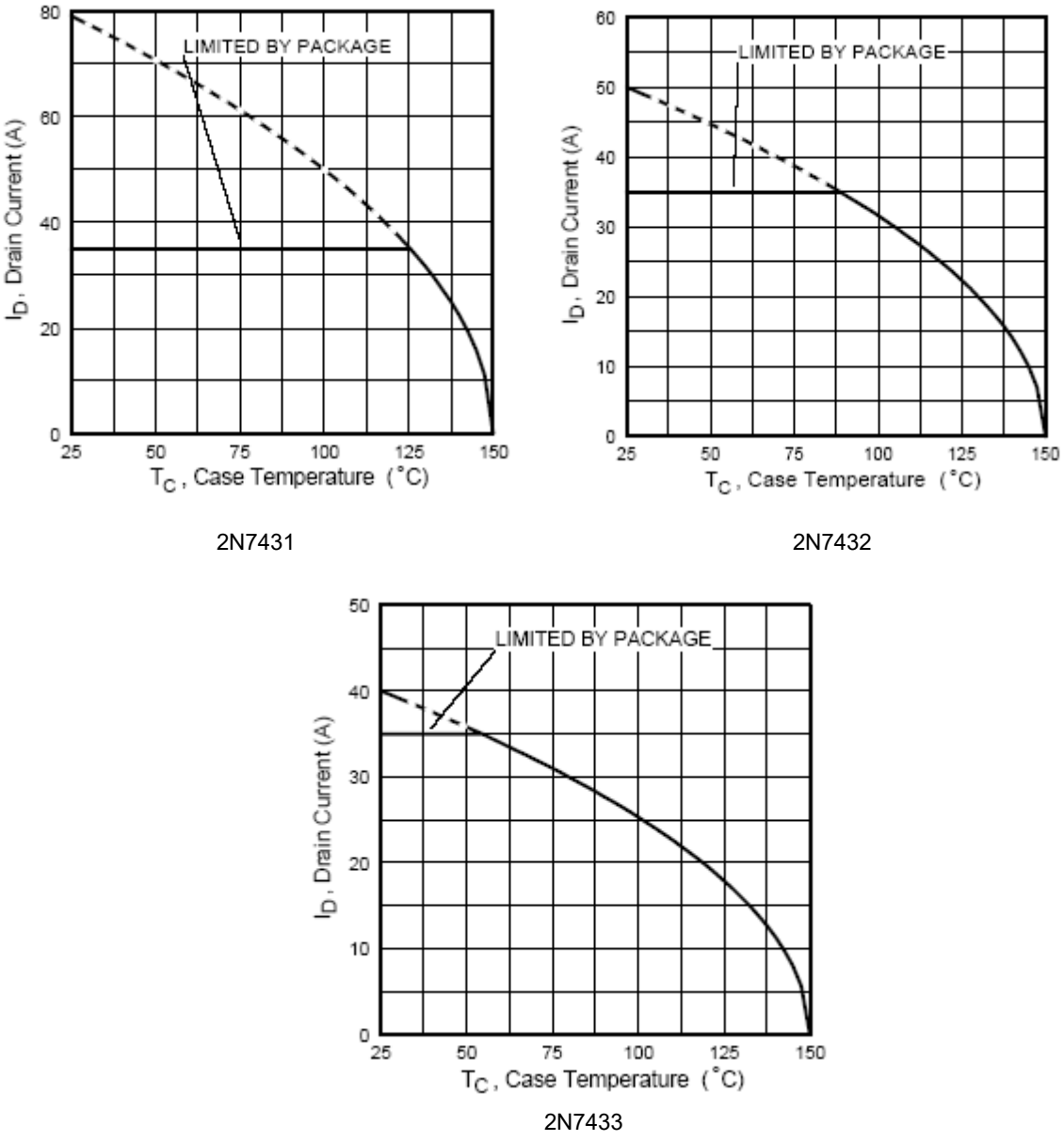


FIGURE 3. Maximum drain current versus case temperature graph (all devices).

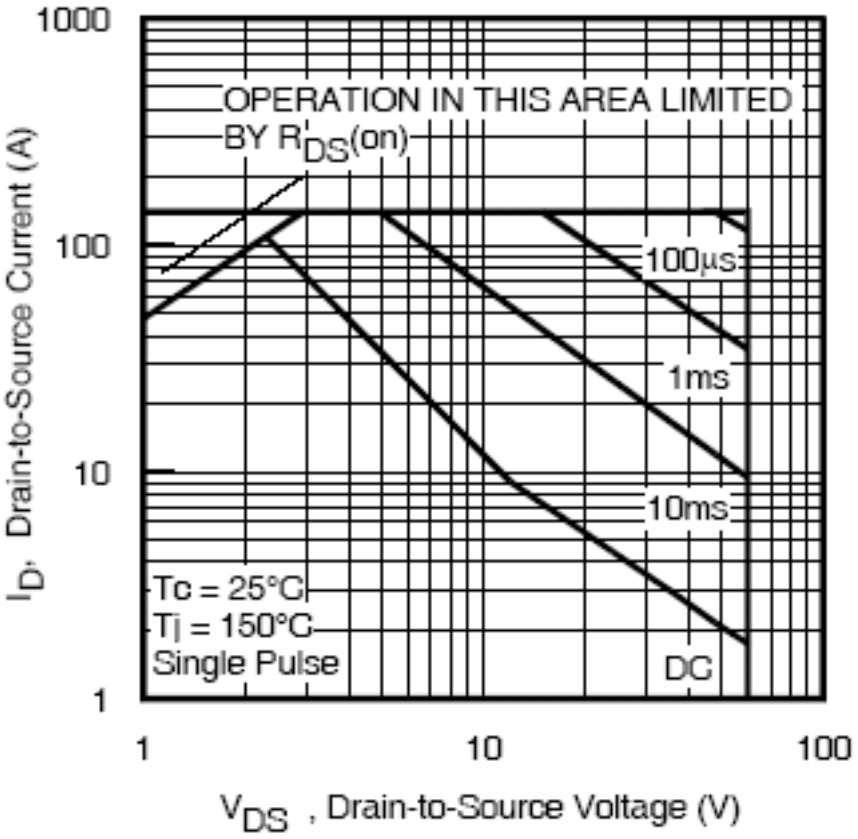


FIGURE 4. Safe operating area graph.

2N7432

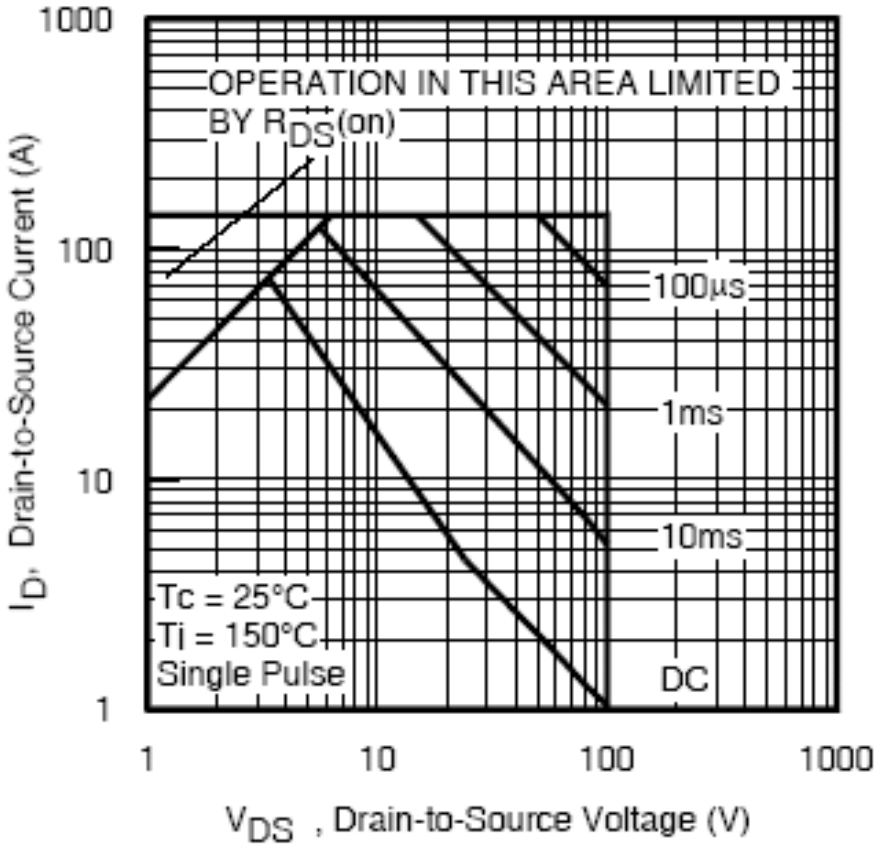


FIGURE 5. Safe operating area graph.

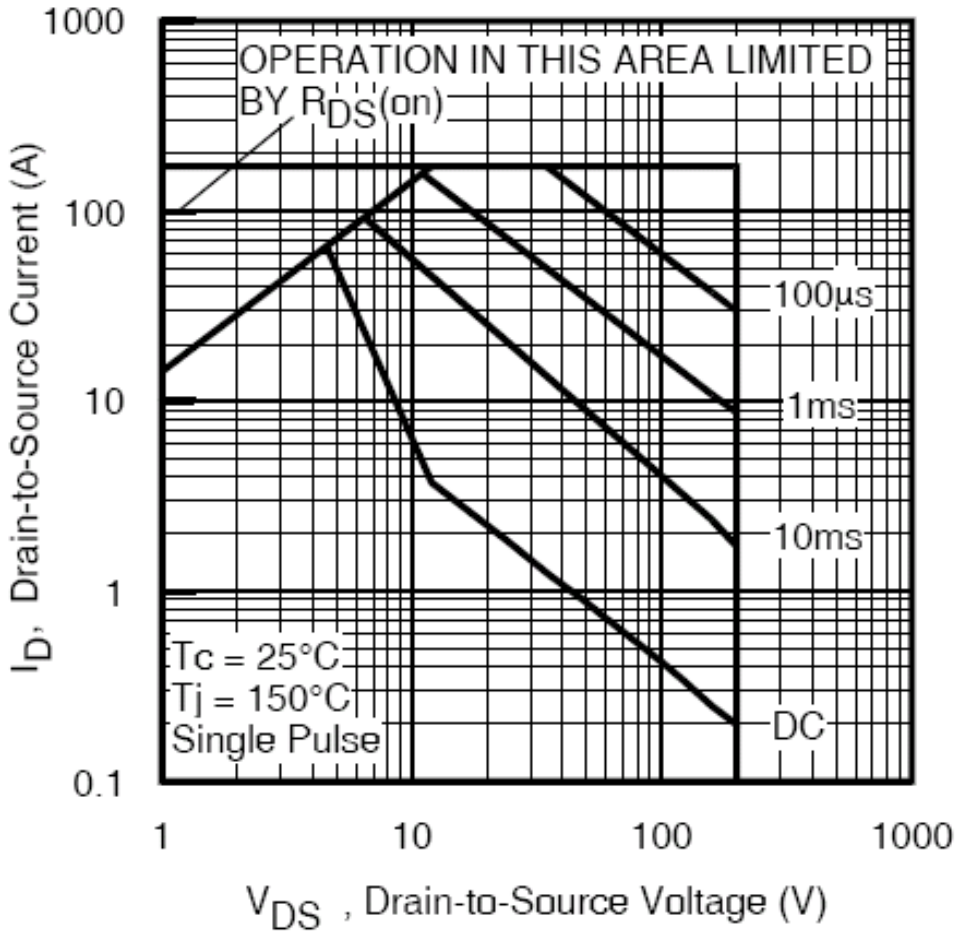


FIGURE 6. Safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

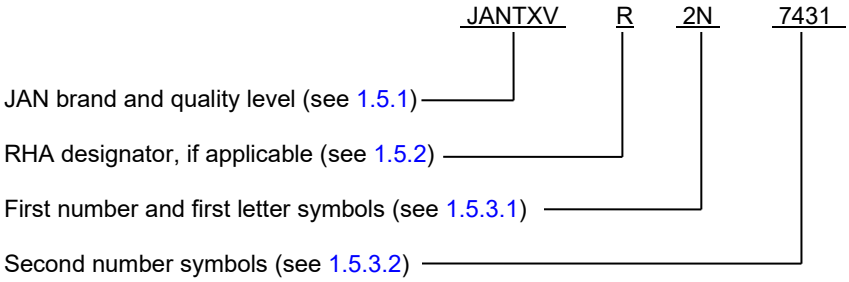
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

f. If specific SEE characterization conditions are desired (see section 6.9 and table IV), manufacturer's cage code should be specified in the contract or order.

g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7431	JANTXV#2N7431	JANS2N7431	JANS#2N7431
JANTXV2N7432	JANTXV#2N7432	JANS2N7432	JANS#2N7432
JANTXV2N7433	JANTXV#2N7433	JANS2N7433	JANS#2N7433

* (1) The number sign (#) represent the RHA designators available "R", "F", "G" and "H".

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types Military PIN	Commercial PIN (1)
	TO254AA
2N7431 2N7432 2N7433	IRHM_064 IRHM_160 IRHM_260

(1) IRHM7: 100k Rad (Si)
IRHM3: 300k Rad (Si)
IRHM4: 600k Rad (Si)
IRHM8: 1,000k Rad (Si)

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/657.

6.8 Surface mount versions. The surface mount version (suffixes U, U2L, and U2S) of these devices are covered under specification sheet MIL-PRF-19500/664.

6.9 Application data.

6.9.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
No manufacturers are currently qualified to the SEE requirements	SEE 1/ Electrical measurements Electrical measurements	1080	See MIL-STD-750E method 1080 I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2 I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

6.10 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-6939 or DSN 850-6939.

* 6.11 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project - 5961-2022-053)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.