

The documentation and process conversion measures necessary to comply with this revision shall be completed by 16 November 2020.

INCH-POUND

MIL-PRF-19500/656C
17 August 2020
SUPERSEDING
MIL-PRF-19500/656B
8 June 2015

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, POWER RECTIFIER,
DEVICE TYPES 1N6785 AND 1N6785R,
COMMON CATHODE OR COMMON ANODE CENTER TAP,
QUALITY LEVELS JAN, JANTX, JANTXV AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a silicon, Schottky, power rectifier diode. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The package outline is a three terminal flange mount header TO-257AA in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Types	V_R (1)	V_{RWM} (1)	I_O (1) (2) (3) $T_J = T_C = +100^\circ\text{C}$	I_{FSM} (1) $T_C = +25^\circ\text{C}$ $t_p = 8.3\text{ ms}$	C_J (1) at 5 V	$R_{\theta JC}$ (1)	$R_{\theta JA}$ (1)	T_{STG} and T_J
	<u>V</u>	<u>V</u>	<u>A dc</u>	<u>A(pk)</u>	<u>pF</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C</u>
1N6785, 1N6785R	45	45	15	150	2,000	1.65	40	-65 to +150

- (1) Each individual diode.
- (2) Derate linearly at $300\text{ mA}/^\circ\text{C}$ from $T_J = T_C = +100^\circ\text{C}$ to $+150^\circ\text{C}$; $300\text{ mA}/^\circ\text{C}$ times $50^\circ\text{C} = 15\text{ A}$, the device rating.
- (3) Total package current is limited to 30 A dc.

1.4 Primary electrical characteristics. $R_{\theta JC} = 1.65^\circ\text{C}/\text{W}$ maximum for all device types.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows: "6785".

1.5.3 Suffix symbols. The suffix letter "R" is used on devices that are reverse polarity of the no suffix devices (see [figure 1](#)).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections [3](#) and [4](#) of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections [3](#) and [4](#) of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

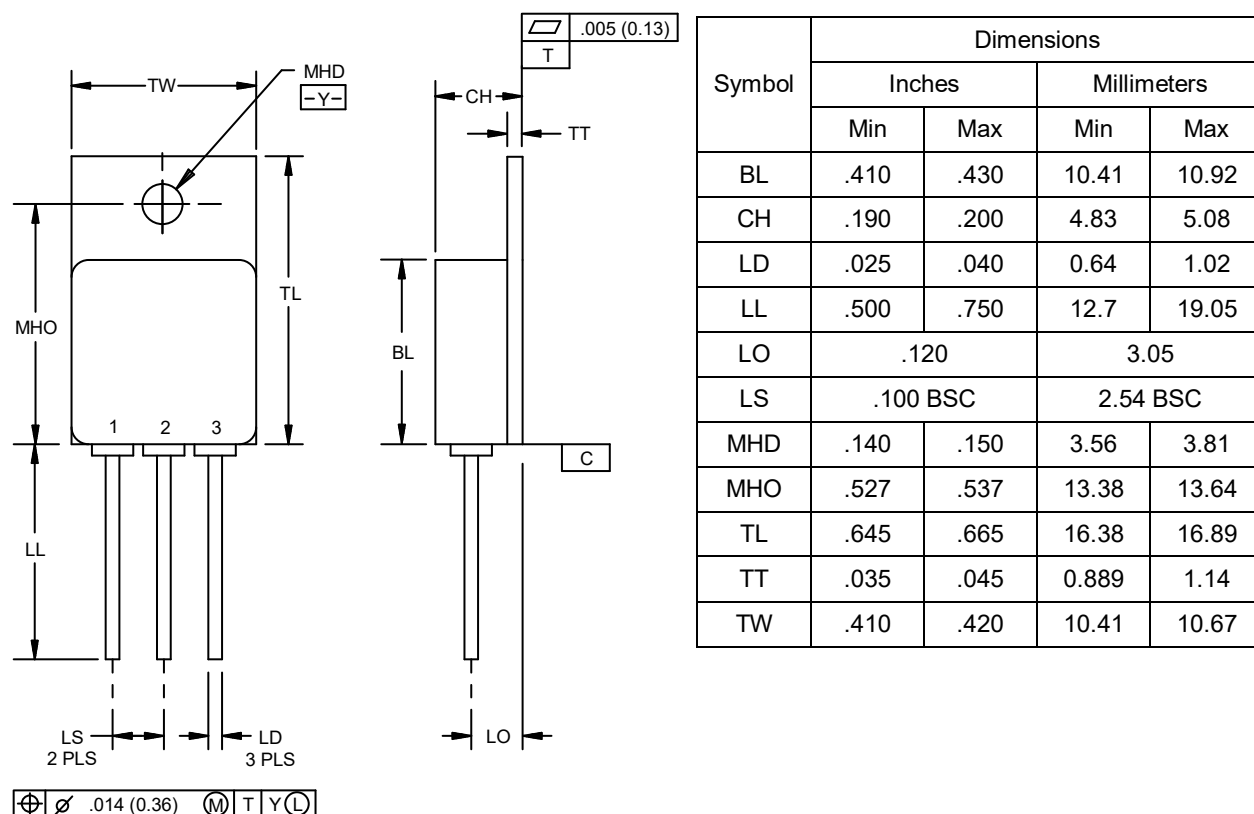
[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

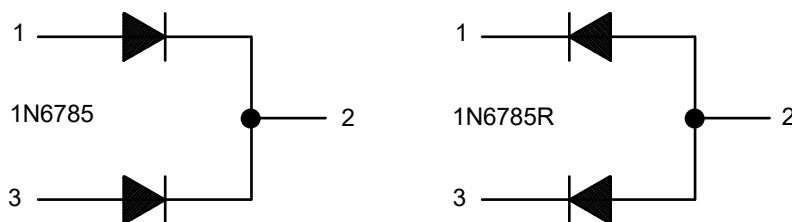
[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



SCHEMATIC



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Protrusion of ceramic eyelets included in dimension LL.
3. All terminals are isolated from case.
4. In accordance with ASME Y14.5M, diameters are equivalent to $\varnothing$ x symbology.

FIGURE 1. Physical dimensions and configuration of three terminal flange mount header package (TO-257AA).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#) (TO-257AA) herein.

3.4.1 Lead finish and formation. Lead finish shall be solderable as defined in [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish or formation is desired, it shall be specified in the acquisition requirements (see [6.2](#)).

3.4.2 Lead formation. Where a choice of lead formation is desired, it shall be specified in the acquisition document (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of [MIL-PRF-19500](#) and 100 percent dc testing in accordance with subgroup 2 of [table I](#) herein on all devices that had its leads altered.

3.4.3 Lead isolation. The methods used for electrical isolation of the terminal feed through shall employ materials that contain a minimum of 90 percent ceramic Al_2O_3 or equivalent. Examples of such construction techniques are metalized ceramic eyelets or ceramic walled packages.

3.4.4 Polarity. Polarity and terminal configuration shall be in accordance with [figure 1](#) herein.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#) and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be group A as specified herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#), and [tables I, II, and III](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#).

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed by the first inspection lot of this revision to maintain qualification.

4.2.2 Thermal impedance for initial qualification or requalification. The thermal impedance measurements shall be performed in accordance with method 3101 of [MIL-STD-750](#). Read and record date thermal impedance derived conditions limits and thermal response curve shall be supplied to the qualifying activity on the qualification lot prior to qualification approval.

4.3 Screening (quality levels JANS, JANTX, and JANTXV only). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2) Peak reverse energy test (see 4.3.3)	Thermal impedance (see 4.3.2) Peak reverse energy test (see 4.3.3)
9 and 10	Not applicable	Not applicable
11	V_{F2} and I_{R1}	V_{F2} and I_{R1}
12	See 4.3.1 , $t = 240$ hours	See 4.3.1 , $t = 48$ hours
13	Subgroups 2 and 3 of table herein; $\Delta V_{F2} = \pm 50$ mV; $\Delta I_{R1} = 100$ percent of initial value or ± 250 μ A dc, whichever is greater.	Subgroup 2 of table herein; $\Delta V_{F2} = \pm 50$ mV; $\Delta I_{R1} = 100$ percent of initial value or ± 250 μ A dc, whichever is greater.

(1) Shall be performed anytime after temperature cycling, screen 3a. JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in shall be performed in accordance with test condition A of method 1038 of [MIL-STD-750](#). The following details shall apply: $T_C = +125$ °C; $V_R = 36$ V dc.

4.3.2 Thermal impedance measurements for screening. The thermal impedance measurements shall be performed in accordance with method 3101 of [MIL-STD-750](#). Each die shall be tested separately. The maximum limit and conditions for thermal impedance in screening (table E-IV of [MIL-PRF-19500](#)) shall be derived by each vendor by means of process control of actual measurements which characterizes the die attach process. When three lot date codes have exhibited control, the data from these three lots will be used to establish a fixed screening limit (not to exceed the group A limit). Once a fixed limit has been established, all future sealing lots shall be monitored using a sample from each lot to be plotted on the applicable statistical process chart.

4.3.3 Peak reverse energy test. The peak reverse energy test shall be performed using the circuit as shown on [figure 2](#) or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: $I_{RM} = 2$ A minimum, $V_{RSM} = 45$ V dc minimum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#), and [table I](#) herein. Delta measurements shall be in accordance with the applicable steps of [table III](#) herein.

4.4.1.1 Thermal impedance measurements for group A. The following test conditions shall be used for thermal impedance measurements for group A inspection:

- a. I_M measure current..... 10 mA.
- b. I_H forward heating current..... 15 to 50 A.
- c. t_H heating time..... 50 ms.
- d. t_{MD} measurement delay time..... 100 μ s minimum.

The maximum limit for thermal impedance under these test conditions are $Z_{\theta JX(max)} = 1.55\text{ }^{\circ}\text{C/W}$.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and E-VIB (JAN, JANTX and JANTXV) of [MIL-PRF-19500](#), and as follows. Delta measurements shall be in accordance with the applicable steps of [table III](#) herein.

4.4.2.1 Quality level JANS (table E-VIA of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B4	1037	I_F or $I_O = 2\text{ A}$ minimum; $\Delta T_J \geq 85\text{ }^{\circ}\text{C}$.
B5	1038	Condition A, $T_J = T_C = +150\text{ }^{\circ}\text{C}$, $V_R = 36\text{ V dc}$.
B6	3101	$R_{\theta JC} = 1.65\text{ }^{\circ}\text{C/W}$ maximum for each die.

4.4.2.2 Quality levels JAN, JANTX and JANTXV (table E-VIB of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1037	I_F or $I_O = 2\text{ A}$ minimum; $\Delta T_J \geq 85\text{ }^{\circ}\text{C}$.
B5	3101	$R_{\theta JC} = 1.65\text{ }^{\circ}\text{C/W}$ maximum for each die.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows. Delta measurements shall be in accordance with the applicable steps of [table III](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A, weight = 10 pounds (4.54 kg), $t = 15\text{ seconds}$.
C6	1037	I_F or $I_O = 2\text{ A}$ (minimum); $\Delta T_J \geq 85\text{ }^{\circ}\text{C}$.

4.4.4. Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Thermal resistance. Thermal resistance shall be measured in accordance with method 3101 or 4081 of [MIL-STD-750](#). Each diode leg shall be measured. The following details shall apply:

- a. I_H 15 to 50 A.
- b. I_M 10 mA.
- c. $R_{\theta JC}$ 1.65 °C/W.
- d. t_{MD} 100 μ s maximum.

4.5.3 Dielectric withstanding voltage (DWV). The test for DWV shall be performed in accordance with test method 1016 of [MIL-STD-750](#). The following details shall apply: V_R = 500 V dc; all leads shorted; Measure from leads to case; The sample shall be $n = 116$, $c = 0$.

TABLE I. Group A inspection.

Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance	3101	See 4.4.1.1	$Z_{\theta JX}$		1.55	°C/W
Forward voltage	4011	Condition B, pulsed (see 4.5.1) $I_F = 5$ A (pk) $I_F = 15$ A (pk) $I_F = 30$ A (pk)	V_{F1} V_{F2} V_{F3}	0.55 0.75 1.0		V dc V dc V dc
Reverse current	4016	Condition A or B, pulsed (see 4.5.1), $V_R = 45$ V dc	I_{R1}		1.0	mA dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +125^\circ\text{C}$				
Reverse current leakage	4016	Condition A or B, pulsed (see 4.5.1), $V_R = 45$ V	I_{R2}		40	mA dc
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward voltage	4011	Condition B, pulsed (see 4.5.1), $I_F = 15$ A (pk)	V_{F4}		0.8	V dc
<u>Subgroup 4</u>						
Junction capacitance	4001	$V_R = 5$ V dc; $f = 1$ MHz, $V_{SIG} = 50$ mV (p-p) (max)	C_J		2,000	pF
<u>Subgroup 5</u>						
Dielectric withstanding Voltage	1016	See 4.5.3	I_{RES}		10	μA
<u>Subgroup 6 and 7</u>						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.2/ Each individual diode.

TABLE II. Group E inspection (all quality levels) for qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			
Thermal shock (temperature cycling)	1051	500 cycles	45 devices, c = 0
Hermetic seal	1071	Fine and gross leak	
Electrical measurements		See table III , steps 1, 2, and 5	
<u>Subgroup 2</u>			45 devices, c = 0
Steady-state blocking life	1048	t = 1,000 hours, T _C = +125 °C; V _R = 36	
Electrical measurements		See table III , steps 1 and 2	
<u>Subgroup 3</u>			N/A
Not applicable			
<u>Subgroup 4</u>			
Thermal impedance curves	3101	See MIL-PRF-19500	22 devices, c = 0
<u>Subgroup 10 1/</u>			
Surge current	4066	Condition B; T _A = +25 °C; I _{FSM} = 150 A, 100 surges	
Electrical measurements		See table III , steps 1 and 2	

1/ For each individual diode.

TABLE III. Delta end-point measurements for groups A, B, and C. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Forward voltage	4011	Condition B, pulsed (see 4.5.1) $I_F = 15 \text{ A (pk)}$,	ΔV_{F2}	$\pm 50 \text{ mV dc}$ from initial reading.		
2.	Reverse current	4016	Condition A or B, pulsed (see 4.5.1) $V_R = 45 \text{ V dc}$, pulsed (see 4.5.1)	ΔI_{R1}			
3.	Thermal impedance	3101	See 4.3.2	$Z_{\theta JX}$		1.55	$^{\circ}\text{C/W}$

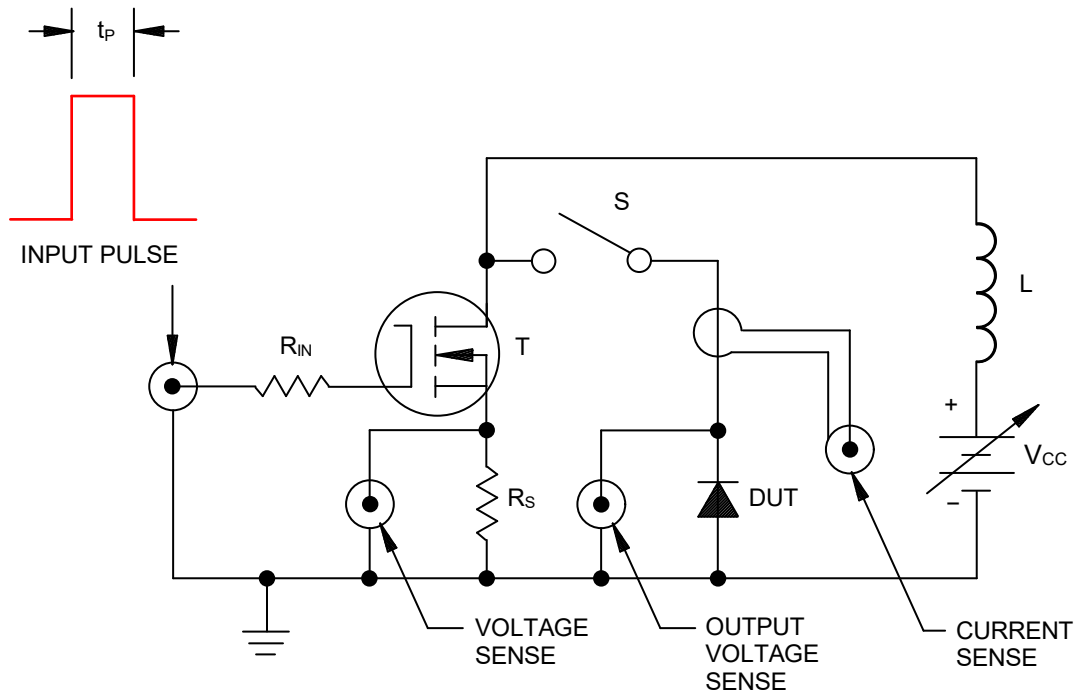
1/ Each individual diode.

2/ The delta end-point measurements taken during group B inspection for quality level JANS (table E-VIA of MIL-PRF-19500) shall be as follows:

- a. In addition to the measurements specified for subgroup 4, the measurements of steps 1, 2, and 3 of this table shall also be taken.
- b. In addition to the measurements specified for subgroup 5, the measurements of step 3 of this table shall also be taken.

3/ The delta end-point measurements taken during group B inspection for quality levels JAN, JANTX, and JANTXV (table E-VIB of MIL-PRF-19500) for subgroup 3 shall include the measurements of step 3 of this table.

4/ The delta end-point measurements taken during group C inspection for all quality levels (table E-VII of MIL-PRF-19500) for subgroup 6 shall include the measurements of step 3 of this table.



PROCEDURE:

1. With S open, adjust pulse width to test current of 2 amps across R_S .
2. Close S , verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

NOTES:

1. The following input pulse details shall apply: $V_G = 10$ Volts, P.W. $\approx 30 \mu s$, duty cycle ≤ 1 percent.
2. The following test circuit component values shall apply: $L = 260 \mu H$, $R_G = 50$ ohms, $R_{in} = 50$ ohms, 1 watt, $R_S = 0.1$ ohms, 1 watt, $T = 2N6756$ (IRF130 or equivalent).
3. The supply voltage $V_{CC} \approx 10$ volts.

FIGURE 2. Peak reverse energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

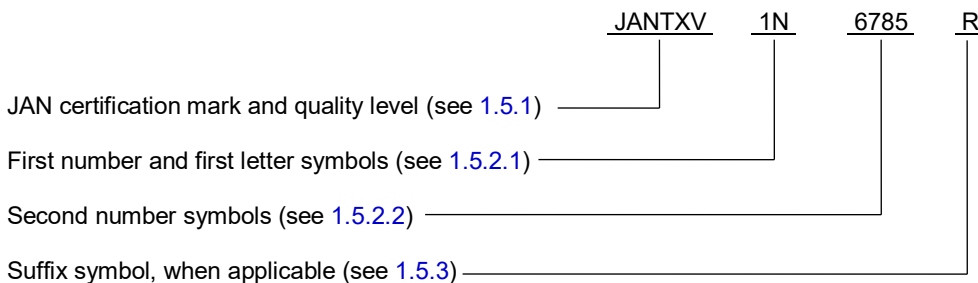
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1) and if applicable, any needed lead formation (see 3.4.2).
- d. The complete PIN, see 1.5 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

Base quality level	Quality level "TX"	Quality level "TXV"	Quality level "S"
PINs for standard polarity			
JAN1N6785	JANTX1N6785	JANTXV1N6785	JANS1N6785
PINs for reverse polarity			
JAN1N6785R	JANTX1N6785R	JANTXV1N6785R	JANS1N6785R

6.6 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:
 Army – CR
 Navy – EC
 Air Force – 85
 NASA – NA
 DLA – CC

Preparing activity:
 DLA – CC
 (Project 5961–2020–046)

Review activity:
 Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.