

The documentation and process conversion measures necessary to comply with this document shall be completed by 21 October 2020.

INCH-POUND

MIL-PRF-19500/652D
21 July 2020
SUPERSEDING
MIL-PRF-19500/652C
6 December 2013

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, HIGH VOLTAGE,
FIELD EFFECT, N-CHANNEL, SILICON, TYPE 2N7387 AND 2N7387U1,
JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a high voltage N-channel, enhancement-mode, power MOSFET transistor, with avalanche energy maximum ratings (E_{AS}) and maximum avalanche current (I_{AS}). Four levels of product assurance are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Physical dimensions. See [figure 1](#) (TO-254AA), and [figure 2](#) for surface mount (U1).

1.3 Maximum ratings. ($T_A = +25^\circ\text{C}$, unless otherwise specified).

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$	$V_{(BR)DSS}$ min $V_{GS} = 0\text{ V dc}$ $I_D = 1.0\text{ mA dc}$	I_{D1} (2) $T_C = +25^\circ\text{C}$	I_{D2} (2) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (3)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>$^\circ\text{C}$</u>
2N7387, 2N7387U1	125	4	1.0	1,000	3	1.9	3	9	-55 to +150

See notes on next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

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1.3 Maximum ratings. - Continued.

Type	I_{AR} (2)	V_{GS}	E_{AS}	$r_{DS(on)max}$ (4) $V_{GS} = 10V$ dc; $I_D = 1.9A$	
				$T_J = +25^\circ C$	$T_J = +150^\circ C$
2N7387, 2N7387U1	$\underline{A}$ 3	$\underline{V}$ dc ± 20	$\underline{mJ}$ 245	$\underline{ohms}$ 4.00	$\underline{ohms}$ 9.60

(1) Derate linearly 1.0 W/ $^\circ C$ for $T_C > +25^\circ C$ (2) $ID = \sqrt{[T_{J(max)} - T_C]/[R_{\theta JX} \times (R_{ds(on)} \text{ at } T_{J(max)})]}$ (3) $IDM = 3 \times I_{D1}$ as calculated in footnote (2).

(4) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. $T_C = +25^\circ C$ (unless otherwise specified).

Type	$V_{(BR)DSS}$ min $V_{GS} = 0$ V dc $I_D = 1.0$ mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ $I_D = 0.25$ mA dc	I_{DSS1} max $V_{GS} = 0$ V dc $V_{DS} = 800$ V dc	$r_{DS(on)}$ (1) $V_{GS} = 10$ V dc $I_D = 1.9$ A dc
2N7387, 2N7387U1	$\underline{V}$ dc 1,000	$\underline{V}$ dc $\underline{min} \quad \underline{max}$ 2.0 4.0	$\underline{\mu A}$ dc 25	$\underline{ohms}$ 4.00

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7387".

* 1.5.2.3 Suffix symbols. Devices with no suffix have standard length leads of 0.5 inch (12.7 mm) minimum to .75 inch (19.1 mm) maximum in figure 1. The suffix letter "U" is used on devices that are packaged in the surface mount package of figure 2.

	A blank second suffix letter indicates a through-hole mount package similar to a TO-254AA metal can (see figure 1).
U1	Indicates a 4 pad surface mount package. The metal lid is connected to pad 4 (see figure 2).

* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

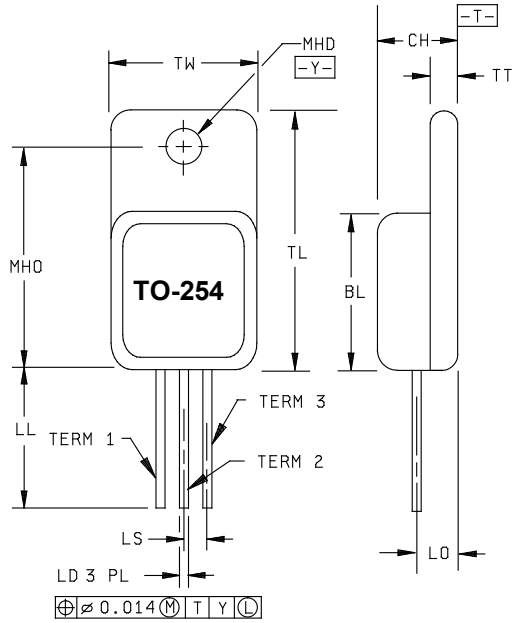
[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



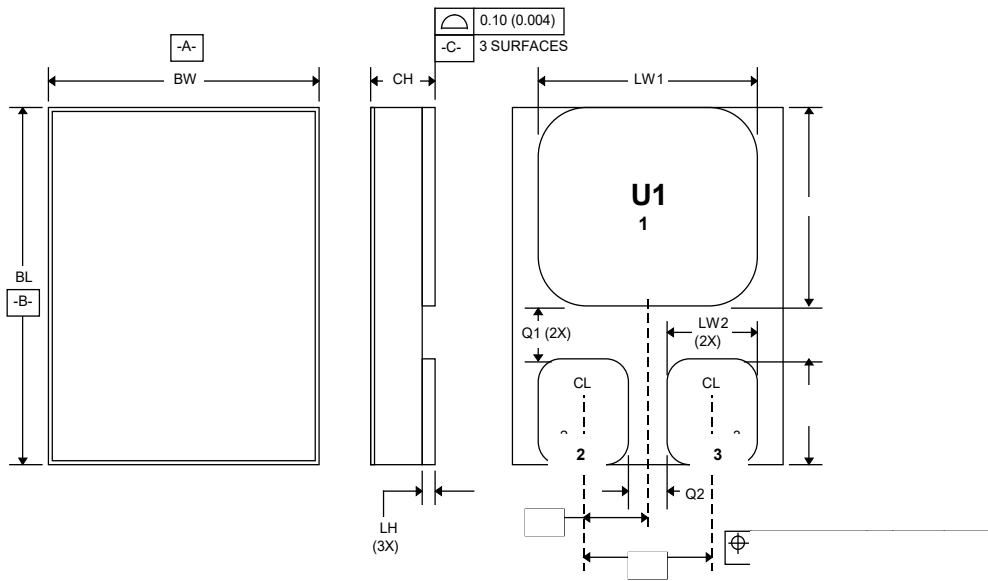
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3, 4
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to $\varnothing$ x symbology.

FIGURE 1. Physical dimensions for (TO-254AA)

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.74	16.00
BW	.445	.455	11.30	11.55
CH	.129	.139	3.27	3.53
LH	.010	.020	0.25	0.51
LW1	.370	.380	9.39	9.65
LW2	.135	.145	3.43	3.68
LL1	.410	.420	10.41	10.66
LL2	.152	.162	3.86	4.11
LS1	.200	.220	5.08	5.59
LS2	.100	.110	2.54	2.79
Q1	.035		0.89	
Q2	.050		1.27	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 2. Physical dimensions for 2N7387U1 (surface mount).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list ([QML-19500](#)) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on figures 1 and 2 herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead material, finish, and formation. Lead material shall be Kovar or Alloy 52; a copper core or plated core is permitted. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead formation, material or finish is desired, it shall be specified in the acquisition document (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of [table II](#) of [MIL-PRF-19500](#) and 100 percent dc testing in accordance with [table I](#), subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended.

- a. Devices should be handled on benches with conductive and grounded surfaces.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source. $R \leq 100\text{K}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and [table I](#) and [table II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein. Alternate flow is allowed for qualification inspection in accordance with figure 4 of [MIL-PRF-19500](#).

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX, JANTXV, and JANS levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2)	Method 3470 of MIL-STD-750, (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-7500, (see 4.3.3)	Method 3161 of MIL-STD-750, (see 4.3.3)
9	Subgroup 2 of table I herein, I_{DSS1} , I_{GSSF1} , I_{GSSR1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$. Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$. Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, condition A	Method 1042 of MIL-STD-750, condition A
13	Subgroups 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.
17	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse unclamped inductive switching.

- a. Peak current, I_{AS} 3 A.
- b. Peak gate voltage, V_{GS} 10 V.
- c. Gate to source resistor, R_{GS} $25 \leq R_g \leq 200$ ohms.
- d. Initial case temperature $+25^{\circ}\text{C}$, $+10^{\circ}\text{C}$, -5°C .
- e. Inductance, L 51.72 mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 50 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). (See [figure 3](#) herein.) Measurement delay time (t_{MD}) = 70 μ s max. See [table II](#), group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage.....900 V dc.
- b. Duration of application of test voltage.....15 seconds (min).
- c. Points of application of test voltage.....All leads to case (bunch connection).
- d. Method of connection.....Mechanical.
- e. Kilovolt-ampere rating of high voltage source.....1,200 V/1.0 mA (min).
- f. Maximum leakage current.....1.0 mA.
- g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#), and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

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4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B4	1042	Test condition D. No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.
B5	1042	A separate sample may be pulled for each test. Condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours min. or T_A = +150°C, t = 48 hours min. Condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours min. or T_A = +150°C, t = 240 hours min.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B2	1051	Test condition G.
B3	1042	Test condition D. No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A; weight = 10 pounds, t = 15 s. Not applicable to surface mount version.
C5	3161	See 4.3.3 , $R_{\theta JC}$ = 0.60 °C/W.
C6	1042	Test condition D. No heat sink or forced air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

Inspections <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	Bias condition C, $V_{GS} = 0$ V dc, $I_D = 1.0$ mA dc	$V_{(BR)DSS}$	1000		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 0.25$ mA dc	$V_{GS(th)1}$	2.0	4.0	V dc
Gate reverse current	3411	Bias condition C, $V_{DS} = 0$ V dc, $V_{GS} = +20$ V dc	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	Bias condition C, $V_{DS} = 0$ V dc, $V_{GS} = -20$ V dc	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, $V_{DS} = 800$ V dc	I_{DSS1}		25	μA dc
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1); $V_{GS} = 10$ V dc, $I_D = 1.9$ A dc	$r_{DS(on)1}$		4.0	ohm
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1); $V_{GS} = 10$ V dc, $I_D = 3$ A dc	$r_{DS(on)2}$		4.2	ohm
Forward voltage (source drain diode)	4011	Pulsed (see 4.5.1), $V_{GS} = 10$ V dc, $I_D = 3$ A dc	V_{SD}		1.8	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate reverse current	3411	Bias condition C, $V_{GS} = +20$ V dc and -20 V dc, $V_{DS} = 0$ V dc	I_{GSS2}		±200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, $V_{DS} = 1,000$ V dc	I_{DSS2}		1.0	mA dc
		$V_{DS} = 800$ V dc	I_{DSS3}		0.5	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 0.25$ mA dc	$V_{GS(th)2}$	1.0		V dc
Static drain to source on-state resistance	3421	Condition A, pulsed (see 4.5.1); $V_{GS} = 10$ V dc, $I_D = 1.9$ A dc	$r_{DS(on)3}$		8.0	ohm

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspections ^{1/}	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 0.25 \text{ mA dc}$	$V_{GS(th)3}$		5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$V_{GS} = 10 \text{ V dc pulsed}$, $V_{DD} = 400 \text{ V dc}$, $R_G = 9.1 \text{ ohms}$, $I_D = 3.0 \text{ A dc}$				
Turn-on delay time			$t_{d(on)}$		25	ns
Rise time			t_r		45	ns
Turn-off delay time			$t_{d(off)}$		150	ns
Fall time			t_f		65	ns
<u>Subgroup 5</u>						
Safe operating area test	3474	See figure 4 , $V_{DS} = 200 \text{ V dc}$, $t_p = 10 \text{ ms}$ See table 1, subgroup 2 herein.				
Electrical measurements						
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$		120	nC
Gate to source charge			Q_{gs}		16	nC
Gate to drain charge			Q_{gd}		75	nC
Reverse recovery time	3473	$V_{DD} \leq 30 \text{ V}$, $d_i/d_t \leq 100 \text{ A}/\mu\text{s}$, $I_D = 3 \text{ A dc}$	t_{rr}		1100	ns

^{1/} For sampling plan, see [MIL-PRF-19500](#).^{2/} This test required for the following end-point measurements only:

Group B, subgroups 2 and 3 (JANTXV).

Group B, subgroups 3 and 4 (JANS).

Group C, subgroup 2 and 6.

Group E, subgroup 1.

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TABLE II. Group E inspection (all quality levels) for qualification only.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	500 cycles, test condition G	
Hermetic seal	1071		
Electrical measurements		See table 1, subgroup 2 herein.	
<u>Subgroup 2</u> ^{1/}			45 devices c = 0
Steady state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table 1, subgroup 2 herein.	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table 1, subgroup 2 herein.	
<u>Subgroup 4</u>			
Thermal impedance	3161	See table E-IX of MIL-PRF-19500, group E, subgroup 4.	
<u>Subgroup 5</u>			3 devices c = 0
Barometric pressure (reduced)	1001	Condition C	

^{1/} A separate sample for each test may be pulled.

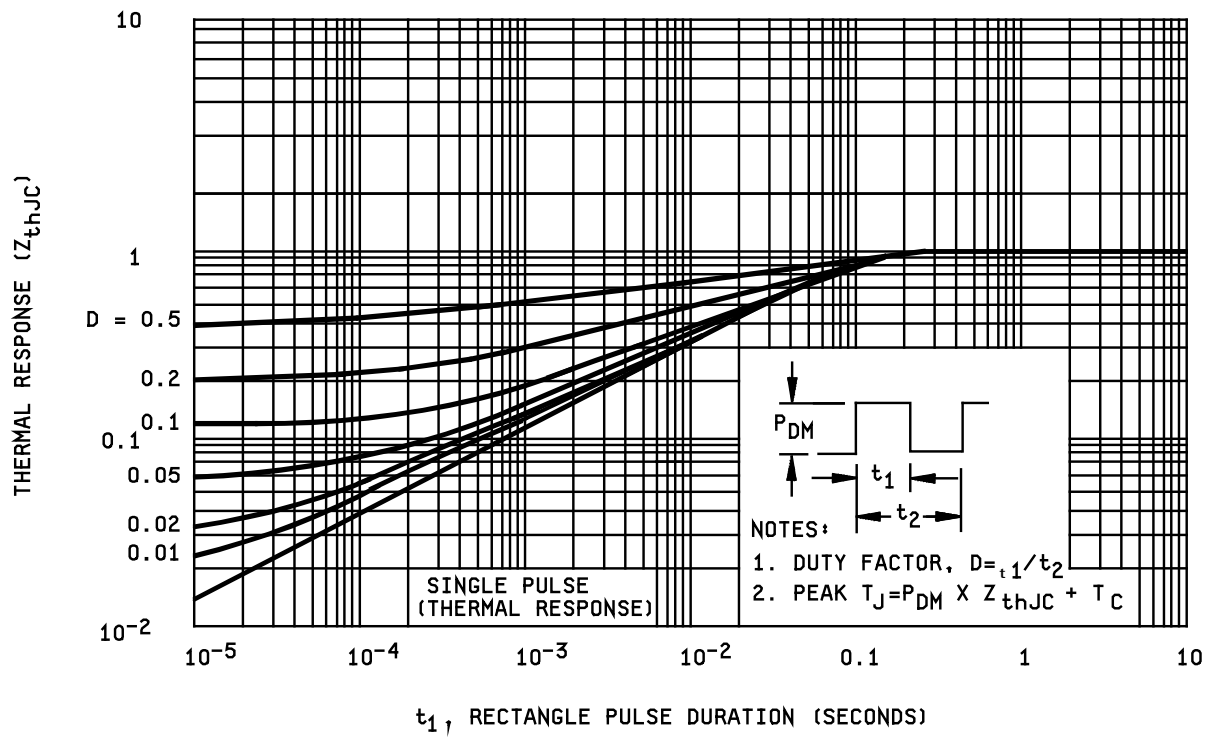


FIGURE 3. Thermal impedance curves.

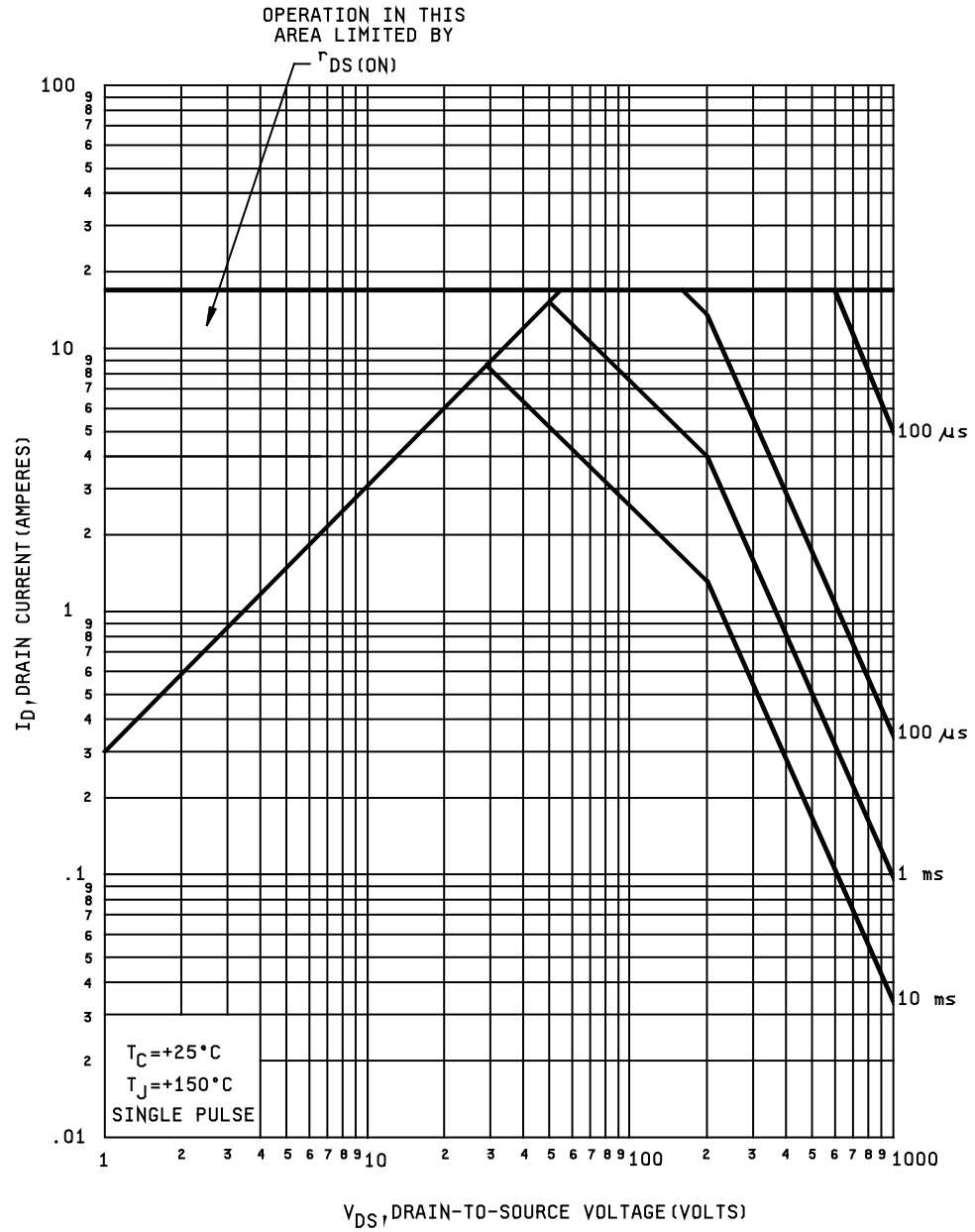


FIGURE 4. Safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

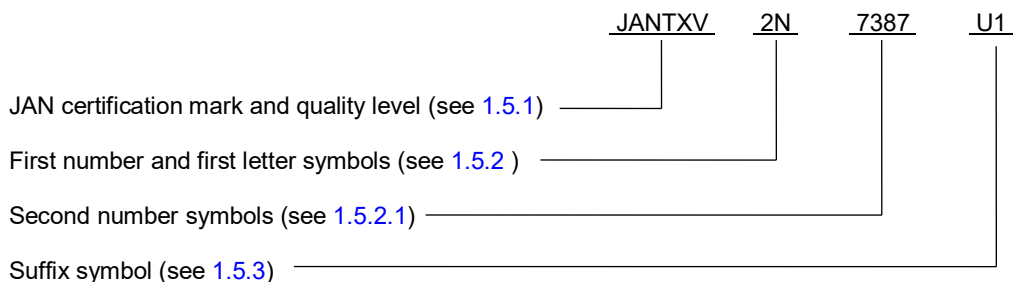
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead material, finish, and formation (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML-19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs.

* 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

Encapsulated PINs for type 2N7387			
JAN2N7387	JANTX2N7387	JANTXV2N7387	JANS2N7387
JAN2N7387U1	JANTX2N7387U1	JANTXV2N7387U1	JANS2N7387U1

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC

(Project 5961-2020-050)

Review activities:
 * Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.