

The documentation and process conversion measures necessary to comply with this revision shall be completed by: 23 December 2024.

INCH-POUND

MIL-PRF-19500/608E
w/AMENDMENT 2
22 July 2024
SUPERSEDING
MIL-PRF-19500/608E
w/AMENDMENT 1
18 November 2022

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, POWER RECTIFIER,
COMMON CATHODE, COMMON ANODE, DOUBLER, TYPE 1N6660, CASE MOUNT PACKAGE,
QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a silicon, Schottky, power rectifier diodes. Four levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The device package is case mount TO-254AA (isolated) in accordance with [figure 1](#) for all device types.

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^{\circ}\text{C}$.

Type	V_R (1)	V_{RWM} (1)	I_O (1) (2) (3) $T_C = 100^{\circ}\text{C}$	I_{FSM} (1) $t_p = 8.3 \text{ ms}$ $T_C = +25^{\circ}\text{C}$	$R_{\theta JC}$ (1) (4) Die 1	$R_{\theta JC}$ (1) (4) Die 2	$R_{\theta JC}$ (entire package) $T_C = 25^{\circ}\text{C}$	$R_{\theta JC}$ (each individual diode) $T_C = 25^{\circ}\text{C}$	T_{STG} & T_J
	V	V	A dc	A(pk)	$^{\circ}\text{C/W}$	$^{\circ}\text{C/W}$	$^{\circ}\text{C/W}$	$^{\circ}\text{C/W}$	$^{\circ}\text{C}$
1N6660	45	45	15	300	1.65	1.65		50	-65 to +150
1N6660CCT1	45	45	15	300	1.65	1.65	0.85	50	
1N6660R	45	45	15	300	2.8	2.8		50	
1N6660CAT1	45	45	15	300	2.8	2.8	1.5	50	
1N6660DT1	45	45	15	300	2.8	1.65	1.5	50	

(1) Each individual diode.

(2) For derating see [figures 2](#) and [3](#).

(3) Total package current is limited to 30 A dc.

(4) For thermal impedance graphs see [figures 4](#) and [5](#).

* 1.4 Primary electrical characteristics. Primary electrical characteristics are not applicable for this specification sheet.

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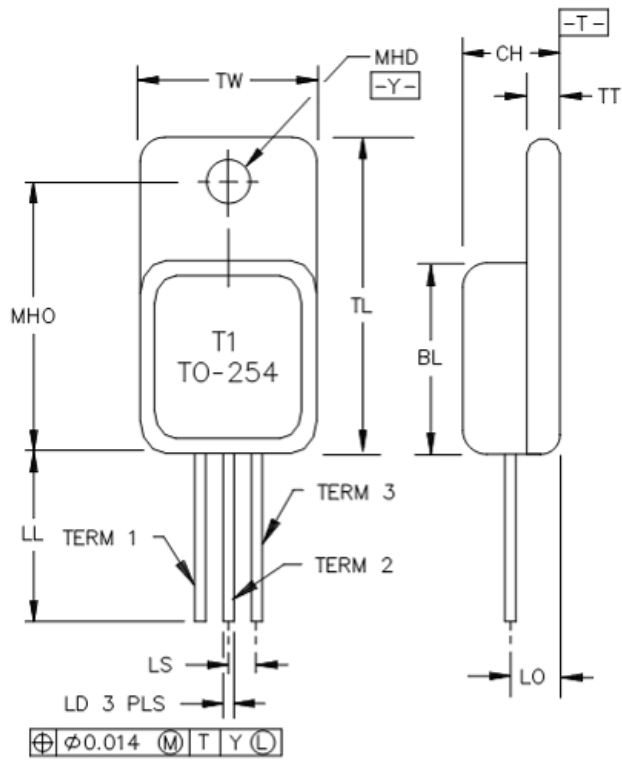
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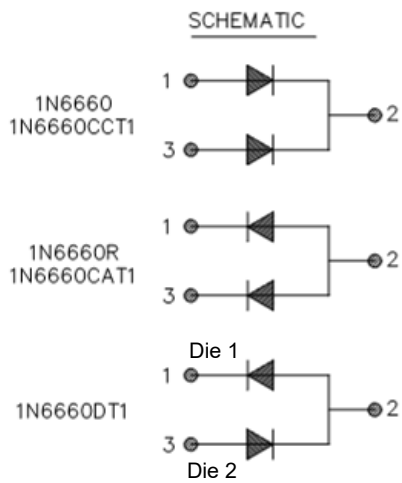


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NOTES:

1. Dimensions are in inches
2. Millimeters are given for general information only.
3. All terminals are isolated from case.



Types 1N6660, 1N6660CCT1, 1N6660R, 1N6660CAT1, and 1N6660DT1

FIGURE 1. Physical dimensions and configuration of TO-254AA package.

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1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example, 6.5 for a list of available PINs, and 6.6 for supersession information.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are "6660".

1.5.3 Suffix symbols. The following suffix symbol(s) are incorporated into the PINs for this specification sheet.

	A blank designator identifies that the device is configured with a common cathode (see 6.6).
R	The "R" designator indicates that the device is configured with a common anode (see 6.6).
CAT1	The "CAT1" designators indicates that the device is configured with a common anode.
CCT1	The "CCT1" designators indicates that the device is configured with a common cathode.
DT1	The "DT1" designators indicates that the device is configured as a doubler.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS 19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods For Semiconductor Devices.
* MIL-STD-883 - Test Methods Standard Microcircuits.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

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2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish, formation and material.

3.4.1.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein (see 6.6.3). Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.1.2 Lead formation. When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein. Where a choice of lead formation is desired, it shall be specified in the acquisition document (see 6.2).

3.4.1.3 Lead material. The lead material shall consist of an iron-nickel or iron-nickel-cobalt alloy that is intended primarily for sealing the lead to the ceramic used for electrical isolation (see 6.6.3).

3.4.2 Electrical isolation of leads. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent Al₂O₃ (ceramic).

3.4.3 Polarity. Polarity and terminal configuration of the device types shall be in accordance with figure 1.

* 3.4.4 Silicone die coating. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883 on each lot of silicone die coating for its intended applications.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

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4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and [tables I and II](#) herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.2 Silicone die coating. When silicone die coating is used, method 5011 of [MIL-STD-883](#) shall be performed on that coating in the full [MIL-PRF-19500](#) qualification process.

4.3 Screening (quality levels JANS, JANTXV, and JANTX only). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTX and JANTXV levels
(1) (2) 3b	Surge current and impulse clamp voltage (see 4.3.1)	Surge current and impulse clamp voltage (see 4.3.1)
3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
3d	Avalanche energy test (see 4.3.3)	Avalanche energy test (see 4.3.3)
4	Required	Not applicable
5	Method 2052 of MIL-STD-750 , PIND (see MIL-PRF-19500 and 4.3.5)	Not applicable
8	Required	Not applicable
9, 10	Not applicable	Not applicable
11	V_{F1} and I_{R1}	V_{F1} and I_{R1}
12	High temperature reverse bias (see 4.3.4)	High temperature reverse bias (see 4.3.4), $t = 48$ hours.
13	Subgroups 2 and 3 of table I herein, V_{F1} and I_{R1} , excluding thermal impedance; $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 25$ μ A dc or ± 100 percent from the initial value, whichever is greater.	Subgroup 2 of table I herein, V_{F1} and I_{R1} , excluding thermal impedance; $\Delta V_{F1} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 25$ μ A dc or ± 100 percent from the initial value, whichever is greater.
15	Required	Not applicable

(1) Surge shall precede thermal impedance.

(2) Surge and thermal impedance shall be performed any time after sealing provided temperature cycling is performed in accordance with [MIL-PRF-19500](#), screen 3a and before screen 13. JANTX and JANTXV levels do not need to be repeated in screening requirements.

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4.3.1 Surge current and impulse clamp voltage. The surge current and impulse clamp voltage test shall be performed in accordance with condition A of method 4066 of MIL-STD-750. The following details shall apply: $I_o = 0$, one current pulse, $t_p = 8.3\text{ms}$, $I_{FSM} = 1.3$ herein, and $V_{RWM} = 0$.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , and t_{MD} . See table III, subgroup 4 herein.

4.3.3 Avalanche energy test. The avalanche energy test shall be performed in accordance with method 4064 of MIL-STD-750 using the circuit as shown on figure 6 or equivalent. The Schottky rectifier under test shall be capable of absorbing the reverse energy, as follows: $I_{AS} = 2\text{ A}$ minimum, $L = 260\text{ }\mu\text{H}$.

4.3.4 High temperature reverse bias. The high temperature reverse bias of devices shall be performed in accordance with test condition A of method 1038 of MIL-STD-750. The following details shall apply: $V_R = 36\text{ V dc}$; $T_J = +125^\circ\text{C}$.

* 4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein. Delta measurements shall be in accordance with the applicable steps of table II herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (JANS) and E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with table II herein.

4.4.2.1 Quality level JANS.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
* B3	2052	PIND, required if not performed in screening. (22 devices, $c = 0$ for large lots, 12 devices, $c = 0$ for small lots).
B4	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2\text{ A}$ minimum for 2,000 cycles.
B5	1038	Condition A, $V_R = 36\text{ V dc}$, $T_J = +125^\circ\text{C}$, $t = 340\text{ hours min}$; heat sinking allowed. This test shall be extended to 1000 on each JANS wafer lot.
B6	4081	1N6660CAT1, 1N6660DT1 (die 1), $R_{\theta JC} = 2.8^\circ\text{C/W}$ maximum for each leg. 1N6660CCT1, 1N6660DT1 (die 2), $R_{\theta JC} = 1.65^\circ\text{C/W}$ maximum for each leg.

4.4.2.2 Quality level JAN, JANTX, and JANTXV.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1037	$\Delta T_C = +85^\circ\text{C}$ minimum, $I_F = 2\text{ A}$ minimum for 2,000 cycles.

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4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#). Delta measurements shall be in accordance with [table II](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Condition A, weight = 10 lbs (4.54 kg), t = 15 seconds.
* C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C6	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2$ A minimum for 6,000 cycles.
C6	1038	Condition A, $V_R = 36\text{V}$ dc, $T_J = 125^\circ\text{C}$, t = 1000 hours minimum (for TX, TXV only); (heat sinking allowed).

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table III](#) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of [MIL-STD-750](#).

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TABLE I. Group A inspection. [1/](#) [2/](#)

Inspection	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance 3/	3101	See 4.3.2	$Z_{\theta JC}$			°C/W
1N6660CAT1, 1N6660DT1 (die 1)						
1N6660CCT1, 1N6660DT1 (die 2)						
Forward voltage	4011	Condition B, $I_F = 5$ A (pk) pulsed (see 4.5.1)	V_{F1}		0.55	V dc
		$I_F = 15$ A (pk) pulsed (see 4.5.1)	V_{F2}		0.75	V dc
		$I_F = 30$ A (pk) pulsed (see 4.5.1)	V_{F3}		1.0	V dc
Reverse current leakage	4016	Condition A or B, Pulsed DC method (see 4.5.1), $V_R = 45$ V dc,	I_{R1}		1.0	mA dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +125^\circ\text{C}$				
Reverse current leakage	4016	Condition A or B, Pulsed DC method (see 4.5.1), $V_R = 45$ V dc	I_{R2}		40	mA dc
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward voltage	4011	Condition B, $I_F = 15$ A (pk) pulsed (see 4.5.1)	V_{F4}		0.8	V dc
<u>Subgroup 4</u>						
Junction capacitance	4001	$V_R = 5$ V dc; $f = 1$ MHz; $V_{SIG} = 50$ mV (p-p) (max)	C_J		2,000	pF
<u>Subgroup 6</u>						
Surge	4066	Condition A, $I_{FSM} = 300$ A (pk), 8.3 ms; pulsed (see 4.5.1)				
Electrical measurements		See table I , subgroup 2 herein				

See footnotes at end of table.

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TABLE I. Group A inspection - Continued. 1/ 2/

Inspection	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u>						
Dielectric withstanding voltage	1016	$V_R = 500$ V dc; all leads shorted; V as measured from leads to case	I_{RES}		10	μA
Scope display evaluation	4023	Condition A, Stable only				
Electrical measurements		See table I , subgroup 2 herein				

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Each individual diode.

3/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
Group C, subgroups 2, and 6.
Group E, subgroup 1.

TABLE II. Groups A, B, C, and E electrical end-point and delta measurements. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits	Limits	Unit
		Method	Conditions		Min	Max	
1.	Forward voltage	4011	Condition B, $I_F = 5$ A (pk), pulsed (see 4.5.1)	ΔV_{F1}	± 50 mV dc from initial reading. ± 25 μA dc or ± 100 percent from initial reading, whichever is greater.		
2.	Reverse current	4016	Condition A or B, Pulsed DC method (see 4.5.1), $V_R = 45$ V dc.	ΔI_{R1}			

1/ Each individual diode.

2/ The electrical measurements for table E-VIA (JANS) of [MIL-PRF-19500](#) are as follows:

- Subgroup 3, see table II herein, steps 1 and 2.
- Subgroup 4, see table II herein, steps 1 and 2.
- Subgroup 5, see table II herein, steps 1 and 2.

3/ The electrical measurements for table E-VIB (JANTX and JANTXV) of [MIL-PRF-19500](#) are as follows:

- Subgroup 2, see table II herein, steps 1 and 2.
- Subgroup 3, see table II herein, steps 1 and 2.
- Subgroup 6, see table II herein, steps 1 and 2.

4/ The electrical measurements for table E-VII of [MIL-PRF-19500](#) are as follows:

- Subgroups 2 and 3, see table II herein, steps 1 and 2.
- Subgroup 6, see table II herein, steps 1 and 2.

5/ The electrical measurements for table E-IX of [MIL-PRF-19500](#) are as follows:

- Subgroup 1, see table II herein, steps 1 and 2.
- Subgroup 2, see table II herein, steps 1 and 2.

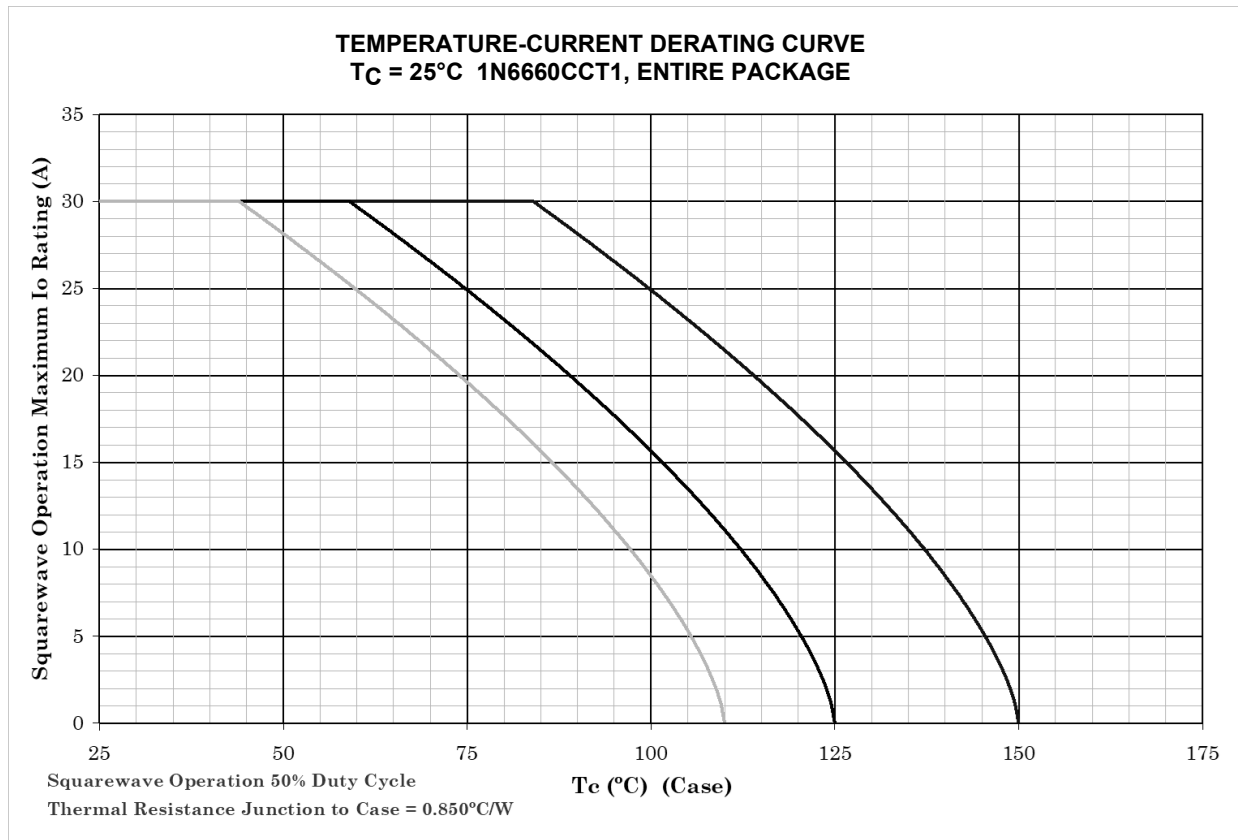
6/ Devices which exceed the table I, limits for this test shall not be accepted.

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TABLE III. Group E inspection (all quality levels) for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			
Temperature cycling	1051	500 cycles	n = 45, c = 0
Hermetic seal	1071		
Electrical measurements		See group A, subgroup 2, and table II	
<u>Subgroup 2</u>			
Steady-state blocking life	1048	t = 1,000 hours, T _J = +125°C; V _R = 36 V dc	n = 45, c = 0
Electrical measurements		See table I , subgroup 2, and table II	
<u>Subgroup 3</u>			
Not applicable			
<u>Subgroup 4</u>			
Thermal impedance curves	3101	See MIL-PRF-19500	
<u>Subgroup 6</u>			
ESD	1020		
<u>Subgroup 10 1/</u>			
Surge	4066	Condition A; T _A = +25°C; I _{FSM} = 300 A, 100 surges	n = 22, c = 0
Electrical measurements		See table I , subgroup 2	

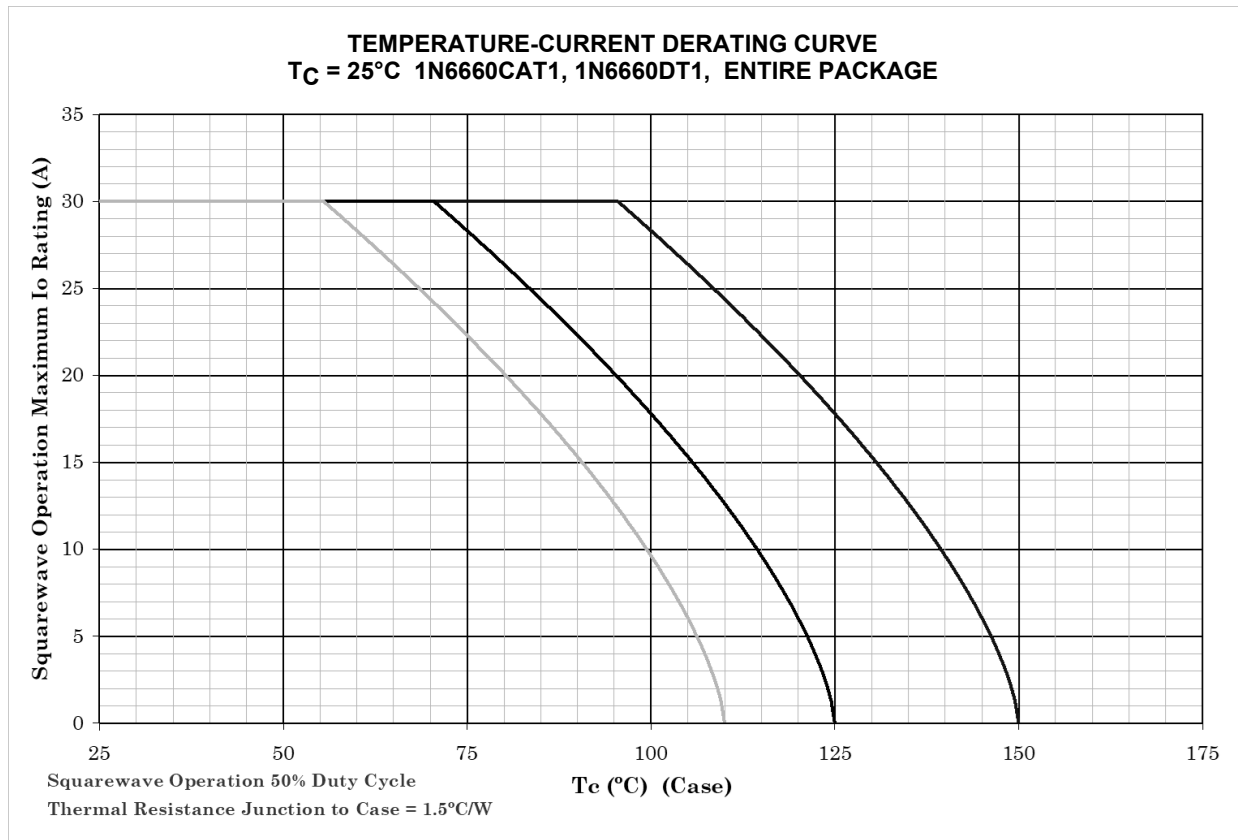
1/ For each diode.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 150^\circ\text{C}$) and power rating specified (see 1.3 herein.)
3. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show current rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-current derating graph.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 150^\circ\text{C}$) and power rating specified (see 1.3 herein.)
3. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show current rating where most users want to limit T_J in their application.

FIGURE 3. Temperature-current derating graph 1N6660CAT1, 1N6660DT1, die 1.

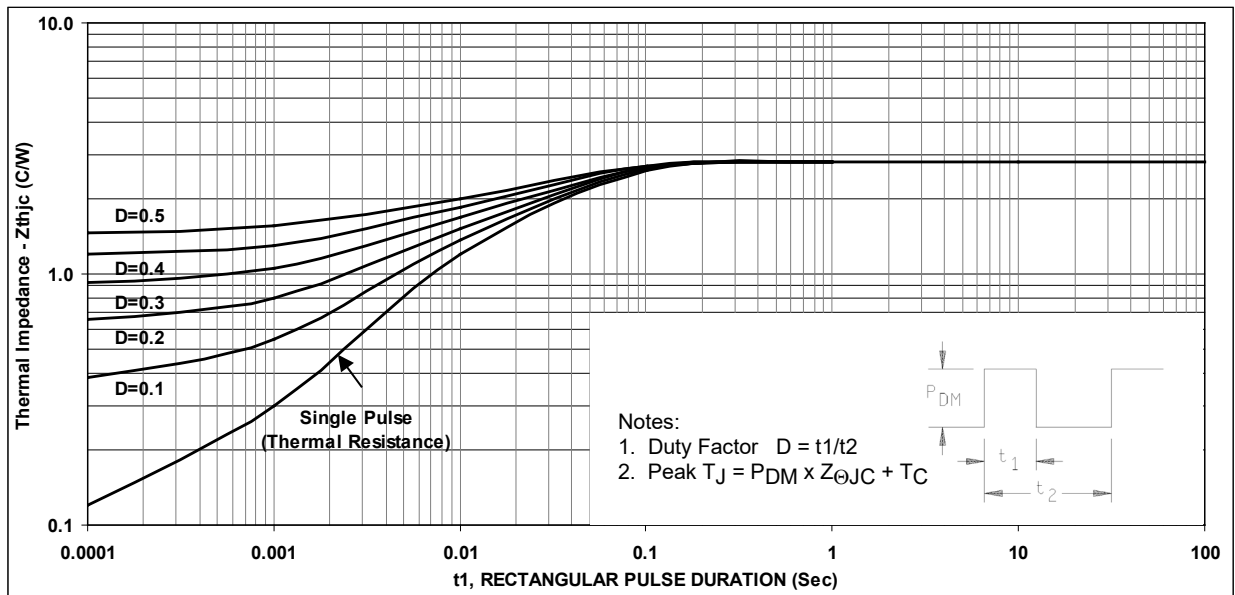


FIGURE 4. Thermal impedance for each leg 1N6660CAT1, 1N6660DT1, die 1, and 1N6660R.

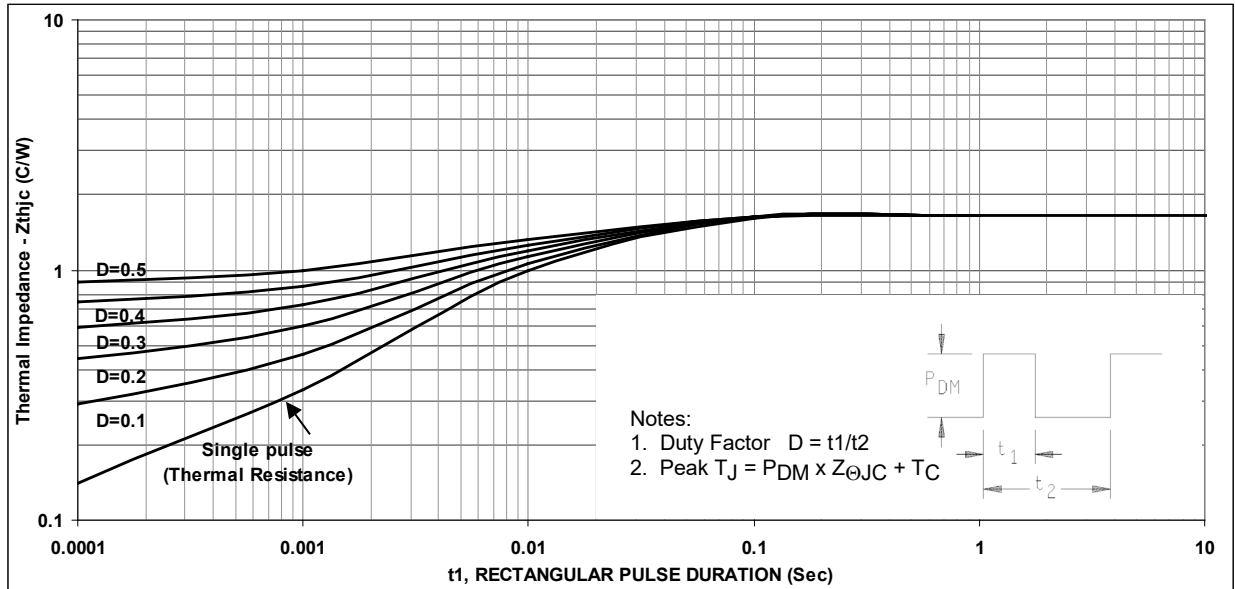
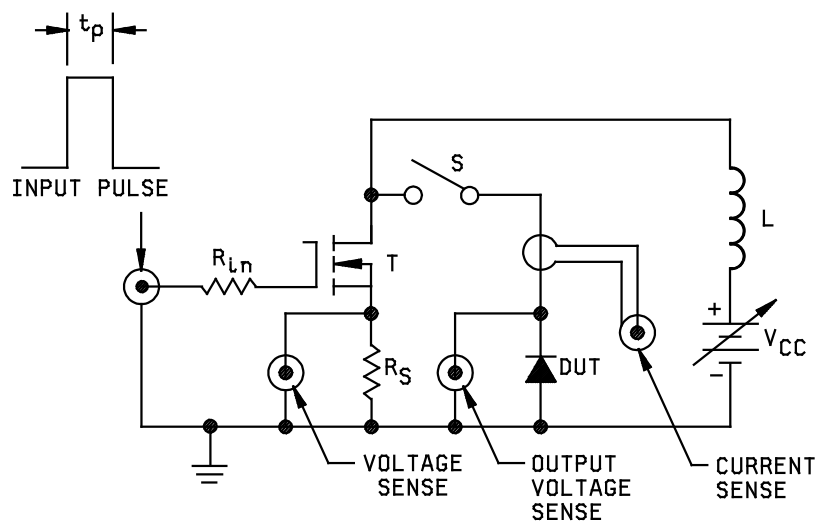


FIGURE 5. Thermal impedance for each leg 1N6660CCT1, 1N6660DT1, die 2, and 1N6660.

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Input pulse: $R_{in} = 50$ ohms
 $V_G = 10$ volts, $R_S = 0.1$ ohms
 $Z_G = 50$ ohms, $V_{CC} \approx 10$ volts
 $L = 260 \mu\text{H}$
Duty cycle ≤ 1 percent, $T = 2\text{N}6756$ or equivalent

PROCEDURES:

1. With S open, adjust pulse width to test current of 2 amps through R_S .
2. Close S , verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

FIGURE 6. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

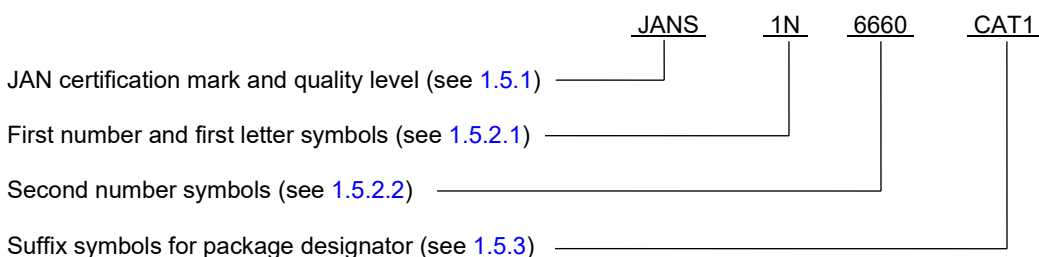
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead material, finish, and formation (see [3.4.1](#)).
- d. The complete PIN, see [1.5](#) and 6.4.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



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6.5 List of PINs. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

JAN quality level	JANTX quality level	JANTXV quality level	JANS quality level
JAN1N6660CAT1	JANTX1N6660CAT1	JANTXV1N6660CAT1	JANS1N6660CAT1
JAN1N6660CCT1	JANTX1N6660CCT1	JANTXV1N6660CCT1	JANS1N6660CCT1
JAN1N6660DT1	JANTX1N6660DT1	JANTXV1N6660DT1	JANS1N6660DT1

6.6 Replacement data.

6.6.1 Superseded PINs. The following supersession data applies to PINs associated with this document:

Superseding PIN as specified within MIL-PRF-19500/608B, dated 17 August 2005	Original PIN as specified within MIL-S-19500/608, dated 22 April 1993
JAN1N6660CCT1	JAN1N6660
JAN1N6660CAT1	JAN1N6660R
JANTX1N6660CCT1	JANTX1N6660
JANTX1N6660CAT1	JANTX1N6660R
JANTXV1N6660CCT1	JANTXV1N6660
JANTXV1N6660CAT1	JANTXV1N6660R
JANS1N6660CCT1	JANS1N6660
JANS1N6660CAT1	JANS1N6660R

6.6.2 Interchangeability. The PINs and device types 1N6660CCT1 and 1N6660CAT1 are interchangeable with the obsolete PINs of device types 1N6660 and 1N6660R respectively.

6.6.3 Lead material. The original issue of this specification through MIL-PRF-19500/608A with Amendment 1 (22 February 1999) did not specify a lead material. MIL-PRF-19500/608B (17 August 2005) added a requirement for either "Alloy 52" or "Kovar" as the lead material. These lead materials were added to address issues with the TO-254AA package and to prevent latent package sealing problems. Because this document is classified as a performance specification sheet, this specific design solution for a lead material is no longer appropriate.

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at "Semiconductor@dla.mil" or by facsimile (614) 693-1642 or DSN 850-6939.

6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

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Custodians:

Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2024-057)

Review activities:

Army - AR, MI, SM
Navy - AS, MC, OS
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.