The documentation and process conversion measures necessary to comply with this document shall be completed by 26 December 2024.

INCH-POUND

MIL-PRF-19500/603L
w/AMENDMENT 3
26 July 2024
SUPERSEDING
MIL-PRF-19500/603L
w/AMENDMENT 2
27 June 2019

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE ONLY), N-CHANNEL, SILICON, (THROUGH-HOLE, SURFACE MOUNT, AND CARRIER BOARD PACKAGES), TYPES 2N7268, 2N7269, 2N7270, 2N7394,
JANTXVR, F, G, H; JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened (total dose only), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Provisions for radiation hardness assurance (RHA) to four radiation levels (“R”, “F”, “G”, and “H”) are provided for JANTXV and JANS product assurance levels. See 6.7 for JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with figure 1 and TO-276AB (U) in accordance with figure 2 for all encapsulated device types. TO-276AB with lead option (U1L) in accordance with figure 3, TO-276AB with carrier board option (U1S) in accordance with figure 4. See 6.7 for unencapsulated devices.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Type (1)	P_T (2)	P_T T_A = +25°C	$R_{\theta JA}$	$R_{\theta JC}$ (3)	$R_{\theta J}$ Carrier board U1S	$R_{\theta J}$ Lid U1L (4)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (5) (6)	I_{D2} (5) (6) T_C = +100°C
	W	W	°C/W	°C/W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc
2N7394, 2N7394U	150	4	35	0.83	1.5	10	60	60	±20	35.0	30.0
2N7268, 2N7268U	150	4	35	0.83	1.5	10	100	100	±20	34.0	21.0
2N7269, 2N7269U	150	4	35	0.83	1.5	10	200	200	±20	26.0	16.0
2N7270, 2N7270U	150	4	35	0.83	1.5	10	500	500	±20	11.0	7.0

Continued next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A
FSC 5961

* DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C - Continued.

Type (1)	I_{DM}	T_J and T_{STG}	V_{ISO} 70,000 ft altitude	I_S
	A(pk)	°C	V dc	A dc
2N7394, 2N7394U	140	-55 to +150	N/A	35.0
2N7268, 2N7268U	136		N/A	34.0
2N7269, 2N7269U	104		N/A	26.0
2N7270, 2N7270U	44		500	11.0

(1) Electrical characteristics for the “U1L” and “U1S” suffix devices are identical to the non-suffix devices unless otherwise noted.
(2) Derate linearly 1.2 W/°C for T_C > +25°C. Does not apply to U1L and U1S devices.
(3) See figure 5 thermal impedance curves.
(4) The Thermal resistance is applicable for mounting methods where a heatsink is attached to the lid for U1L suffix devices.
(5) The following formula derives the maximum theoretical I_D limit. I_D is limited by package design:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(6) See figure 6 for maximum drain current graphs.

1.4 Primary electrical characteristics at T_c = +25°C.

Type (1)	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (2) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = +25°C at I_{D2}	T_J = +150°C at I_{D2}		
	V dc	Min	Max	µA dc	ohm	ohm	mJ	A
		V dc	V dc					
2N7394, 2N7394U	60	2.0	4.0	25	0.027	0.030	500	35.0
2N7268, 2N7268U	100	2.0	4.0	25	0.065	0.132	500	34.0
2N7269, 2N7269U	200	2.0	4.0	25	0.100	0.230	500	26.0
2N7270, 2N7270U	500	2.0	4.0	50	0.450	1.260	500	11.0

(1) Electrical characteristics for the “U1L” and “U1S” suffix devices are identical to the non-suffix devices unless otherwise noted.
(2) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JANTXV” and "JANS".

* 1.5.2 RHA designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7268", "7269", “7270” and "7394".

1.5.3.3 Suffix letters. No suffix letters are used on devices that are packaged in the TO-254AA package of figure 1. The suffix letter "U" (in lieu of "U1") is used on devices that are packaged in the TO-276AB package of figure 2. The suffix letters "U1L" are used on devices that are packaged in the TO-276AB package and have additional flat leads added, see figure 3. The suffix letters "U1S" are used on devices that are packaged in the TO-276AB package mounted to a carrier board, see figure 4.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

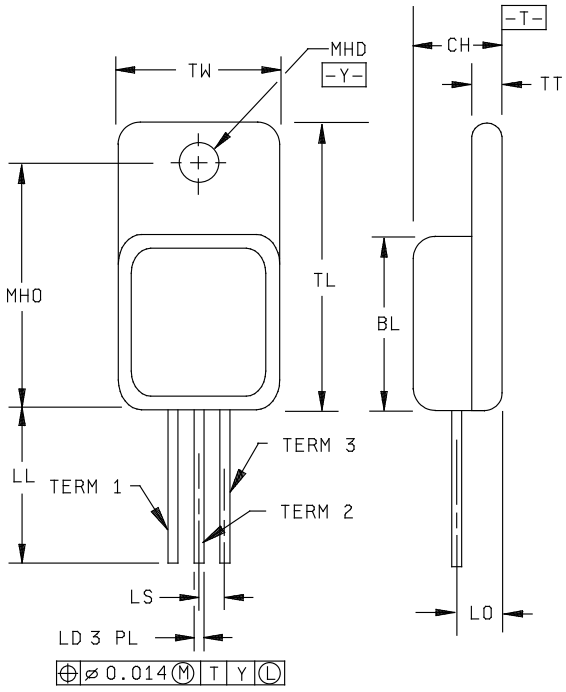
* 1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

For device type 2N7394, 2N7268, 2N7269, 2N7270: ..... 500 krads(Si) 1/

For device type, 2N7394U, 2N7268U, 2N7269U, 2N7270U: ..... 500 krads(Si) 1/

* 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 500 krads(Si).

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
Term 1	Drain			
Term 2	Source			
Term 3	Gate			



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Refer to applicable symbol list.
4. All terminals are isolated from case.

* FIGURE 1. Physical dimensions for TO-254AA (2N7268, 2N7269, 2N7270, and 2N7394).

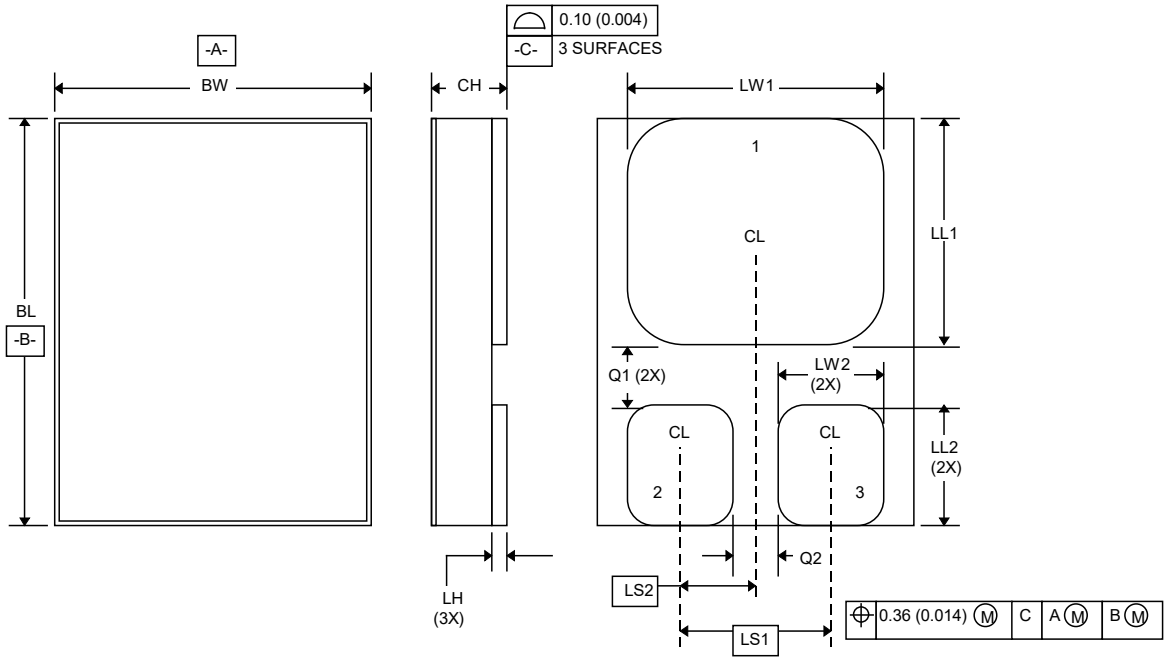
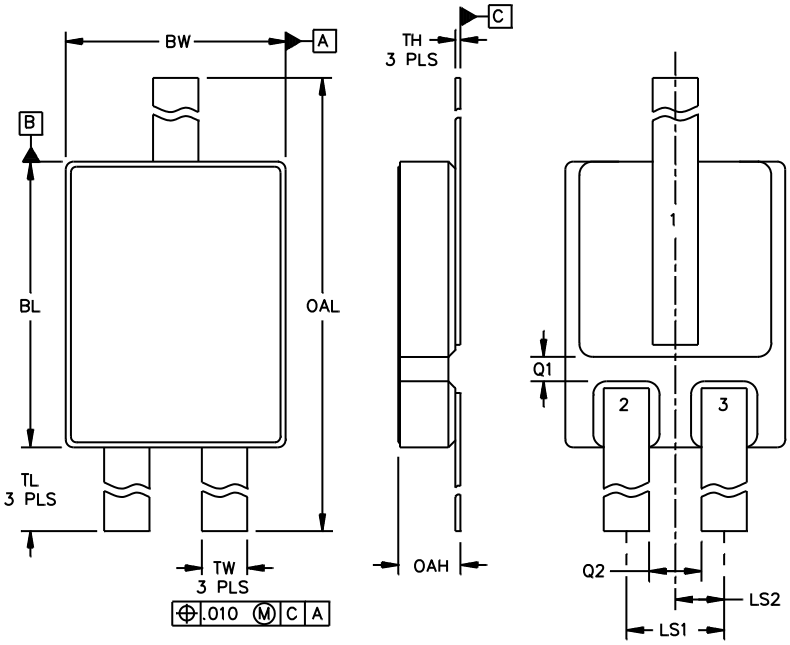


FIGURE 2. Dimensions and configuration of surface mount package outline, TO-276AB (2N7268U, 2N7269U, 2N7270U, AND 2N7394U).

Dimensions				
Symbol	SMD-1			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL_1	.410	.420	10.41	10.67
LL_2	.152	.162	3.86	4.11
LS_1	.210 BSC		5.33 BSC	
LS_2	.105 BSC		2.67 BSC	
LW_1	.370	.380	9.40	9.65
LW_2	.135	.145	3.43	3.68
Q_1	.030		0.76	
Q_2	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. This suffix "U" for this package was assigned before the "U1" was assigned to the TO-276AB package used in other slash sheets.

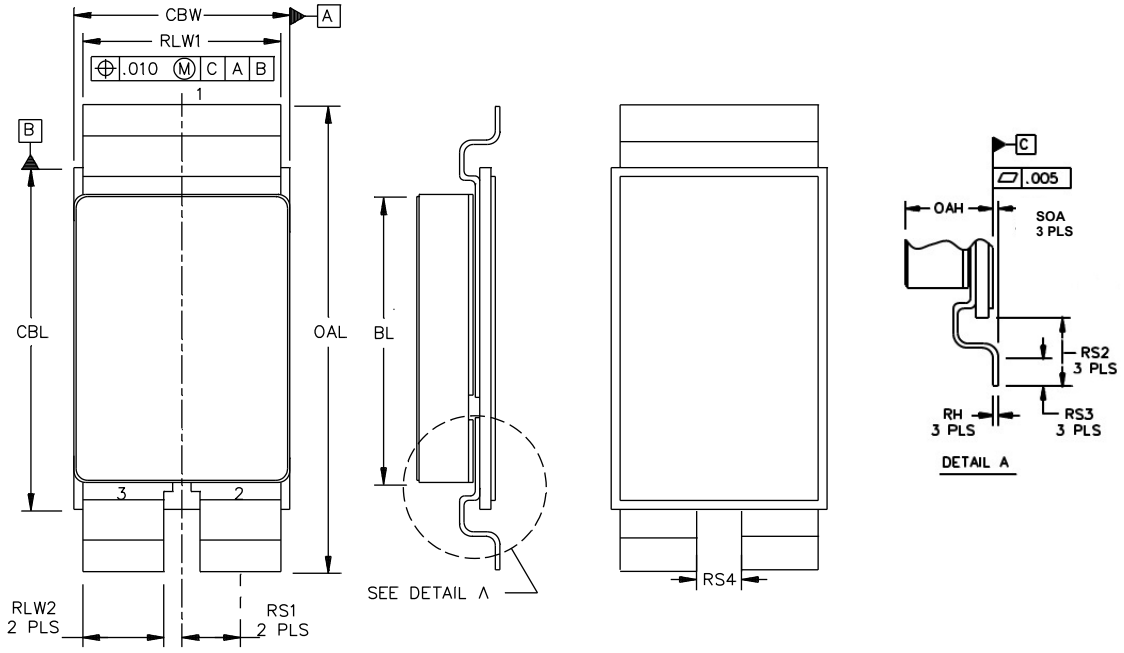
* FIGURE 2. Dimensions and configuration of surface mount package outline, TO-276AB (2N7268U, 2N7269U, 2N7270U, AND 2N7394U) - Continued.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
* BW	.445	.455	11.31	11.55
LS1	.210 BSC		5.33 BSC	
LS2	.105 BSC		2.67 BSC	
Q1	.030		0.76	
Q2	.035		0.89	
TH	.005	.007	0.127	0.177
TL	.650	.680	16.51	17.27
TW	.095	.105	2.42	2.66
OAH		.150		3.81
OAL	1.92	1.99	48.77	50.54
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* FIGURE 3. Physical dimensions, U with leaded option (2N7268U1L. 2N7269U1L, 2N7270U1L, and 2N7394U1L).



.010 M C A B

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
CBL	.825	.840	20.96	21.34
CBW	.520	.535	13.21	13.59
OAH	.174	.204	4.42	5.18
OAL	1.109	1.144	28.17	29.06
RH	.009	.015	0.23	0.38
RLW1	.473	.497	12.01	12.62
RLW2	.178	.202	4.52	5.13
RS1	.1475 BSC		3.75 BSC	
RS2	.142	.152	3.61	3.86
RS3	.045	.055	1.14	1.40
RS4	.093		2.36	
SOA	.005	.015	0.13	0.38
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* FIGURE 4. Physical dimensions, U with carrier board option (2N7268U1S, 2N7269U1S, 2N7270U1S, and 2N7394U1S).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Method Standard Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS} ..... Rated avalanche current, non-repetitive.
nC ..... nano Coulomb.
PIND ..... Particle impact noise detector.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, and 4 herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction is not permitted.

3.4.3 Lead attach or Carrier package. Alternations to the device shall be performed on devices that have passed all screening and QCI required per MIL-PRF-19500 and listed herein. When leads or carrier attach is added to the U package, as a minimum, the vendor shall perform the tests specified in 4.3.6 herein.

* 3.4.4 Silicone die coat. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883, on each lot of silicone die coating for its intended applications.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. Devices that have been altered with lead or carrier attached per the specification herein shall have the altered part number on the device or on the device packaging.

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.2 Lead or carrier attach. For devices that include a lead or carrier attach package configuration, qualification shall be performed in accordance with table IV herein, at initial qualification and after process or design changes.

* 4.2.3 Silicone die coating. When silicone die coating is used, method 5011 of MIL-STD-883 shall be performed on that coating in the full MIL-PRF-19500 qualification process.

* 4.3 Screening (JANTXV and JANS levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTXV levels
(3)	Gate stress test (see 4.3.1).	Gate stress test (see 4.3.1).
(3)	Single pulse avalanche energy test, method 3470 of MIL-STD-750 (see 4.3.2).	Single pulse avalanche energy test, method 3470 of MIL-STD-750 (see 4.3.2).
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.3).	Method 3161 of MIL-STD-750 (see 4.3.3).
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.5)	Not applicable
9	Subgroup 2 of table I herein.	Subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A.	Method 1042 of MIL-STD-750, test condition A.
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =± 20 percent of initial value $\Delta V_{GS(th)1}$ = ± 20 percent of initial value.	Subgroup 2 of table I herein ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ =± 20 percent of initial value $\Delta V_{GS(th)1}$ = ± 20 percent of initial value.
17	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein. (Not applicable for TO-276AB surface mount devices).	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein. (Not applicable for TO-276AB surface mount devices).

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $V_{GS(th)1}$, and $r_{DS(ON)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy E_{AS}.

a. Peak current (I_{AS}) ..... $I_{AS(max)}$.

b. Peak gate voltage (V_{GS}) ..... 12 V.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance (L) ..... $L = (2E_{AS}/(I_{D1})^2)((V_{BR}-V_{DD})/V_{BR})$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V for 2N7268, 2N7394, 2N7268U, 2N7268U1L, 2N7268U1S, 2N7394U, 2N7394U1L, and 2N7394U1S, 50 V for 2N7269, 2N7269U, 2N7269U1L, 2N7269U1S, and 2N7270, 2N7270U, 2N7270U1L, and 2N7270U1S.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, t_{SW}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage ..... 900 V dc.

b. Duration of application of test voltage ..... 15 seconds (min).

c. Points of application of test voltage ..... All leads to case (bunch connection).

d. Method of connection ..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200V /1.0 mA (min).

f. Maximum leakage current ..... 1.0 mA.

g. Voltage ramp up time ..... 500 V /second.

4.3.5 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.6 Lead or carrier attach screening (All quality levels). All surface mount devices with added leads or carrier boards shall be screened as specified herein following screening and quality conformance inspection.

Screen	MIL-STD-750 Method	Conditions
1. Hermetic Seal 1/ a. Fine Leak b. Gross Leak	1071	
2. Thermal impedance (see 4.3.3) Electrical measurements 2/ 3/	3161	Read and Record. Read and record in alignment with A2 testing.
3. X-Radiography	2076	The solder material coverage at the package lead pad/SMD carrier sub interfaces shall be 85% minimum
4. External Visual Examination	2071	Cracks or separation of materials shall not be evident on any device after the surface mount device lead attach assembly operation. Pad and Isolation areas shall be free from foreign matter and extraneous solder. Solder filet coverage at the lead/package lead pad interfaces, along all visible sides, minimum of 75% solder fillet coverage.
5a. Physical dimensions	2066	6 piece sample, each device shall meet the requirements specified in figures 3 and 4.
5b. Terminal Strength	2036	3 piece sample.

1/ Evaluation of surface sorption in accordance with method 1071 shall be performed.
2/ Only DC electrical test specified herein.
3/ When lead carrier bend is requested, the electrical test is performed prior to the bend process.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2077	SEM qualification may be performed anytime prior to lot formation.
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	The heating cycle shall be 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours minimum; or, T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours minimum; or, T_A = +150°C, t = 240 hours minimum.
B6		Not applicable for surface mount packages.

4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	The heating cycle shall be 30 seconds minimum.
B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.
B4	2075	See 3.4.2.
B5		Not applicable for surface mount packages.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Test condition A; weight = 10 pounds (4.54 kg); t = 15 s (applicable to TO-254AA only).
C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	Thermal resistance, see 4.3.3. Not required when performed in Group B.
C6	1042	The heating cycle shall be 30 seconds minimum.

* 4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with appendix E, table E-VIII of MIL-PRF-19500 and table II herein.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III (and table IV as applicable) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3.	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 1 mA dc bias condition C	$V_{(BR)DSS}$			
2N7394, 2N7394U				60		V dc
2N7268, 2N7268U				100		V dc
2N7269, 2N7269U				200		V dc
2N7270, 2N7270U				500		V dc
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$ I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+ 100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		- 100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}			
2N7394, 2N7394U					25	µA dc
2N7268, 2N7268U					25	µA dc
2N7269, 2N7269U					25	µA dc
2N7270, 2N7270U					50	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(on)1}$			
2N7394, 2N7394U					0.027	ohm
2N7268, 2N7268U					0.065	ohm
2N7269, 2N7269U					0.100	ohm
2N7270, 2N7270U					0.450	ohm
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), I_D = I_{D1}	$r_{DS(on)2}$			
2N7394, 2N7394U					0.030	ohm
2N7268, 2N7268U					0.070	ohm
2N7269, 2N7269U					0.110	ohm
2N7270, 2N7270U					0.500	ohm
Forward voltage	4011	I_D = I_{D1}, V_{GS} = 0 V dc, condition A	V_{SD}			
2N7394, 2N7394U					1.4	V
2N7268, 2N7268U					1.4	V
2N7269, 2N7269U					1.4	V
2N7270, 2N7270U					1.6	V

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate current	3411	V_{GS} = +20 and -20 V dc bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0; bias condition C V_{DS} = 100 percent of rated V_{DS}	I_{DSS2}		1.0	mA dc
		V_{DS} = 80 percent of rated V_{DS}	I_{DSS3}		0.25	mA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7394, 2N7394U					0.060	ohm
2N7268, 2N7268U					0.132	ohm
2N7269, 2N7269U					0.200	ohm
2N7270, 2N7270U					1.000	ohm
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7394, 2N7394U				12		S
2N7268, 2N7268U				8		S
2N7269, 2N7269U				8		S
2N7270, 2N7270U				4		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc R_G = 2.35Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7394, 2N7394U					27	ns
2N7268, 2N7268U					45	ns
2N7269, 2N7269U					33	ns
2N7270, 2N7270U					45	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Rise time			t_r			
2N7394, 2N7394U					100	ns
2N7268, 2N7268U					190	ns
2N7269, 2N7269U					140	ns
2N7270, 2N7270U					190	ns
Turn-off delay time			$t_{d(off)}$			
2N7394, 2N7394U					75	ns
2N7268, 2N7268U					170	ns
2N7269, 2N7269U					140	ns
2N7270, 2N7270U					190	ns
Fall time			t_f			
2N7394, 2N7394U					75	ns
2N7268, 2N7268U					130	ns
2N7269, 2N7269U					140	ns
2N7270, 2N7270U					130	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figures 7, 8, 9, and 10 t_p = 10 ms minimum V_{DS} = 80 percent of maximum rated V_{DS}, ($V_{DS} \leq 200$)				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7394, 2N7394U					200	nC
2N7268, 2N7268U					160	nC
2N7269, 2N7269U					170	nC
2N7270, 2N7270U					150	nC

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 7 - Continued						
Gate to source charge			Q_{gs}			
2N7394, 2N7394U					60	nC
2N7268, 2N7268U					35	nC
2N7269, 2N7269U					30	nC
2N7270, 2N7270U					30	nC
Gate to drain charge			Q_{gd}			
2N7394, 2N7394U					75	nC
2N7268, 2N7268U					65	nC
2N7269, 2N7269U					60	nC
2N7270, 2N7270U					75	nC
Reverse recovery time	3473	Condition A, di/dt ≤ 100 A/μs, V_{DD} ≤ 30 V, $I_D = I_{D1}$	t_{rr}			
2N7394, 2N7394U					280	ns
2N7268, 2N7268U					570	ns
2N7269, 2N7269U					820	ns
2N7270, 2N7270U					1,100	ns

1/ For sampling plan, see MIL-PRF-19500. Electrical characteristics for the “U1L” and “U1S” suffix devices are identical to the non-suffix devices unless otherwise noted.

2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Preirradiation limits				Postirradiation limits				Unit
	Method	Conditions		R		3/ F, G, and H		R		3/ F, G, and H		
				Min	Max	Min	Max	Min	Max	Min	Max	
Subgroup 1												
Not applicable												
Subgroup 2		T_C = +25°C										
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = 12 V V_{DS} = 0										
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)										
End-point electricals												
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 1 mA bias cond. C	V_{BRDSS}									
2N7394, 2N7394U				60		60		60		60		V dc
2N7268, 2N7268U				100		100		100		100		V dc
2N7269, 2N7269U				200		200		200		200		V dc
2N7270, 2N7270U				500		500		500		500		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ I_D = 1 mA	V_{GSth}									
2N7394, 2N7394U				2	4	2	4	2	4	1.25	4.50	V dc
2N7268, 2N7268U				2	4	2	4	2	4	1.25	4.50	V dc
2N7269, 2N7269U				2	4	2	4	2	4	1.25	4.50	V dc
2N7270, 2N7270U				2	4	2	4	2	4	1.25	4.50	V dc
Gate current	3411	V_{GS} = 20 V V_{DS} = 0 bias cond. C	I_{GSSF1}		100		100		100		100	nA dc
Gate current	3411	V_{GS} = -20 V V_{DS} = 0 bias cond. C	I_{GSSR1}		-100		-100		-100		-100	nA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Preirradiation limits				Postirradiation limits				Unit
	Method	Conditions		R		3/ F, G, and H		R		3/ F, G, and H		
				Min	Max	Min	Max	Min	Max	Min	Max	
Subgroup 2 - Continued												
Drain current	3413	Bias cond. C V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS}									
2N7394, 2N7394U					25		25		25		50	µA dc
2N7268, 2N7268U					25		25		25		50	µA dc
2N7269, 2N7269U					25		25		25		50	µA dc
2N7270, 2N7270U					50		50		50		100	µA dc
Static drain to source on-state voltage	3405	Condition A V_{GS} =12 V pulsed see 4.5.1 $I_D = I_{D2}$	V_{DSon1}									
2N7394, 2N7394U					0.81		0.81		0.81		1.2	V dc
2N7268, 2N7268U					1.365		1.365		1.365		1.89	V dc
2N7269, 2N7269U					1.6		1.6		1.6		2.48	V dc
2N7270, 2N7270U					3.15		3.15		3.15		4.2	V dc
Forward voltage source drain diode	4011	Condition A, V_{GS} = 0 $I_D = I_{D1}$	V_{SD}									
2N7394, 2N7394U					1.4		1.4		1.4		1.4	V dc
2N7268, 2N7268U					1.4		1.4		1.4		1.4	V dc
2N7269, 2N7269U					1.4		1.4		1.4		1.4	V dc
2N7270, 2N7270U					1.6		1.6		1.6		1.6	V dc

1/ For sampling plan, see MIL-PRF-19500. Electrical characteristics for the “U1L” and “U1S” suffix devices are identical to the non-suffix devices unless otherwise noted. At the manufacturer’s option, group D samples need not be subjected to the screening tests, and may be assembled in it’s qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ The F designation represent devices which pass end-points at both 100 k and 300 k rads (Si). The G designation represents devices which pass 100 k, 300 k, and 500 k rad (Si) end-points. H must meet end-points for 100 k, 300 k, 500 k and 1,000 k RAD (Si).

4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Thermal shock (temperature cycling)	1051	Test condition G.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			3 devices c = 0
Barometric pressure (2N7270, 2N7270U only)	1001	Test condition C. For device type 2N7270, 2N7270U, 2N7270U1L, 2N7270U1S: V_{DS} = 500 V; $I_{(ISO)}$ < 0.25 mA.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

1/ A separate sample may be pulled for each test condition.

* TABLE IV. Lead alternation Qualification inspection requirements.

Inspections 1/	MIL-STD-750		Sample size
	Method	Conditions	
Subgroup 1			6 devices, c = 0
Temperature cycle	1051	100 Temp cycles, test condition G or maximum storage temperature.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2. Read and record.	
Thermal response	3161		
Visual and mechanical examination	2071	Cracks or separation of materials shall not be evident on test samples.	
Subgroup 2			6 devices, c = 0
Intermittent operating life	1042	Condition D; 6,000 cycles.	
Electrical measurements		See table I, subgroup 2. Read and record.	
Thermal response	3161		
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	
Subgroup 3			6 devices, c = 0
Terminal strength	2036	Tension; Condition A 10lbs (4.54 kg) for 10 seconds Fatigue; Condition E 3 arcs of 90 +/-5 degrees each 8.0 oz.	
Electrical measurements		See table I, subgroup 2. Read and record.	
Visual and mechanical examination	2071	Cracks or separation of materials shall not be evident on test samples.	

1/ Qualification samples performed on non-formed leaded devices.

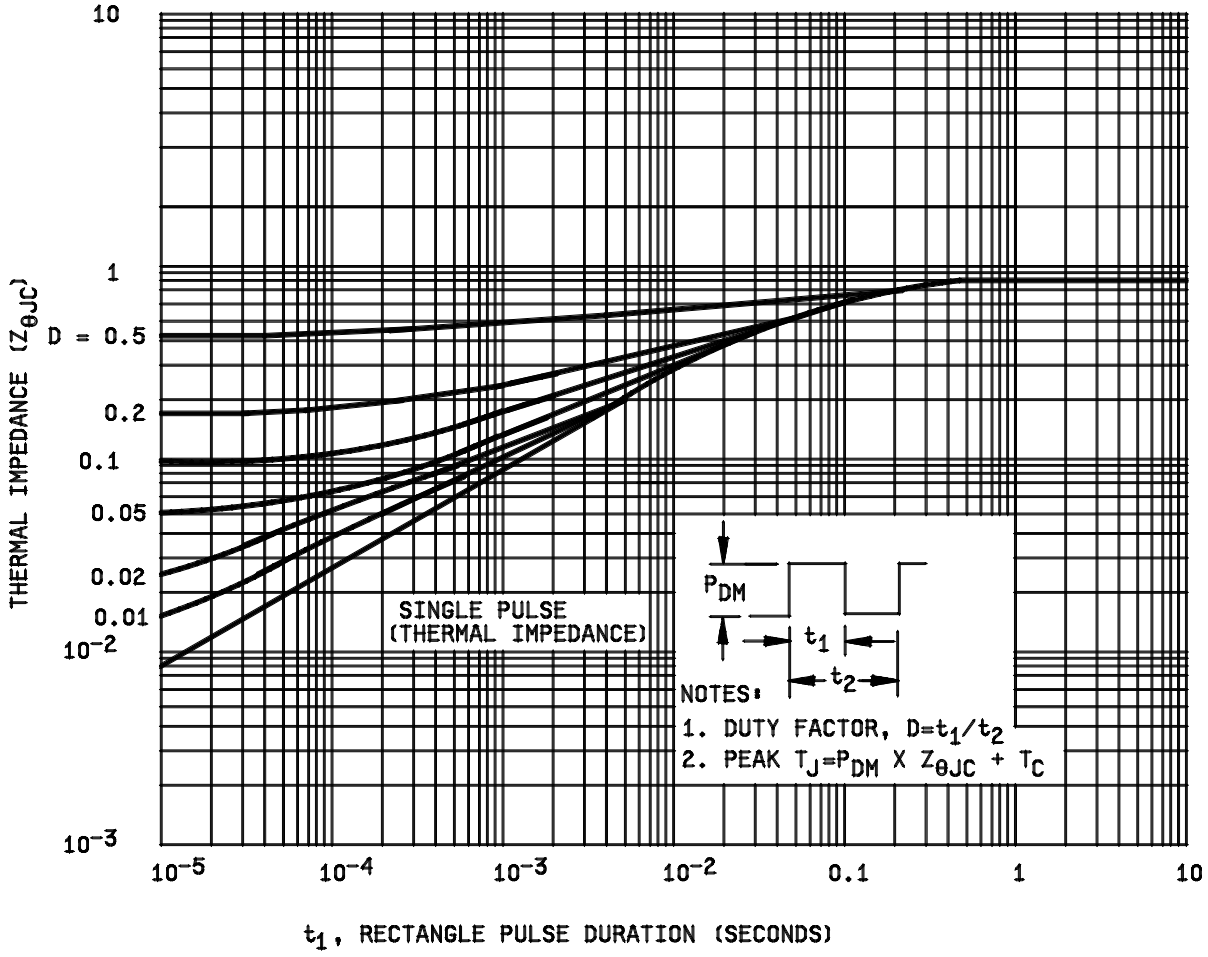
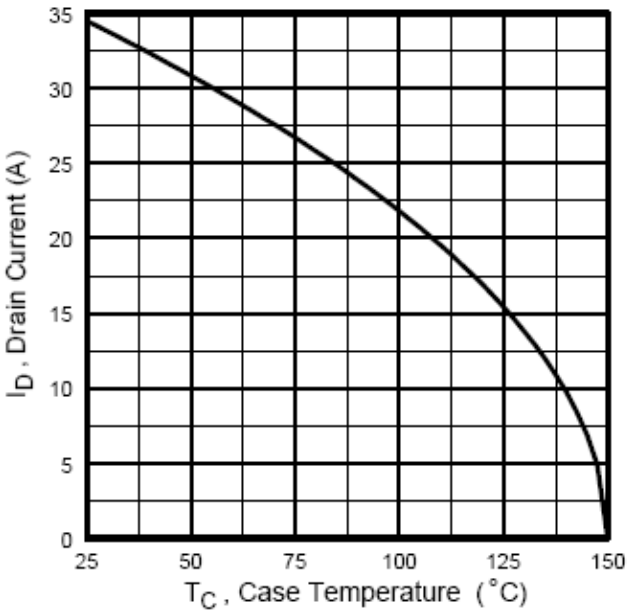


FIGURE 5. Thermal impedance curves.

2N7268, 2N7268U, 2N7268U1L, 2N7268U1S



2N7269, 2N7269U, 2N7269U1L, 2N7269U1S

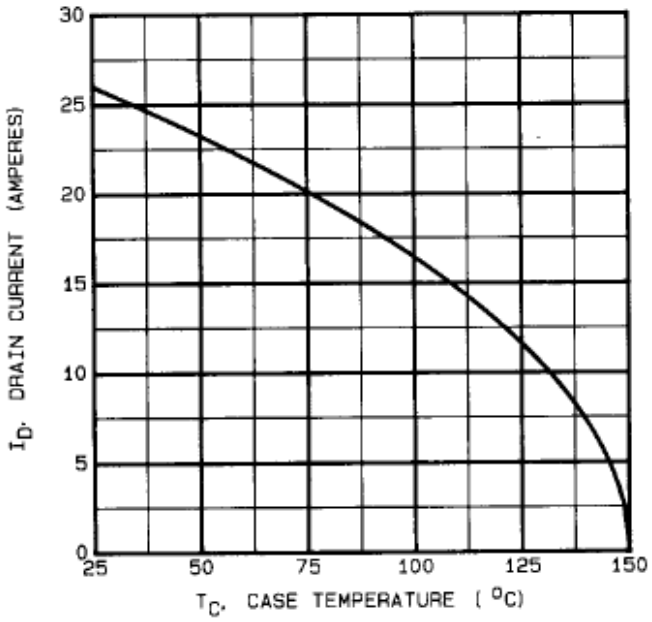
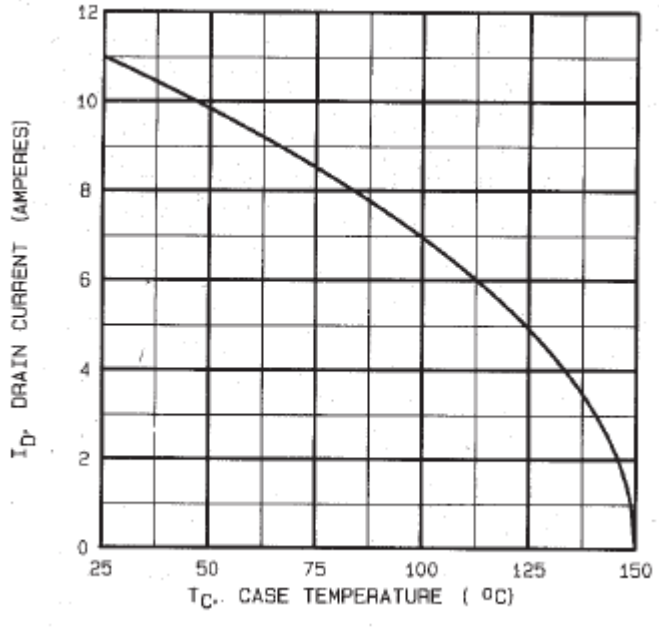


FIGURE 6. Maximum drain current vs case temperature.

2N7270, 2N7270U, 2N7270U1L, 2N7270U1S



2N7394, 2N7394U, 2N7394U1L, 2N7394U1S

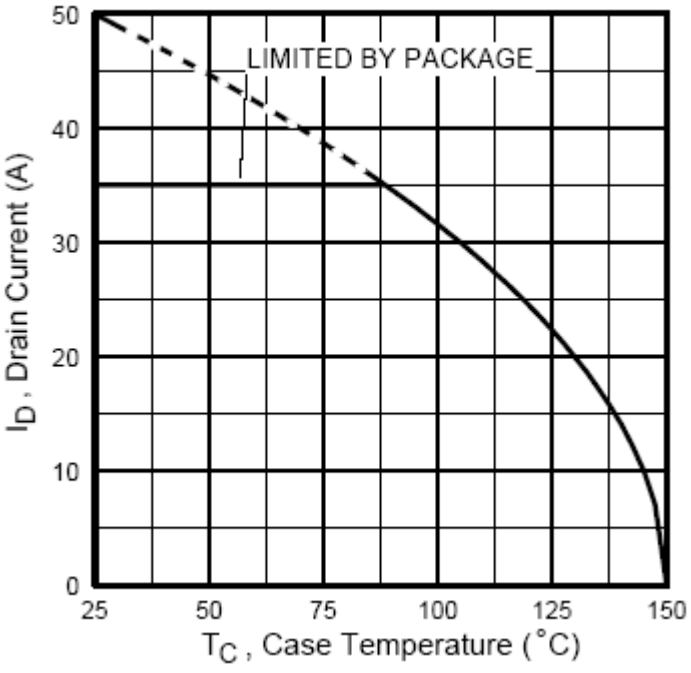


FIGURE 6. Maximum drain current vs case temperature - Continued.

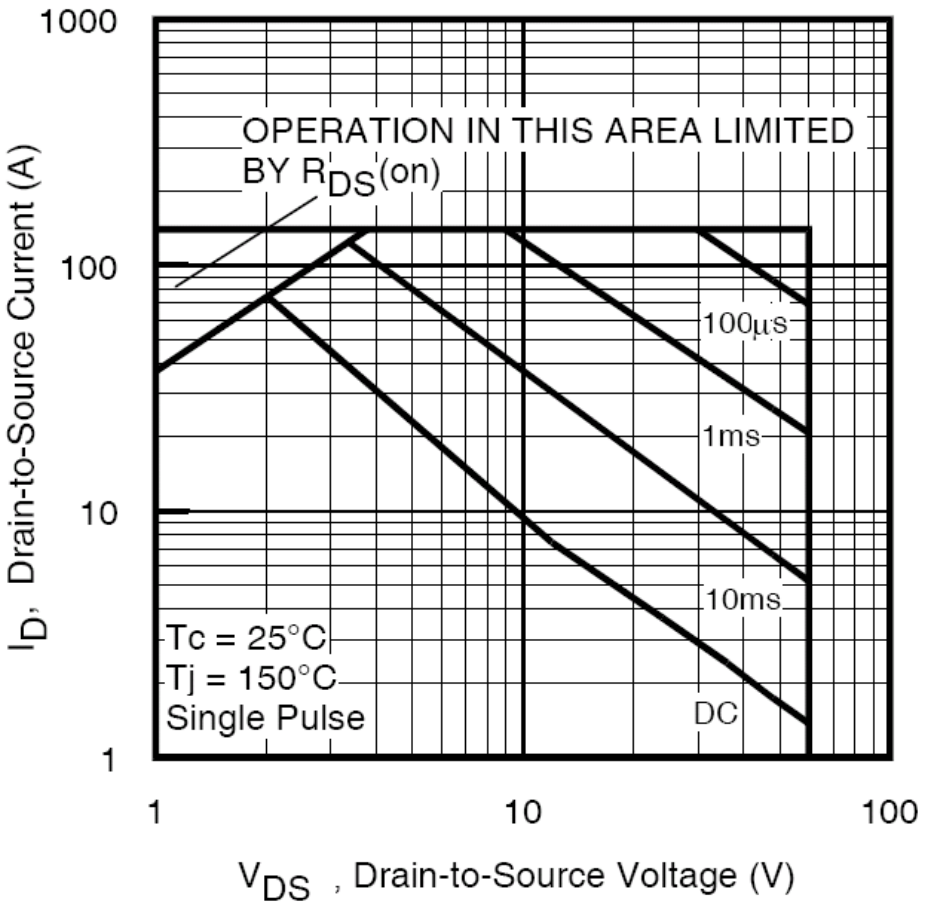


FIGURE 7. Safe-operating-area graphs.

* 2N7394U, 2N7394U1L, 2N7394U1S

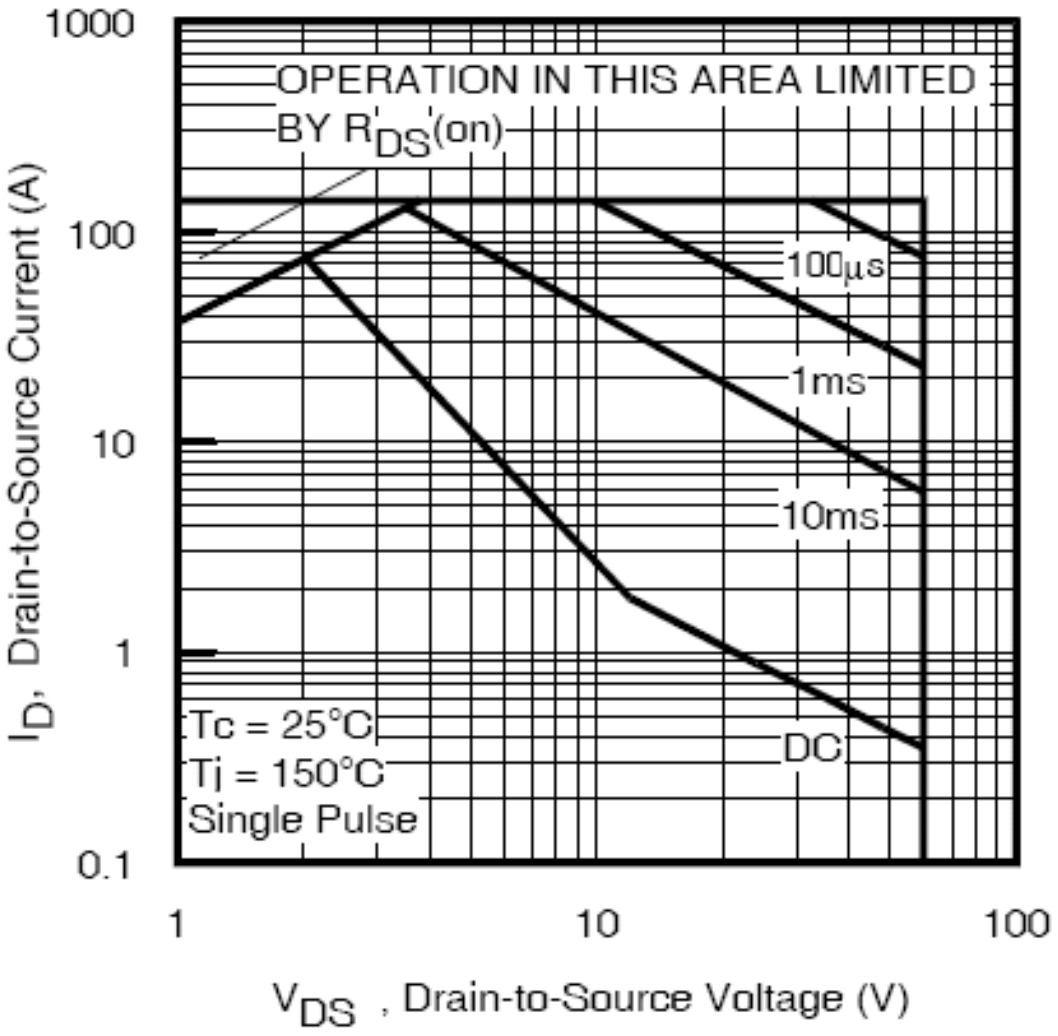


FIGURE 7. Safe-operating-area graphs - Continued

2N7268

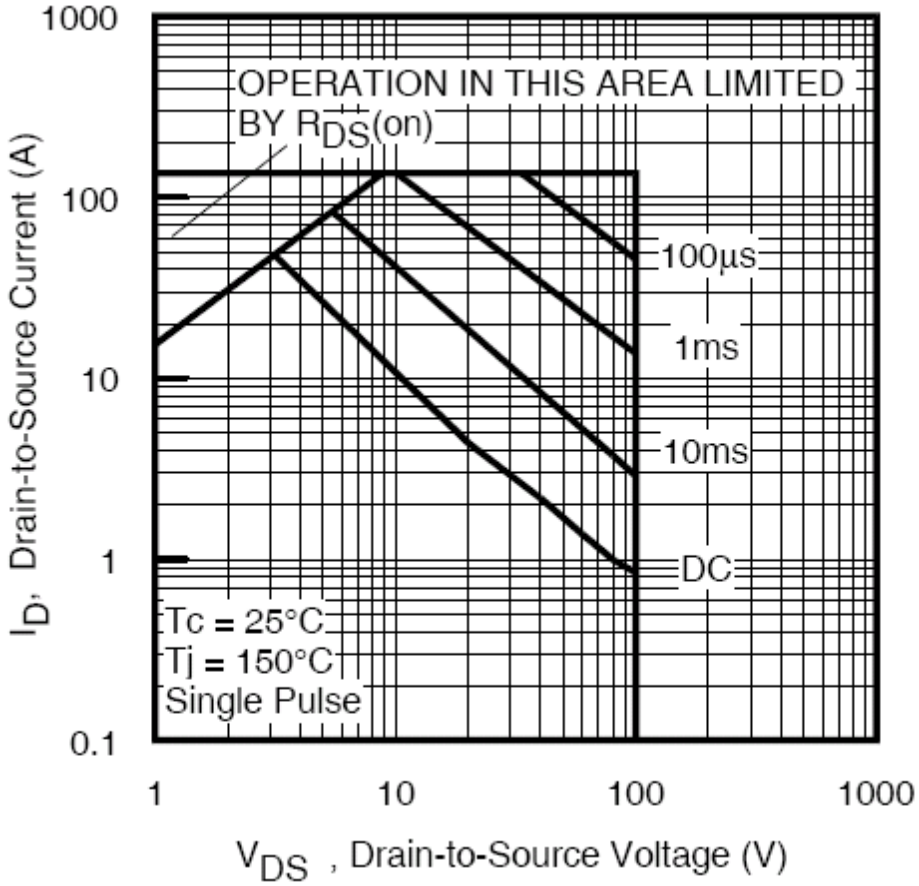


FIGURE 8. Safe-operating-area graphs.

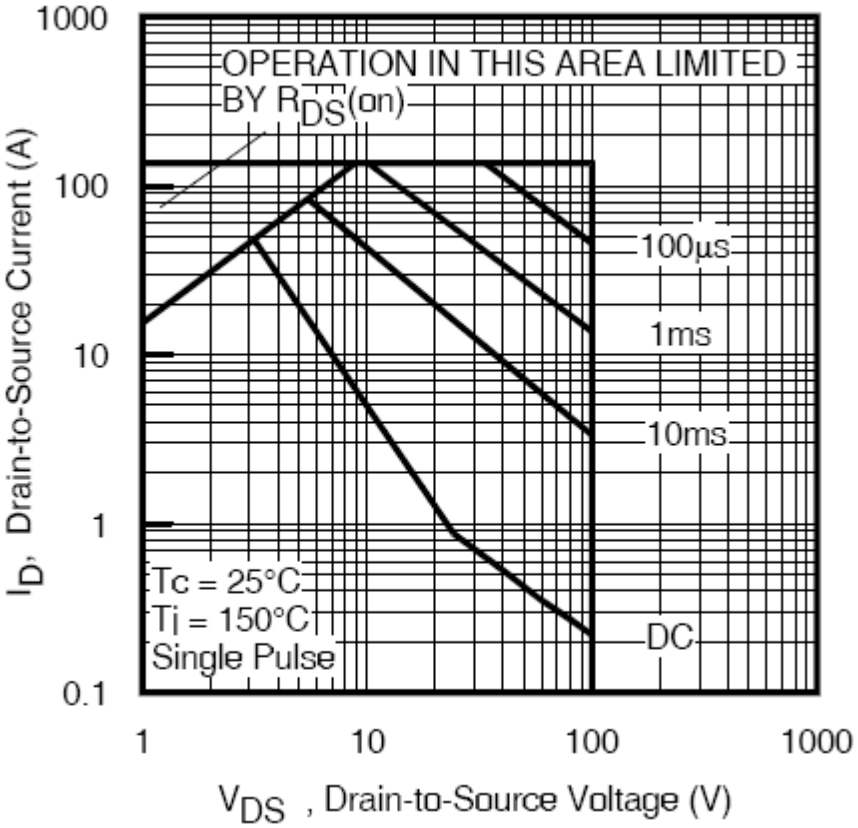


FIGURE 8. Safe-operating-area graphs – Continued.

2N7269

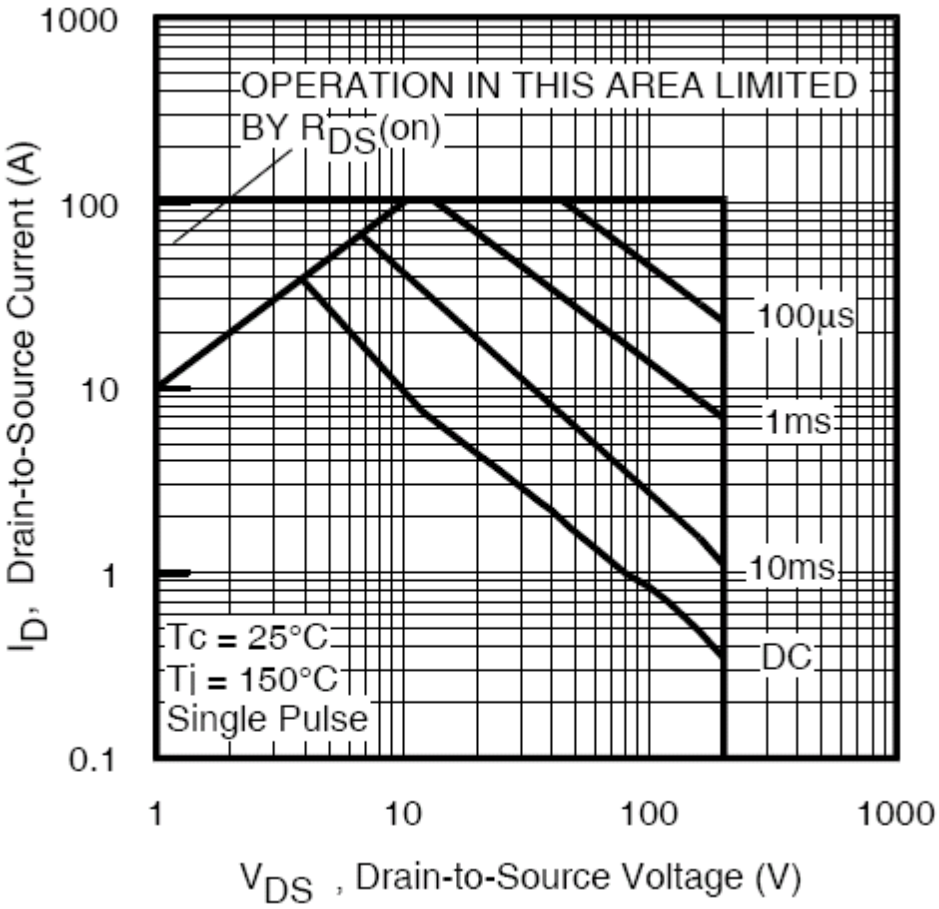


FIGURE 9. Safe-operating-area graphs.

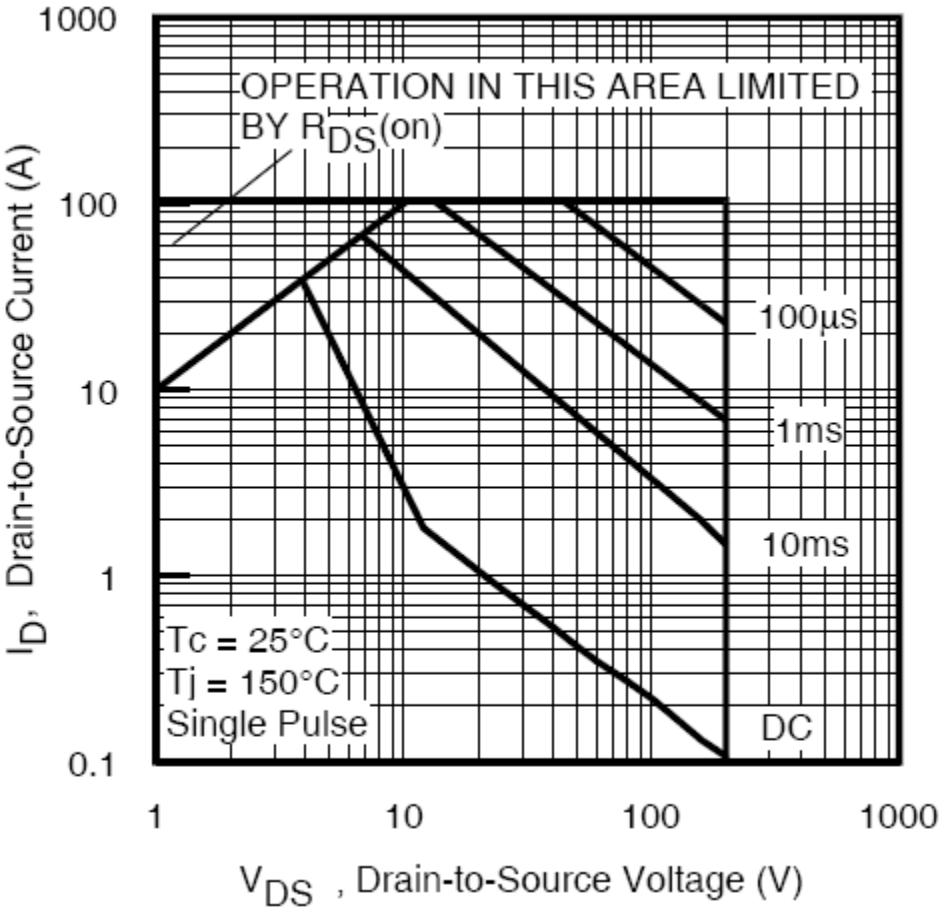


FIGURE 9. Safe-operating-area graphs – Continued.

2N7270

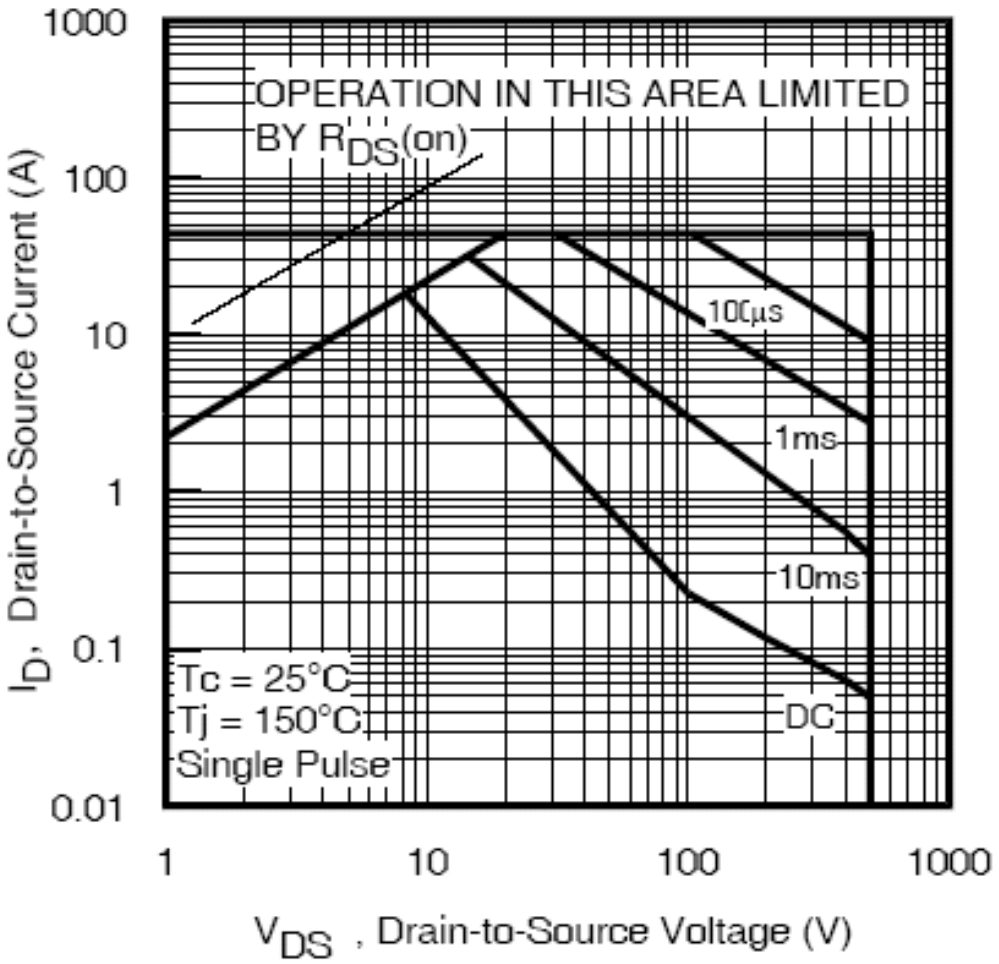


FIGURE 10. Safe-operating-area graphs.

2N7270U, 2N7270U1L, 2N7270U1S

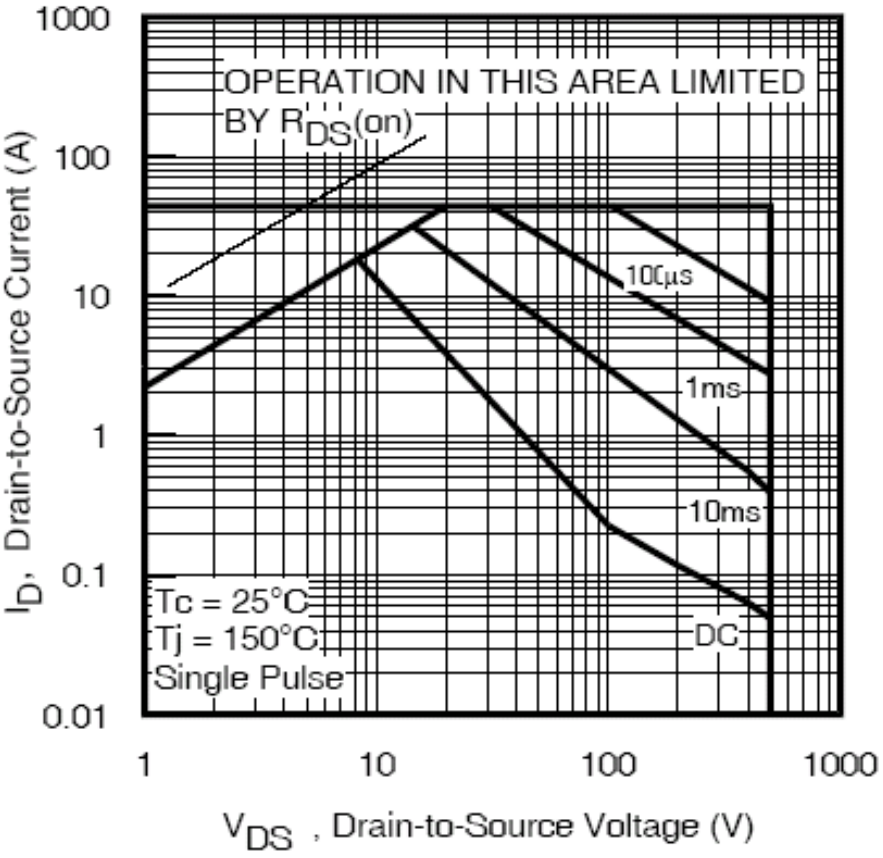


FIGURE 10. Safe-operating-area graphs – Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.6.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

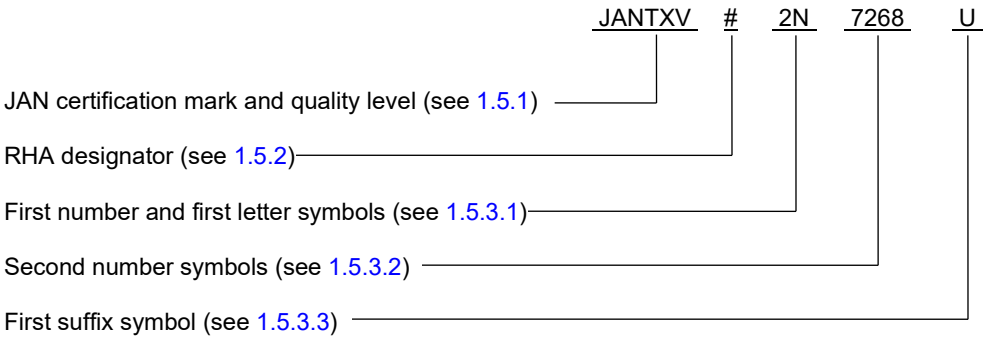
* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's PIN. This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types	Commercial types (1)	
	TO254-AA	"U"
2N7394 2N7268 2N7269 2N7270	IRHM7054 IRHM7150 IRHM7250 IRHM7450	IRHN7054 IRHN7150 IRHN7250 IRHN7450

(1) IRH 7: 100k RAD (Si)
IRH 3: 300k RAD (Si)
IRH 4: 600k RAD (Si)
IRH 8: 1,000k RAD (Si)

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7268	JANTXV#2N7268	JANS2N7268	JANS#2N7268
JANTXV2N7268U	JANTXV#2N7268U	JANS2N7268U	JANS#2N7268U
JANTXV2N7268U1L	JANTXV#2N7268U1L	JANS2N7268U1L	JANS#2N7268U1L
JANTXV2N7268U1S	JANTXV#2N7268U1S	JANS2N7268U1S	JANS#2N7268U1S
JANTXV2N7269	JANTXV#2N7269	JANS2N7269	JANS#2N7269
JANTXV2N7269U	JANTXV#2N7269U	JANS2N7269U	JANS#2N7269U
JANTXV2N7269U1L	JANTXV#2N7269U1L	JANS2N7269U1L	JANS#2N7269U1L
JANTXV2N7269U1S	JANTXV#2N7269U1S	JANS2N7269U1S	JANS#2N7269U1S
JANTXV2N7270	JANTXV#2N7270	JANS2N7270	JANS#2N7270
JANTXV2N7270U	JANTXV#2N7270U	JANS2N7270U	JANS#2N7270U
JANTXV2N7270U1L	JANTXV#2N7270U1L	JANS2N7270U1L	JANS#2N7270U1L
JANTXV2N7270U1S	JANTXV#2N7270U1S	JANS2N7270U1S	JANS#2N7270U1S
JANTXV2N7394	JANTXV#2N7394	JANS2N7394	JANS#2N7394
JANTXV2N7394U	JANTXV#2N7394U	JANS2N7394U	JANS#2N7394U
JANTXV2N7394U1L	JANTXV#2N7394U1L	JANS2N7394U1L	JANS#2N7394U1L
JANTXV2N7394U1S	JANTXV#2N7394U1S	JANS2N7394U1S	JANS#2N7394U1S

(1) The pound symbol (#) represents the RHA level of “R”, “F”, “G”, or “H”. The PIN is also available without a RHA designator.

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/657.

* 6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil.

6.9 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Navy - AS
Air Force - 19, 70, 170

Preparing activity:
DLA - CC

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.