

The documentation and process conversion measures necessary to comply with this document shall be completed by 24 September 2024.

INCH-POUND

MIL-PRF-19500/595L
w/AMENDMENT 1
24 April 2024
SUPERSEDING
MIL-PRF-19500/595L
30 January 2019

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, REPETITIVE AVALANCHE, FIELD EFFECT,
P-CHANNEL, SILICON, TYPES 2N7236, AND 2N7237,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device, and two levels of product assurance (JANHC and JANKC) for each unencapsulated device, with avalanche energy ratings (E_{AS} and E_{AR}) and maximum avalanche current (I_{AR}).

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with [figure 1](#), TO-267AB in accordance with [figure 2](#) for all encapsulated device types. See [figures 3](#) and [4](#) for unencapsulated devices.

1.3 Maximum ratings ($T_C = +25^\circ\text{C}$, unless otherwise specified).

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = -1.0$ mA dc	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>
2N7236, 2N7236U	125	4.0	1.0	-100	± 20	-18	-11	-18	-72	-55 to +150
2N7237, 2N7237U	125	4.0	1.0	-200	± 20	-11	-7	-11	-44	-55 to +150

See notes next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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FSC 5961



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1.3 Maximum ratings - continued.

Type	I _{AR}	E _{AS}	E _{AR}	r _{DS(on)} max (6) V _{GS} = -10 V dc I _D = I _{D2}	
				T _J = +25°C	T _J = +150°C
	<u>A</u>	<u>mJ</u>	<u>mJ</u>	<u>ohm</u>	<u>ohm</u>
2N7236, 2N7236U	-18	500	12.5	0.20	0.400
2N7237, 2N7237U	-11	500	12.5	0.51	1.122

- (1) Derate linearly 1.0 W/°C for T_C > +25°C.
(2) See [figure 5](#), thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

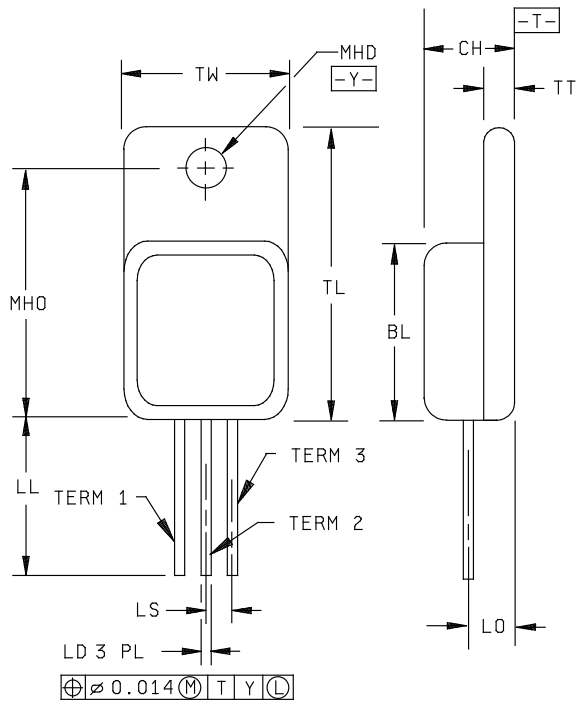
- (4) See [figure 6](#), maximum drain current graphs.
(5) I_{DM} = 4 X I_{D1} as calculated in footnote (3).
(6) Pulsed (see [4.5.1](#)).

1.4 Primary electrical characteristics. T_C = +25°C (unless otherwise specified).

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = -1.0 mA dc	V _{GS(th)1} V _{DS} ≥ V _{GS} I _D = -0.25 mA dc		Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(on)1} (1) I _D = I _{D2} V _{GS} = 10 V
	<u>V dc</u>	<u>V dc</u>		<u>μA dc</u>	<u>Ohms</u>
		<u>Min</u>	<u>Max</u>		
2N7236, 2N7236U	-100	-2.0	-4.0	-25	0.20
2N7237, 2N7237U	-200	-2.0	-4.0	-25	0.51

- (1) Pulsed (see [4.5.1](#)).

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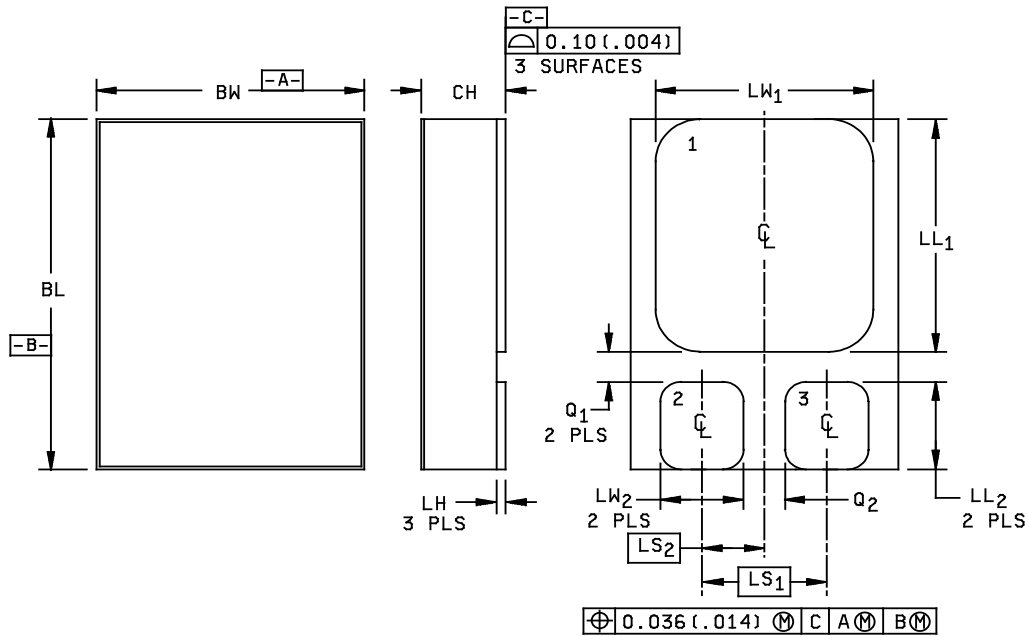
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	4
TW	.535	.545	13.59	13.84	
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.

* FIGURE 1. Physical dimensions for TO-254AA (2N7236 and 2N7237).

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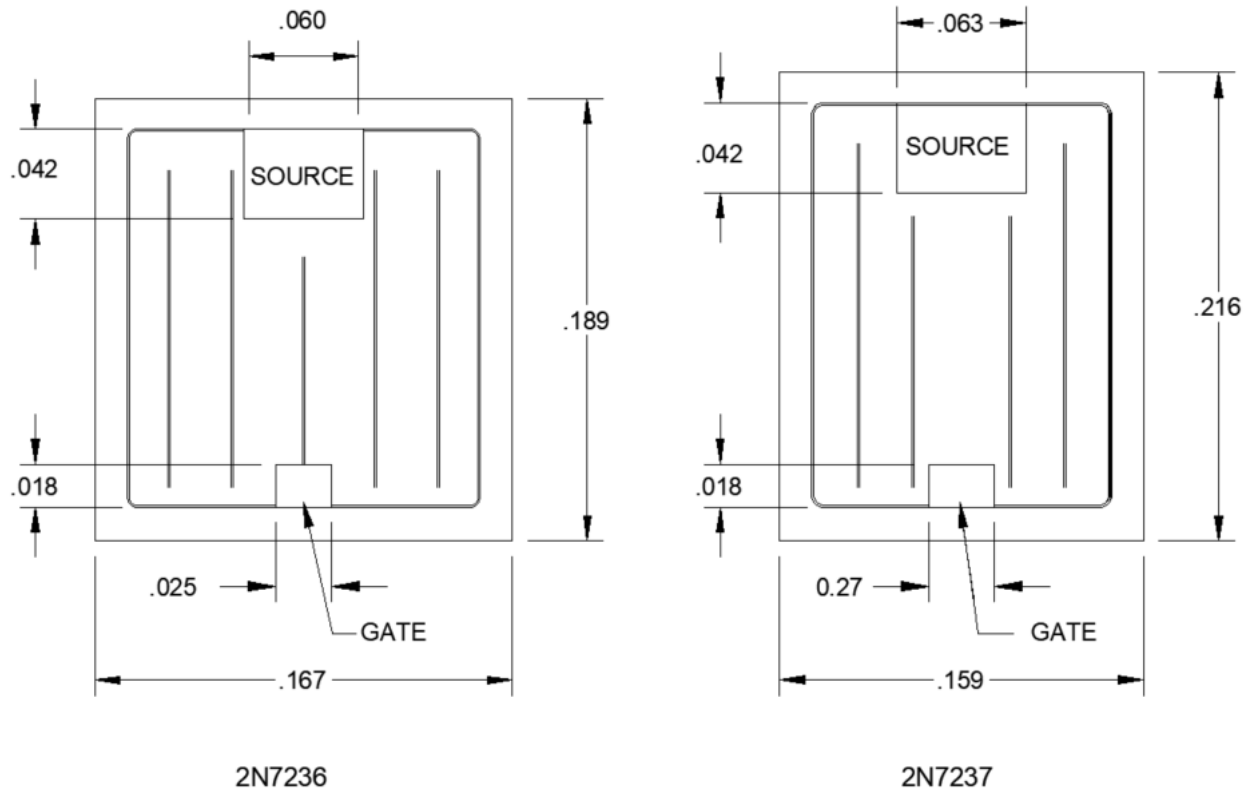
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.620	.630	15.75	16.00
BW	.445	.455	11.30	11.56
CH		.142		3.60
LH	.010	.020	0.26	0.50
LL ₁	.410	.420	10.41	10.67
LL ₂	.152	.162	3.86	4.11
LS ₁	.210 BSC		5.33 BSC	
LS ₂	.105 BSC		2.67 BSC	
LW ₁	.370	.380	9.40	9.65
LW ₂	.135	.145	3.43	3.68
Q ₁	.030		0.76	
Q ₂	.035		0.89	
Term 1	Drain			
Term 2	Gate			
Term 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* FIGURE 2. Dimensions and configuration of surface mount package outline (TO-276AB), 2N7236U and 2N7237U).

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A version

Inches	mm
.018	0.46
.025	0.64
.027	0.69
.042	1.07
.060	1.52
.063	1.60
.159	4.04
.167	4.24
.189	4.80
.216	5.49

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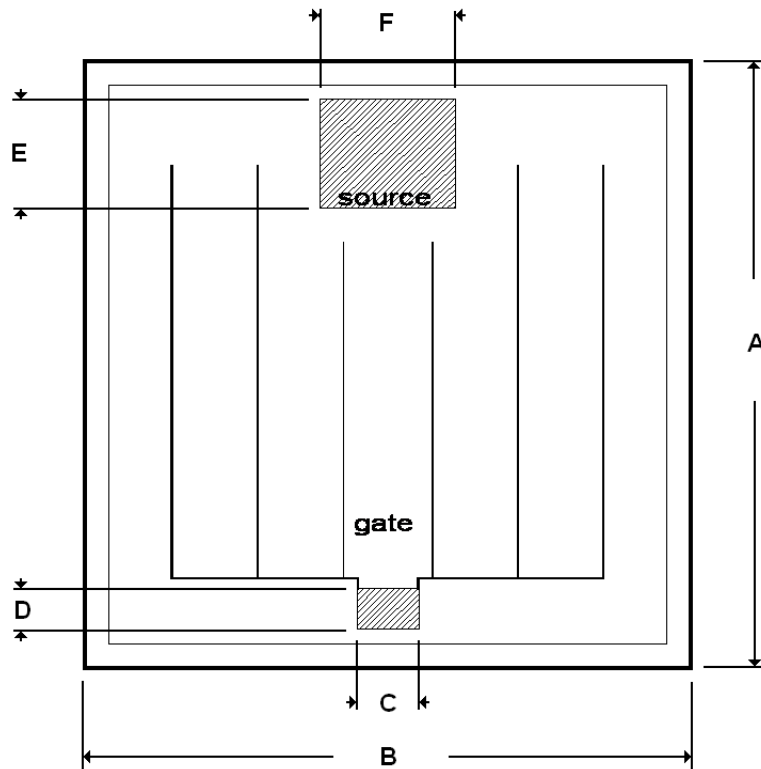
NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Unless otherwise specified, tolerance is ± 0.005 inch (0.13 mm).
4. Physical characteristics of the die thickness = .0187 inch (0.47 mm).
5. Back metal: Cr - Ni - Ag.
6. Top metal: Al.
7. Back contact: Drain.

* FIGURE 3. Physical dimensions JANHCA and JANKCA die.

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2N7236



Ltr	Dimensions - 2N7236			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.177	.183	4.50	4.65
B	.177	.183	4.50	4.65
C	.030	.034	.76	.86
D	.017	.022	.43	.56
E	.034	.038	.86	.97
F	.047	.051	1.19	1.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± 0.005 inch (0.13 mm).
4. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and the back contact is the drain. The top metal is aluminum.
5. Die thickness is .015 inch (0.38 mm) ± 0.001 inch (0.025 mm).

FIGURE 4. JANHCB and JANKCB (B-version) die dimensions for 2N7236 only.

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1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.5](#) for PIN construction example and [6.6](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7236" and "7237".

1.5.3.3 Suffix letter. No suffix letter is used on devices package in the TO-254AA package of [figure 1](#). The suffix letter "U" is used on devices that are packaged in the TO-276AB package of [figure 2](#).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A" and "B" (see [figures 3 and 4 and 6.5](#)).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

nC nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on figures 1 (TO-254AA), 2 (TO-267AB, surface mount), and 3 and 4 (die) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead formation or finish is desired, it shall be specified in the acquisition document (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of table E-IV of [MIL-PRF-19500](#) and 100 percent dc testing in accordance with [table I](#), subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction is not permitted.

3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source. $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Marking. Marking shall be in accordance with [MIL-PRF-19500](#), except at the option of the manufacturer, the country of origin and/or the manufacturers identification may be omitted from the body of the transistor.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for qualification inspection in accordance with of MIL-PRF-19500.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

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4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS level	JANTX and JANTXV level
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2)
(3)	Method 3470 of MIL-STD-750. (see 4.3.3)	Method 3470 of MIL-STD-750. (see 4.3.3)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = -20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 25 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$	Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A or $T_A = +175^\circ\text{C}$ and $t = 48$ hours
13	Subgroup 2 and 3 of table I herein. $\Delta I_{GSSF1} = +20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = -20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 25 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(on)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(th)1} = \pm 20 \text{ percent of initial value.}$	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = +20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = -20 \text{ nA dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 25 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(on)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(th)1} = \pm 20 \text{ percent of initial value.}$
17	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	For TO-254AA packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV do not need to be repeated in screening requirements.

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4.3.1 Screening (JANHC and JANKC). Screening of die shall be in accordance with appendix G of MIL-PRF-19500. As a minimum, die shall be 100 percent probed in accordance with table I, subgroup 2, except test current shall not exceed 20 A.

4.3.2 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

4.3.3 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_D) $I_{AR}(\text{max})$.
- b. Peak gate voltage (V_{GS}).....-10 V.
- c. Gate to source resistor (R_{GS}) $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature +25°C +10°C, -5°C.
- e. Inductance $\left[\frac{2E_{AS}}{(I_{DI})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}).....25 V for 2N7236, 2N7236U, -50 V for 2N7237, 2N7237U.

4.3.4 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). See table II, group E, subgroup 4 herein.

4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage.....900 V dc.
- b. Duration of application of test voltage.....15 seconds (min).
- c. Points of application of test voltage.....All leads to case (bunch connection).
- d. Method of connection.....Mechanical.
- e. Kilovolt-ampere rating of high voltage source.....1,200 V/1.0 mA (min).
- f. Maximum leakage current.....1.0 mA.
- g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and as follows.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G.
B3	2037	Test condition D. All internal wires for each device shall be pulled separately. If group B3 is to be continued to C6, strength test may be performed after C6.
B4	1042	Test condition D. The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted during the "on" cycle.
* B5	1042	A separate sample may be pulled for each test. Accelerated steady-state reverse bias; test condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours, or T_A = +150°C, t = 240 hours, read and record $V_{BR(DSS)}$ (pre and post) at I_D = -1 mA dc. Read and record I_{DSS} (pre and post) in accordance with table I , subgroup 2 herein. $V_{BR(DSS)}$ delta cannot exceed 10 percent.
B5	2037	Bond strength; test condition D.
B6		Not applicable.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G.
B3	1042	Test condition D. The heating cycle shall be 1 minute minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
* C2	2036	Test condition A; weight = 10 pounds (4.54 kg), t = 10 s (not applicable for surface mount devices).
C5	3161	See 4.3.4 , $R_{\theta JC(max)}$ = 1.0°C/W.
C6	1042	Test condition D. The heating cycle shall be 1 minute minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.4	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source 2N7236, 2N7236U 2N7237, 2N7237U	3407	Bias condition C, $V_{GS} = 0V$, $I_D = 1$ mA dc	$V_{(BR)DSS}$	-100 -200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -.25$ mA	$V_{GS(th)1}$	-2.0	-4.0	V dc
Gate forward current	3411	Bias condition C, $V_{GS} = +20$ V dc, $V_{DS} = 0$ V dc	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	Bias condition C, $V_{GS} = -20$ V dc, $V_{DS} = 0$ V dc	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ V dc, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		-25	μA dc
Static drain to source on-state resistance 2N7236, 2N7236U 2N7237, 2N7237U	3421	$V_{GS} = 10$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)1}$		0.20 0.51	Ω Ω
Static drain to source on-state resistance 2N7236, 2N7236U 2N7237, 2N7237U	3421	$V_{GS} = -10$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D1}$ (see 1.3)	$r_{DS(on)2}$		0.22 0.52	Ω Ω
Forward voltage (source drain diode) 2N7236, 2N7236U 2N7237, 2N7237U	4011	$V_{GS} = 0$ V dc, condition A, $I_D = \text{rated } I_{D1}$	V_{SD}		-5.0 -5.0	V V

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^{\circ}\text{C}$				
Gate reverse current	3411	Bias condition C $V_{GS} = \pm 20 \text{ V dc}$, $V_{DS} = 0 \text{ V dc}$,	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 100 \text{ percent of rated } V_{DS}$	I_{DSS2}		-1.0	mA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS3}		-0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -0.25 \text{ mA}$	$V_{GS(th)2}$	-1.0		V dc
Static drain to source on-state resistance	3421	$V_{GS} = -10 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)3}$			
2N7236, 2N7236U					0.34	Ω
2N7237, 2N7237U					1.10	Ω
Low temperature operation:		$T_C = T_J = -55^{\circ}\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -0.25 \text{ mA}$	$V_{GS(th)3}$		-5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$ (see 1.3), $V_{GS} = -10 \text{ V dc}$, gate drive impedance = 9.1Ω , $V_{DD} = 50 \text{ percent of } V_{BR(DSS)}$				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		85	ns
Turn-off delay time			$t_{d(off)}$		85	ns
Fall time			t_f		65	ns

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 7 ; $t_p = 10 \text{ ms}$, $V_{DS} = 80$ percent of rated $V_{BR(DSS)}$, $V_{DS} =$ 200 V maximum				
Electrical measurements		See table I , subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge 2N7236, 2N7236U 2N7237, 2N7237U			$Q_{g(on)}$		60 60	nC nC
Gate to source charge 2N7236, 2N7236U 2N7237, 2N7237U			Q_{gs}		13 15	nC nC
Gate to drain charge 2N7236, 2N7236U 2N7237, 2N7237U			Q_{gd}		35.2 38	nC nC
Reverse recovery time 2N7236, 2N7236U 2N7237, 2N7237U	3473	$d_i/d_t \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 30 \text{ V}$, $I_D = I_{D1}$, (see 1.3), condition A	t_{rr}		280 440	ns ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	500 cycles, test condition G	
Hermetic seal	1071	As applicable	
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

See footnote at end of table.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
<u>Subgroup 11</u> Repetitive avalanche energy Electrical measurements	3469	Peak current $I_{AR} = I_D$; peak gate voltage $V_{GS} = -10$ V; gate to source resistor, $R_{GS} 25 \leq R_{GS} \leq 200$ ohms; temperature = $T_J = +150^\circ\text{C} +0, -10^\circ\text{C}$. Inductance = $\left[\frac{2E_{AR}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right] \text{ mH minimum}$ Number of pulses to be applied = 3.6×10^8 ; supply voltage (V_{DD}) = -25 V for 2N7236 and 2N7236U, (V_{DD}) = -50 V for 2N7237 and 2N7237U, time in avalanche = 2 μs min., 20 μs max., frequency = 500 Hz minimum. See table I , subgroup 2	5 devices c = 0

1/ A separate sample for each test may be pulled.

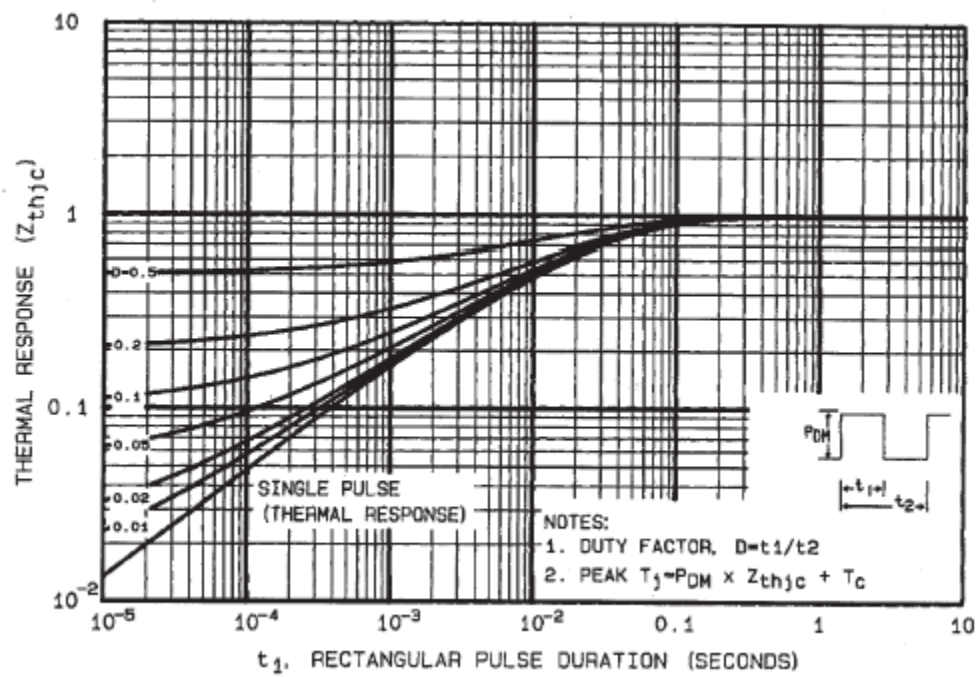


FIGURE 5. Thermal impedance curves.

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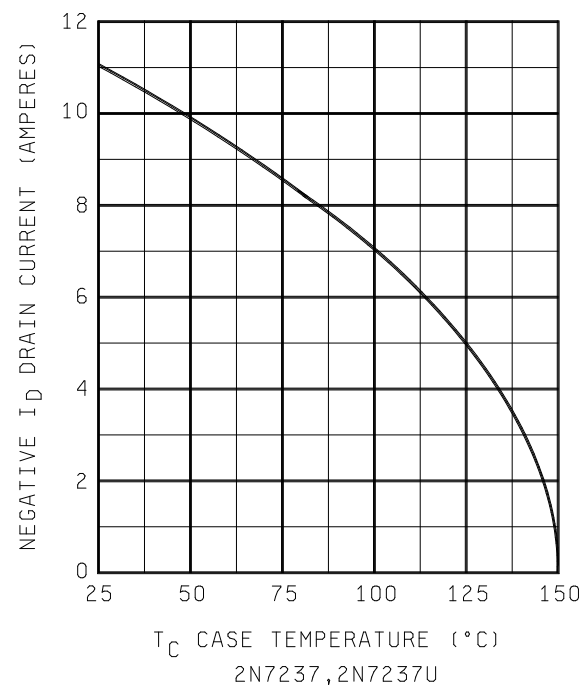
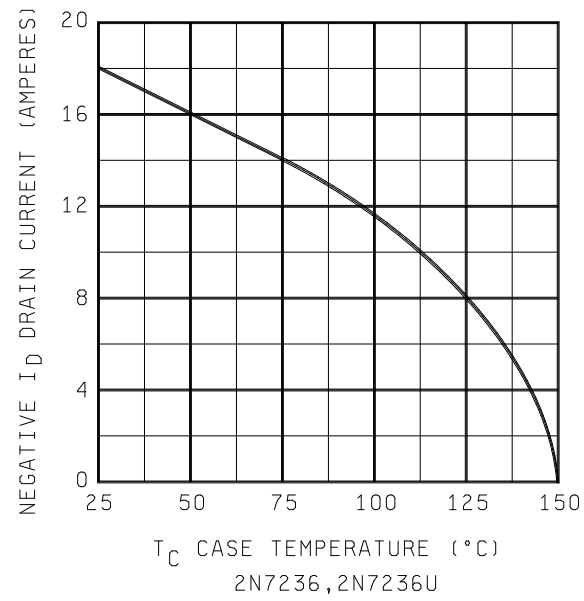
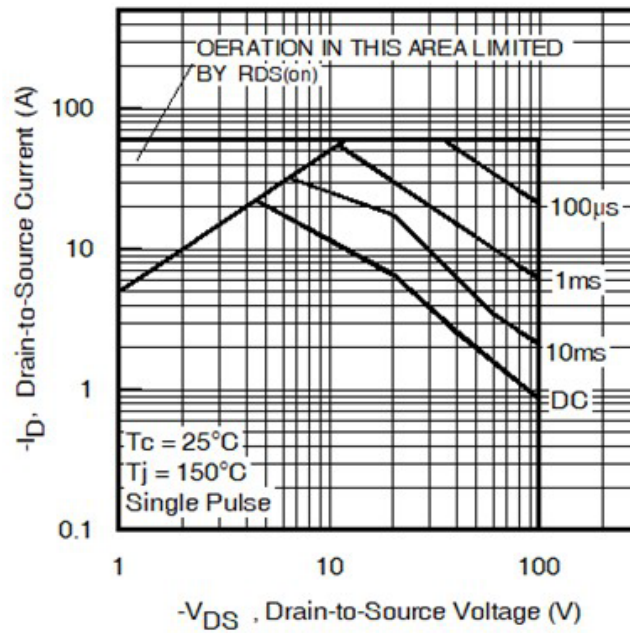
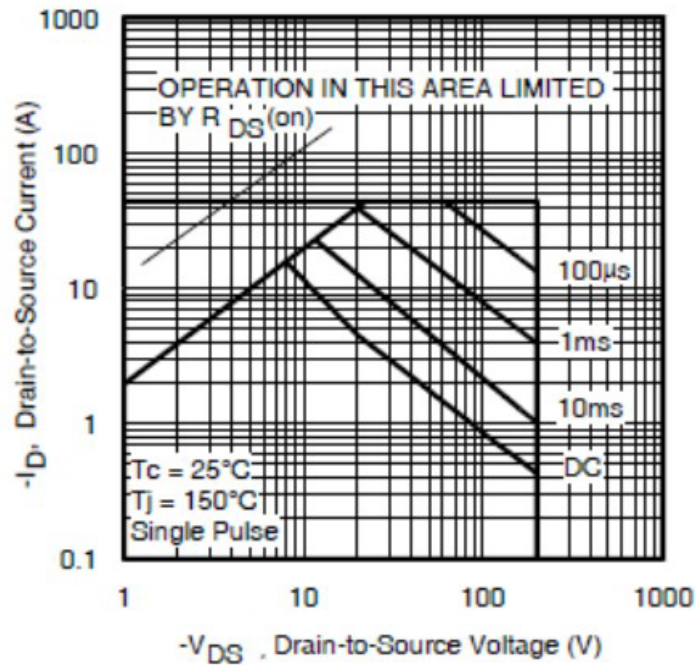


FIGURE 6. Maximum drain current versus case temperature graphs.



2N7236, 2N7236U



2N7237, 2N7237U

* FIGURE 7. Safe operating area graphs.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. Type designation and product assurance level and for die acquisition, specify the JANHC or JANKC letter version (see figure 3, 4, and 6.5).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QPDSIS-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

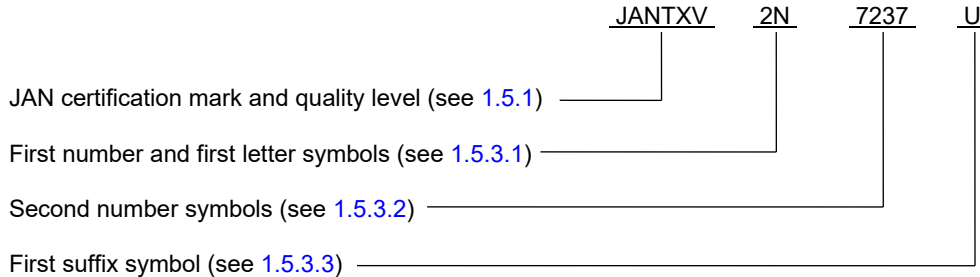
* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable as a substitute for the military PIN.

Military PIN	Manufacturer's CAGE		Manufacturer's and user's PIN
2N7236	43611	69210	IRFM9140
2N7237		69210	IRFM9240
2N7236U	43611	69210	IRFN9140
2N7237U		69210	IRFN9240

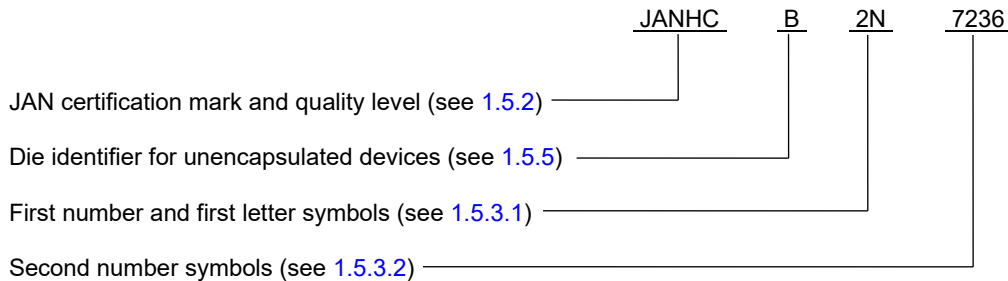
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6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N7236	JANTX2N7236	JANTXV2N7236	JANS2N7236
JAN2N7237	JANTX2N7237	JANTXV2N7237	JANS2N7237
JAN2N7236U	JANTX2N7236U	JANTXV2N7236U	JANS2N7236U
JAN2N7237U	JANTX2N7237U	JANTXV2N7237U	JANS2N7237U

6.6.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (example JANHCA2N7236) will be identified on the QML.

JANC ordering information		
Military PIN	Manufacturer	
	59993	43611
2N7236	JANHCA2N7236 JANKCA2N7236	JANHCB2N7236 JANKCB2N7236
2N7237	JANHCA2N7237 JANKCA2N7237	

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6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

* 6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2024-017)

Review activities:

Army - MI, SM
Navy - AS, MC
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.