

The documentation and process conversion measures necessary to comply with this revision shall be completed by 15 August 2023.

INCH-POUND

MIL-PRF-19500/566D
w/AMENDMENT 1
15 June 2023
SUPERSEDING
MIL-PRF-19500/566D
18 January 2018

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, N-CHANNEL, SILICON, LOGIC LEVEL,
TYPES 2N6902, AND 2N6904 JAN, JANTX, JANTXV AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for logic level, N-channel, enhancement-mode, MOSFET, power transistor. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Package outlines. The device package outlines are as follows: TO-204AA in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. (Unless otherwise specified, $T_A = +25^\circ\text{C}$).

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T	$R_{\theta JC}$	V_{DS}	V_{DG}	V_{GS}	I_{D1} (2) $T_C = +25^\circ\text{C}$	I_{D2} (2) $T_C = +100^\circ\text{C}$	I_S (2)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>$^\circ\text{C}$</u>
2N6902	75	4	1.67	100	100	± 20	12.0	9.6	12.0	-55
2N6904	75	4	1.67	200	200	± 20	8.0	5.1	8.0	to +150

(1) Derate linearly, 0.6 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.

(2) Derate above $T_C = +25^\circ\text{C}$ according to the formula $I_D = \sqrt{\frac{P(\text{rated})}{K}}$ where $P(\text{rated}) = P_T - (T_C - 25) \text{ (W/}^\circ\text{C) watts}$;

$K = \text{Max } r_{DS(\text{on})} \text{ at } T_J = +150^\circ\text{max} - T_C^\circ\text{C}$.

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MIL-PRF-19500/566D
w/AMENDMENT 1

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	I_{DM}	Min $V_{(BR)DSS} V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA dc}$	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0 \text{ mA}$		Max I_{DSS1} $V_{GS} = 0 \text{ V}$		Max $r_{DS(on)} (1)$ $V_{GS} = 5 \text{ V dc}$	
					$V_{DS} = 80 \text{ V}$	$V_{DS} = 160 \text{ V}$	$T_J = +25^\circ\text{C}$ at I_{D1}	$T_J = +150^\circ\text{C}$ at I_{D2}
	<u>A (pk)</u>	<u>V dc</u>	<u>V dc</u> Min	<u>V dc</u> Max	<u>$\mu\text{A dc}$</u>	<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>
2N6902	30	100	1.0	2.0	1.0		0.2	0.52
2N6904	20	200	1.0	2.0		1.0	0.6	1.17

(1) Pulsed (see 4.5.1)

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6902" and "6904".

1.5.3 Suffix symbols. No suffix symbols are used on devices packaged in the TO-204AA package of [figure 1](#).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

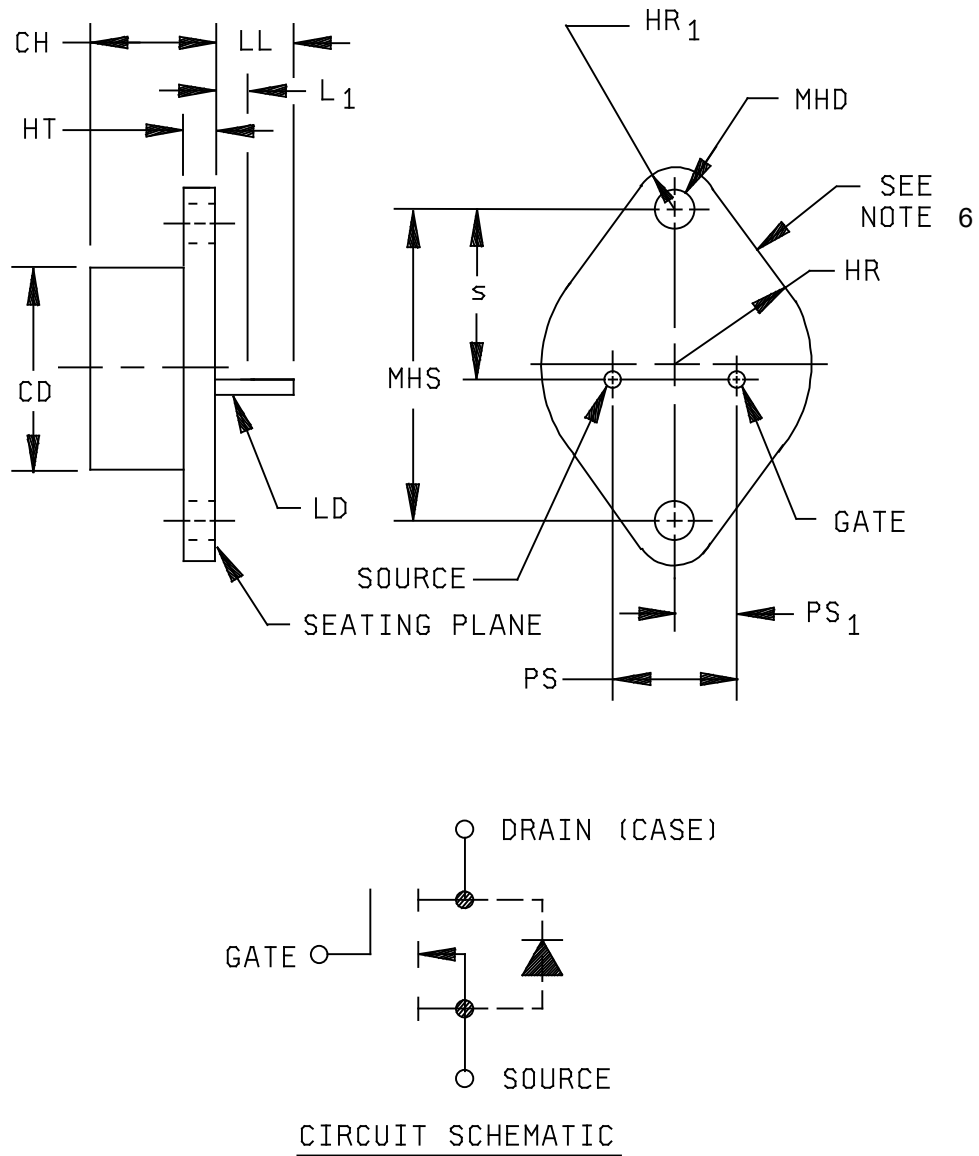


FIGURE 1. Physical dimensions of transistor type TO-204AA.

MIL-PRF-19500/566D
w/AMENDMENT 1

Dimensions					
Ltr	Inches	Inches	mm	mm	Notes
	Min	Max	Min	Max	
CD		.875		22.23	
CH	.250	.360	6.35	9.15	3
HR	.495	.525	12.57	13.3	
HR ₁	.131	.188	3.33	4.78	
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.10	
LL	.312	.500	7.92	12.70	
L ₁		.050		1.27	
MHD	.151	.161	3.84	4.09	
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	3
PS ₁	.205	.225	5.21	5.72	3
s	.655	.675	16.64	17.15	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions shall be measured at points .050 inch (1.27 mm) and .055 inch (1.40 mm) below the seating plane. When gauge is not used, measurement will be made at the seating plane.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. Mounting holes shall be deburred on the seating plane side.
6. Drain is electrically connected to the case.

FIGURE 1. Physical dimensions of transistor type TO-204AA - Continued.

MIL-PRF-19500/566D
w/AMENDMENT 1

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

I_{AS} Rated avalanche current, nonrepetitive
nC nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

MIL-PRF-19500/566D
w/AMENDMENT 1

* 3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static discharge. The following handling practices shall be followed.

- a. Devices shall be handled on benches with conductive and grounded surface.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate shall be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#))
- c. Conformance inspection (see [4.4](#) and [table I](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

MIL-PRF-19500/566D
w/AMENDMENT 1

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTX and JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2) optional	Method 3470 of MIL-STD-750, (see 4.3.2) optional
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein. I_{DSS1} , I_{GSSF1} , I_{GSSR1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 2$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 2$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value $\Delta V_{GS(th)1} = \pm 20$ percent of initial value	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 2$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value $\Delta V_{GS(th)1} = \pm 20$ percent of initial value

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $V_{GS(th)1}$, and $r_{DS(ON)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a. JANTX and JANTXV levels do not need to be repeated in screening requirements.

MIL-PRF-19500/566D
w/AMENDMENT 1

4.3.1 Gate stress test. Apply $V_{GS} = 15 \text{ V}$ minimum for $t = 250 \mu\text{s}$ minimum.

4.3.2 Single pulse unclamped inductive switching.

- a. Peak current, I_D 3.0 A.
- b. Peak gate voltage, V_{GS} 10 V.
- c. Gate to source resistor, R_{GS} $25 \leq R_{GS} \leq 200$.
- d. Initial case temperature+25°C +10, -5°C.
- e. Inductance 100 μH minimum.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage V_{DD} 50 V.

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). See [table II](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#), table E-V and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#), subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX and JANTXV) of [MIL-PRF-19500](#), and as follows.

MIL-PRF-19500/566D
w/AMENDMENT 1

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G
B3	2075	See 3.4.2 .
B4	1042	Test condition D, the heating cycle shall be 1 minute minimum.
B5	1042	Test condition A; V_{DS} = rated V_{DS} (see 1.3), T_A = +175° C, t = 120 hours minimum, read and record $V_{BR(DSS)}$ (pre and post) at I_D = 1 mA, read and record I_{DSS} (pre and post), (see table I).
B5	1042	Test condition B; V_{GS} = rated V_{GS} (see 1.3), T_A = +175° C, t = 24 hours minimum.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B2	1051	Test condition G
B3	1042	Test condition D; The heating cycle shall be 1 minute minimum.
B4	2075	See 3.4.2 .

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A; weight = 10 lbs., t = 15 s.
C5	3161	See 4.3.3 .
C6	1042	Test condition D; The heating cycle shall be 1 minute minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

MIL-PRF-19500/566D
w/AMENDMENT 1

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source 2N6902 2N6904	3407	$V_{GS} = 0$ V dc; $I_D = 1$ mA dc, Bias condition C	$V_{(BR)DSS}$	100 200		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; $I_D = 1.0$ mA dc	$V_{GS(th)1}$	1.0	2.0	V dc
Gate current	3411	$V_{GS} = +10$ V dc; bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -10$ V dc; bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current 2N6902 2N6904	3413	Bias condition C, $V_{GS} = 0$ V dc; $V_{DS} = 80$ V dc $V_{DS} = 160$ V dc	I_{DSS1}		1.0 1.0	μA dc
Static drain to source on-state resistance 2N6902 2N6904	3421	Bias condition A, $V_{GS} = 5$ V dc, pulsed (see 4.5.1), $I_{D2} = 9.6$ A dc $I_{D2} = 5.1$ A dc	$r_{DS(on)1}$		0.2 0.6	Ω
Drain to source "on-state" voltage 2N6902 2N6904	3405	Bias condition A $V_{GS} = 5$ V dc, pulsed (see 4.5.1), $I_D = 12.0$ A dc $I_D = 8.0$ A dc	$V_{DS(on)}$		3.3 5.5	V dc
Forward voltage (source-drain diode) 2N6902 2N6904	4011	Condition A, $V_{GS} = 0$ V $I_S = 12.0$ A dc $I_S = 8.0$ A dc	V_{SD}	0.8	1.6	V dc
Forward transconductance 2N6902 2N6904	3475	$I_D = \text{Rated } I_{D2}$ (see 1.3) Pulsed (see 4.5.1)	g_{FS}	3 3	12 12	S

See footnote at end of table.

MIL-PRF-19500/566D
w/AMENDMENT 1

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = 125^{\circ}\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}; I_D = 1.0 \text{ mA dc}$	$V_{GS(th)2}$	0.5		V dc
Gate current	3411	Bias condition C; $V_{GS} = +10 \text{ and } -10 \text{ V dc}$ $V_{DS} = 0 \text{ V dc}$	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C; $V_{GS} = 0 \text{ V dc}$	I_{DSS2}		50	$\mu\text{A dc}$
2N6902 2N6904		$V_{DS} = 80 \text{ V dc}$ $V_{DS} = 100 \text{ V dc}$				
Static drain to source on-state resistance	3421	Bias condition A, $V_{GS} = 5 \text{ V dc}$ pulsed (see 4.5.1)	$r_{DS(on)2}$			Ω
2N6902 2N6904		$I_{D2} = 9.6 \text{ A dc}$ $I_{D2} = 5.1 \text{ A dc}$			0.32 1.11	
Low temperature operation:		$T_C = T_J = -55^{\circ}\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}; I_D = 1.0 \text{ mA dc}$	$V_{GS(th)3}$		3.0	V dc
<u>Subgroup 4</u>						
Switching time	3472	$I_D = \text{rated } I_{D2} \text{ (see 1.3)}$ $V_{GS} = 5 \text{ V dc}$ Gate drive impedance = 7.5 Ω				
Turn-on delay time 2N6902 2N6904		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$	$t_{d(on)}$		50 45	ns
Rise time 2N6902 2N6904		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$	t_r		150 150	ns
Turn-off delay time 2N6902 2N6904		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$	$t_{d(off)}$		130 135	ns
Fall time 2N6902 2N6904		$V_{DD} = 50 \text{ V dc}$ $V_{DD} = 100 \text{ V dc}$	t_f		150 105	ns

See footnote at end of table.

MIL-PRF-19500/566D
w/AMENDMENT 1
TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area	3474	See figure 2 , $V_{DS} = 80$ percent of rated V_{DS} and $V_{DS} \leq 200$ V max				
High voltage test		$t_p = 1$ s				
2N6902 2N6904						
Electrical measurements		See table I, subgroup 2 herein				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition A or B	$Q_{g(on)}$			nC
On-state gate charge						
2N6902 2N6904				9 7	19 17	
Gate to source charge			Q_{gs}			nC
2N6902 2N6904				1.1 1.4	5.0 5.0	
Gate to source charge			Q_{gd}			nC
2N6902 2N6904				5 3	16 14	
Reverse recovery time	3473	Condition A, $di/dt = 100$ A/ μ s $V_{DD} \leq 30$ V dc, $I_F = 4$ A	t_{rr}			ns
2N6902 2N6904					375 625	

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3, 4, and 5 (JANS).
Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

MIL-PRF-19500/566D
w/AMENDMENT 1

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection <u>1/</u>
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 ^{1/}</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 10</u>			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	22 devices c = 0

1/ A separate sample for each test may be pulled.

2N6902

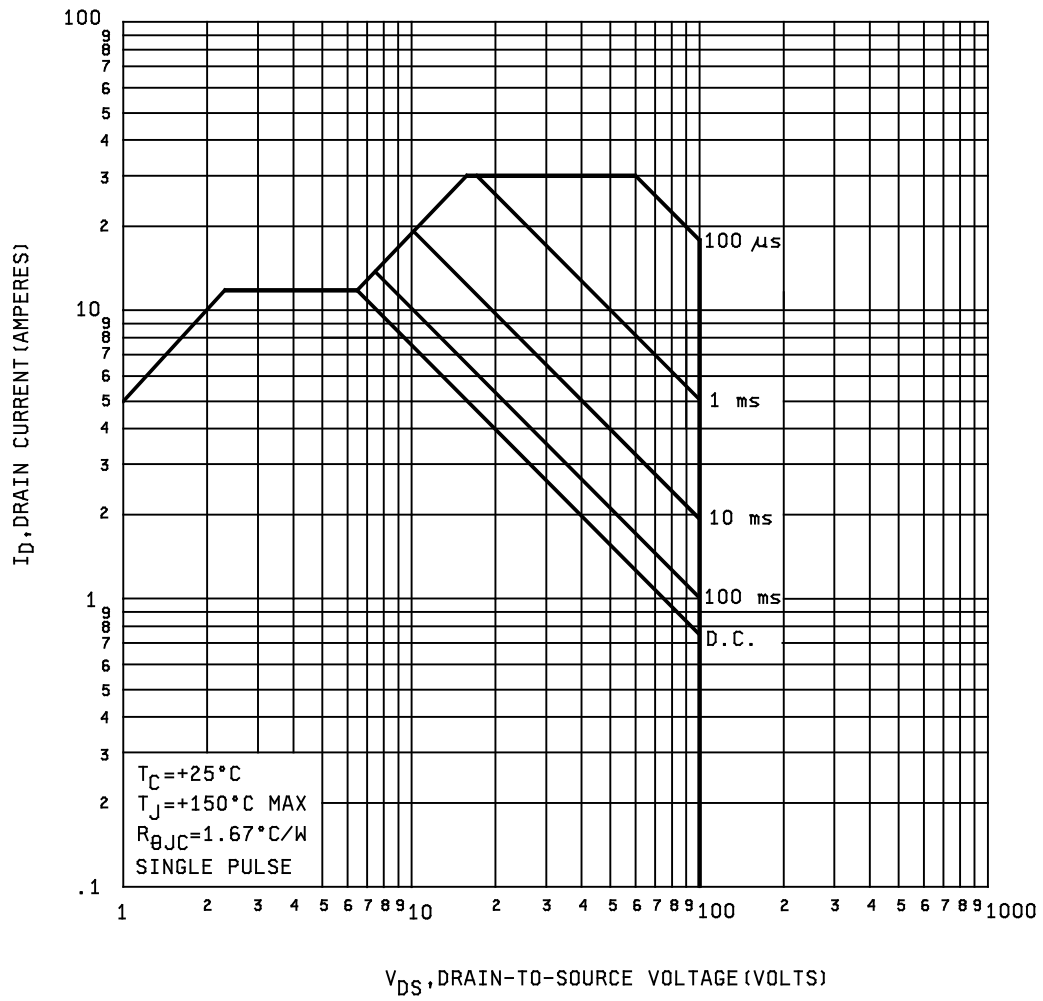


FIGURE 2. Safe operating area graph.

2N6904

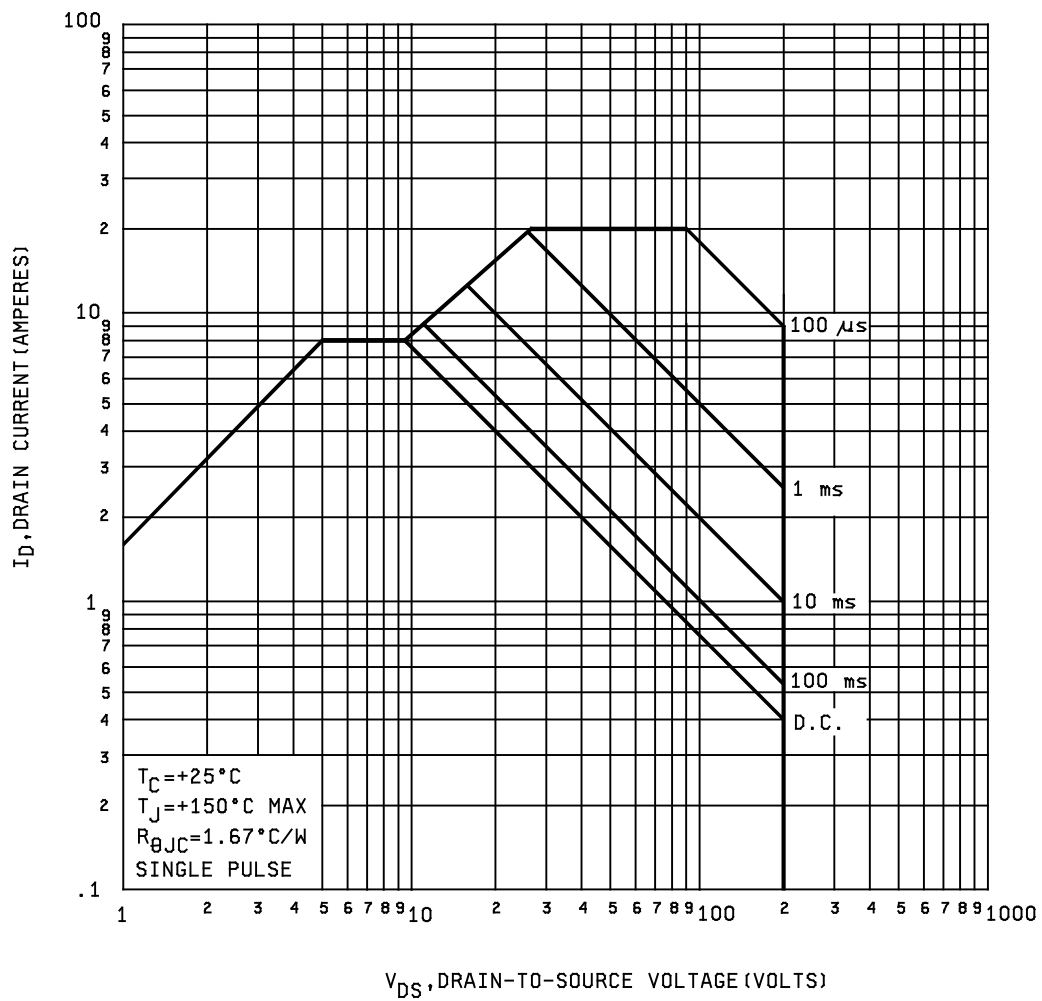


FIGURE 2. Maximum safe operating area graph - Continued.

MIL-PRF-19500/566D
w/AMENDMENT 1

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

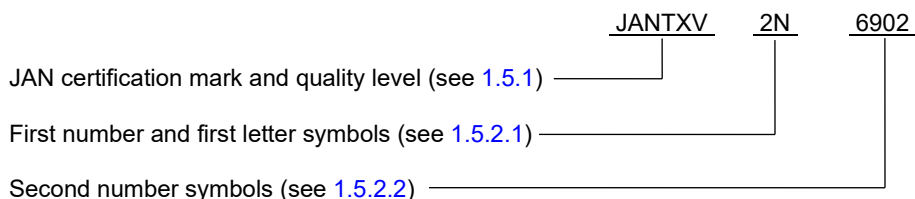
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QPDSIS-19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



MIL-PRF-19500/566D
w/AMENDMENT 1

6.5 List of PINs.

6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6902	JANTX2N6902	JANTXV2N6902	JANS2N6902
JAN2N6904	JANTX2N6904	JANTXV2N6904	JANS2N6904

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2023-059)

Review activities:

* Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.