

The documentation and process conversion measures necessary to comply with this revision shall be completed by 21 November 2024.

INCH-POUND

MIL-PRF-19500/562F
w/AMENDMENT 1
21 June 2024
SUPERSEDING
MIL-PRF-19500/562F
30 January 2019

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, P-CHANNEL,
SILICON, ENCAPSULATED (THROUGH-HOLE MOUNT PACKAGES)
AND UN-ENCAPSULATED (DIE), TYPES 2N6804 AND 2N6806
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, power transistor intended for use in high density power switching applications. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device and two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device.

1.2 Package outlines. The device package outlines are as follows: TO-204AA (formerly TO-3) in accordance with [figure 1](#) for all encapsulated device types. See [figures 2, 3, and 4](#) for unencapsulated devices.

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>$^\circ\text{C}$</u>
2N6804	75	4	1.67	-100	-100	± 20	-11.0	-7.0	-11.0	-44	-55 to +150
2N6806	75	4	1.67	-200	-200	± 20	-6.5	-4.0	-6.5	-26	-55 to +150

- (1) Derate linearly 0.6 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.
- (2) See [figure 5](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 6](#), maximum drain current graph.
- (5) $I_{DM} = 4 \times I_{D1}$ as calculated in note 3.

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AMSC N/A

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MIL-PRF-19500/562F
w/AMENDMENT 1

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0\text{ V}$ $I_D = -1.0\text{ mA dc}$	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ $I_D = -0.25\text{ mA dc}$		Max I_{DSS1} $V_{GS} = 0\text{ V}$	Max $r_{DS(on)} (1)$ $V_{GS} = -10\text{ V dc}$		$R_{\theta JC}$ maximum
				$V_{DS} = 80$ percent of rated V_{DS}	$T_J = +25^{\circ}\text{C}$ at I_{D2}	$T_J = +150^{\circ}\text{C}$ at I_{D2}	
	<u>V dc</u>	<u>V dc</u>		<u>$\mu\text{A dc}$</u>	<u>ohm</u>	<u>ohm</u>	<u>$^{\circ}\text{C/W}$</u>
		<u>Min</u>	<u>Max</u>				
2N6804	-100	-2.0	-4.0	-25	0.30	0.60	1.67
2N6806	-200	-2.0	-4.0	-25	0.80	1.80	1.67

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANH" and "JANK".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

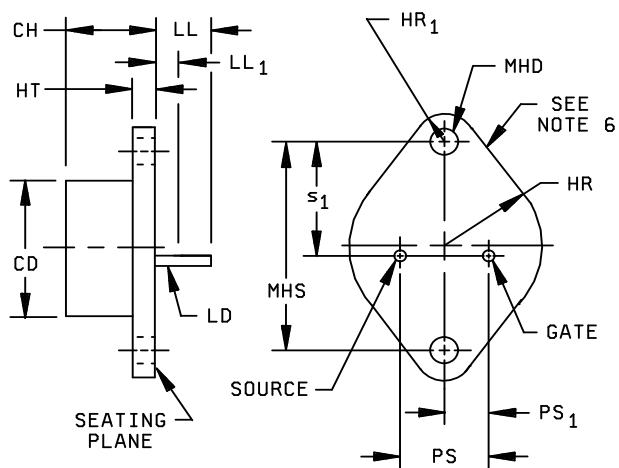
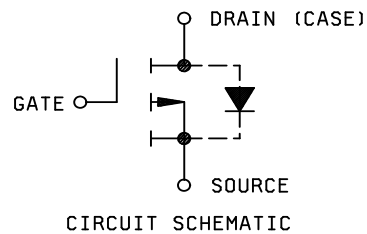
1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6804" and "6806".

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A" (see figures 2 and 3 and 6.6) and "B" (see figure 4 and 6.6).

MIL-PRF-19500/562F
w/AMENDMENT 1

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.250	.360	6.35	9.15	3
LD	.038	.043	0.97	1.10	
CD		.875		22.23	
PS	.420	.440	10.67	11.18	3
PS ₁	.205	.225	5.21	5.72	3
HT	.060	.135	1.52	3.43	
LL	.312	.500	7.92	12.70	
LL ₁		.050		1.27	
MHD	.151	.165	3.84	4.19	
MHS	1.177	1.197	29.90	30.40	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	
s ₁	.655	.675	16.64	17.15	

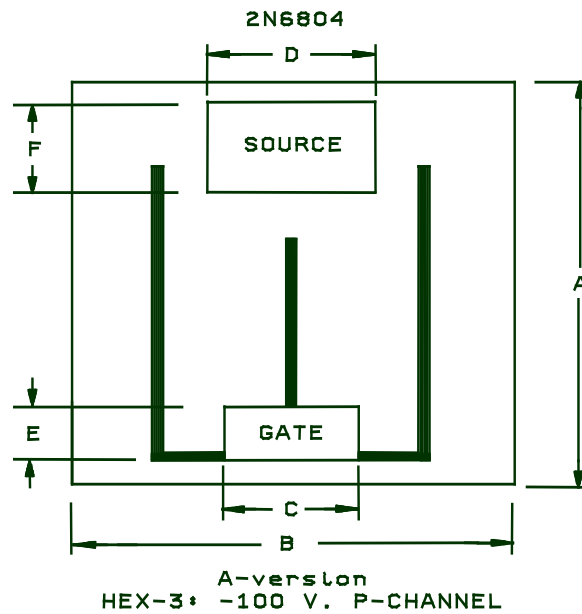


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. Measurement will be made at the seating plane.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. Mounting holes shall be deburred on the seating plane side.
6. Drain is electrically connected to case.

* FIGURE 1. Physical dimensions of transistor (TO-204AA).

MIL-PRF-19500/562F
w/AMENDMENT 1



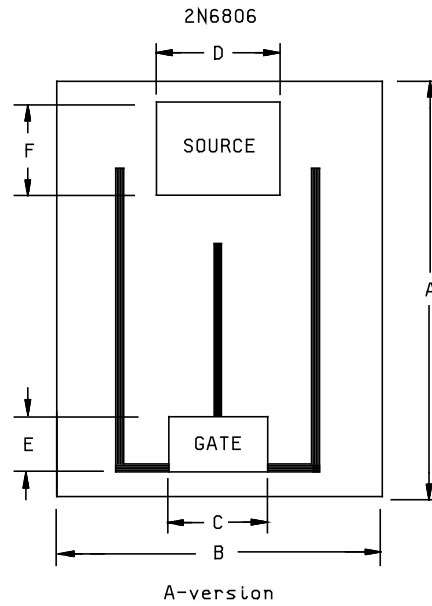
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.170	.185	4.32	4.70
B	.102	.118	2.59	3.00
C	.021	.029	0.53	0.74
D	.035	.043	0.89	1.09
E	.014	.022	0.36	0.56
F	.025	.036	0.64	0.91

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
Back metals are chromium, nickel, and silver.
Top metal is aluminum.
Back contact is the drain.
4. The die thickness is .0187 inch (0.474 mm), the tolerance is ± 0.0050 inch (0.13 mm).
5. Unless otherwise specified, tolerance is ± 0.0005 inch (0.013 mm).

FIGURE 2. JANHCA and JANKCA die dimensions for 2N6804.

MIL-PRF-19500/562F
w/AMENDMENT 1



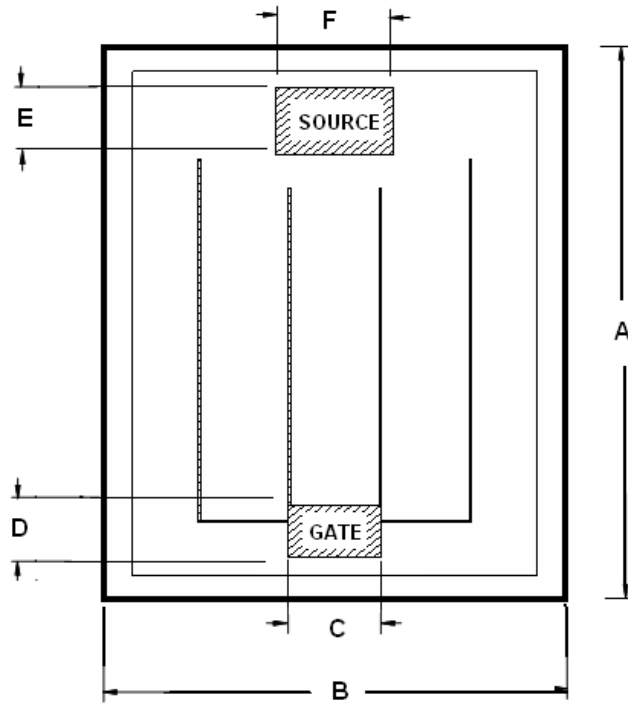
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.170	.186	4.32	4.72
B	.105	.121	2.67	3.07
C	.022	.030	0.56	0.76
D	.030	.038	0.76	0.97
E	.012	.020	0.30	0.51
F	.021	.029	0.53	0.74

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
Back metals are chromium, nickel, and silver.
Top metal is aluminum.
Back contact is the drain.
4. The die thickness is .0187 inch (0.474 mm), the tolerance is $\pm .0050$ inch (0.13 mm).
5. Unless otherwise specified, tolerance is $\pm .0005$ inch (0.013 mm).

FIGURE 3. JANHCA and JANKCA die dimensions for 2N6806.

MIL-PRF-19500/562F
w/AMENDMENT 1



Ltr	Dimensions - 2N6804			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.181	.185	4.60	4.70
B	.116	.120	2.95	3.05
C	.032	.034	.81	.86
D	.017	.019	.43	.48
E	.024	.026	.61	.66
F	.035	.037	.89	.94

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ± 0.005 inch (0.13 mm).
4. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and the back contact is the drain. The top metal is aluminum.
5. Die thickness is .015 inch (0.38 mm) ± 0.001 inch (0.025 mm).

FIGURE 4. JANHCB and JANKCB (B-version) die dimensions for 2N6804.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

nC ----- nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#) (TO-204AA), [2](#), [3](#), and [4](#) (JANHC and JANKC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#) and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Devices shall be marked in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

MIL-PRF-19500/562F
w/AMENDMENT 1

3.7 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and table II herein. Alternate flow is allowed for qualification inspection in accordance with [MIL-PRF-19500](#).

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.2 JANHC and JANKC die. Qualification shall be in accordance with [MIL-PRF-19500](#).

MIL-PRF-19500/562F
w/AMENDMENT 1

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2)
(3) (4)	Method 3470 of MIL-STD-750, (optional) (see 4.3.4)	Method 3470 of MIL-STD-750, (optional) (see 4.3.4)
(3) 3c	Method 3161 of MIL-STD-750, (see 4.3.3)	Method 3161 of MIL-STD-750, (see 4.3.3)
9	Subgroup 2 of table I herein.	Subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein;
12	Method 1042 of MIL-STD-750, test condition A, t = 240 hours	Method 1042 of MIL-STD-750, test condition A; $T_A = +175^\circ\text{C}$ and t = 48 hours
13	Subgroups 2 and 3 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime before screen 9.
- (4) Method 3470 is optional if performed as a sample in group A, subgroup 5.

MIL-PRF-19500/562F
w/AMENDMENT 1

4.3.1 Screening (JANHC and JANKC). Screening of die shall be in accordance with [MIL-PRF-19500](#). As a minimum, die shall be 100-percent probed in accordance with [table I](#), subgroup 2.

4.3.2 Gate stress test. Apply $V_{GS} = \pm 30$ V minimum for $t = 250$ μ s minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). See [table II](#), group E, subgroup 4 herein.

4.3.4 Unclamped inductive switching.

- a. Peak current (I_D) Rated I_{D1} .
- b. Peak gate voltage (V_{GS}) -10 V.
- c. Gate to source resistor (R_{GS}) $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature (T_C) +25°C +10°C, -5°C.
- e. Inductance (L) 100 μ H ± 10 percent.
- f. Number of pulses to be applied 1 pulse minimum.
- g. Pulse repetition rate None.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#). Alternate flow is allowed for quality conformance inspection in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and herein.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B4	1042	Test condition D. The heating cycle shall be 1 minute minimum.
* B5	1042	Accelerated steady-state operation life; test condition A; $V_{DS} = \text{rated}$ $T_A = +175^\circ\text{C}$, $t = 120$ hours or $T_A = 150^\circ\text{C}$, $t = 240$ hours. Read and record $V_{(BR)DSS}$ (pre and post) at $1 \text{ mA} = I_D$. Read and record I_{DSS} (pre and post) in accordance with table I , subgroup 2 herein. Deltas for $V_{(BR)DSS}$ shall not exceed 10 percent and I_{DSS} shall not exceed 25 μ A.
*		Accelerated steady-state gate stress; condition B, $V_{GS} = \text{rated}$, $T_A = +175^\circ\text{C}$, $t = 24$ hours or $T_A = 150^\circ\text{C}$, $t = 48$ hours.
B5	2037	Bond strength; test condition D.

MIL-PRF-19500/562F
w/AMENDMENT 1

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G.
B3	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 10 pounds; t = 15 s.
C5	3161	See 4.3.3 .
C6	1042	Test condition D. The heating cycle shall be 1 minute minimum.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

MIL-PRF-19500/562F
w/AMENDMENT 1

TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	Bias condition C, $V_{GS} = 0$ V; $I_D = -1.0$ mA dc	$V_{(BR)DSS}$			V dc
2N6804 2N6806				-100 -200		
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; $I_D = -0.25$ mA dc	$V_{GS(th)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	Bias condition C; $V_{DS} = 0$ V; $V_{GS} = +20$ and -20 V dc	I_{GSS1}		± 100	nA dc
Drain current	3413	$V_{GS} = 0$; bias condition C; $V_{DS} = 0$ V; $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		-25	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = -10$ V dc; condition A, pulsed (see 4.5.1)	$r_{DS(on)1}$			Ω
2N6804 2N6806		$I_D = -7$ A dc $I_D = -4$ A dc			0.30 0.80	
Drain to source on-state resistance	3421	$V_{GS} = -10$ V dc; condition A, pulsed (see 4.5.1)	$r_{DS(on)2}$			Ω
2N6804 2N6806		$I_D = -11$ A dc $I_D = -6.5$ A dc			0.36 0.94	
Forward voltage (source drain diode)	4011	Condition A, $V_{GS} = 0$ V	V_{SD}			
2N6804 2N6806		For devices with a multiple diode structure $I_S = -11$ A dc $I_S = -6.5$ A dc			-4.7 -6.0	V V

See footnote at end of table.

MIL-PRF-19500/562F
w/AMENDMENT 1

TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 3</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
High temperature operation:		$T_C = T_J = +125^{\circ}\text{C}$				
Gate reverse current	3411	Bias condition C, $V_{DS} = 0\text{ V}$, $V_{GS} = +20\text{ V dc}$ and -20 V dc	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ percent rated } V_{DS}$	I_{DSS2}		-0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; $I_D = -0.25\text{ mA}$	$V_{GS(th)2}$	-1.0		V dc
Static drain to source on-state resistance	3421	$V_{GS} = -10\text{ V dc}$, condition A, pulsed (see 4.5.1)	$r_{DS(on)3}$			Ω
2N6804 2N6806		$I_D = -7\text{ A dc}$ $I_D = -4\text{ A dc}$			0.55 1.60	
Low temperature operation:		$T_C = T_J = -55^{\circ}\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; $I_D = -0.25\text{ mA}$	$V_{GS(th)3}$		-5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D2}$ (see 1.3); $V_{GS} = -10\text{ V dc}$; $R_g = 7.5\text{ ohms}$				
Turn-on delay time			$t_{d(on)}$			ns
* * 2N6804 2N6806		$V_{DD} = -50\text{ V dc}$ $V_{DD} = -100\text{ V dc}$			60 50	
Rise time			t_r			ns
* * 2N6804 2N6806		$V_{DD} = -50\text{ V dc}$ $V_{DD} = -100\text{ V dc}$			140 100	

See footnote at end of table.

MIL-PRF-19500/562F
w/AMENDMENT 1

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> – Continued						
Turn-off delay time			$t_{d(off)}$			ns
* 2N6804		$V_{DD} = -50$ V dc			140	
* 2N6806		$V_{DD} = -100$ V dc			100	
Fall time			t_f			ns
* 2N6804		$V_{DD} = -50$ V dc			140	
* 2N6806		$V_{DD} = -100$ V dc			80	
<u>Subgroup 5</u>						
Single pulse unclamped inductive switching <u>3/</u>	3470	See 4.3.4 , 116 devices, c = 0				
Electrical measurements		See table I , subgroup 2 herein.				
Safe operating area test	3474	$V_{DS} = 80$ percent of rated V_{DS} ; $V_{DS} \leq 200$ V maximum, $t_p = 10$ ms (see figure 7).				
Electrical measurements		See table I , subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
<u>Test 1</u>						
On-state gate charge			$Q_{g(on)}$			nC
2N6804					29.0	
2N6806					31.0	
<u>Test 2</u>						
Gate to source charge			Q_{gs}			
2N6804					7.1	
2N6806					7.0	

See footnote at end of table.

MIL-PRF-19500/562F
w/AMENDMENT 1

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> – Continued						
<u>Test 3</u>						
Gate to drain charge			Q_{gd}			nC
2N6804					21.0	
2N6806					17.0	
Reverse recovery time	3473	$V_{DD} \leq -50$ V, condition A	t_{rr}			ns
2N6804		$di/dt \leq -100$ A/ μ s; $I_F = -11$ A			250	
2N6806		$di/dt \leq -100$ A/ μ s; $I_F = -6.5$ A			400	

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:

Group B, subgroups 3 and 4 (JANS).

Group B, subgroups 2 and 3 (JANTXV).

Group C, subgroup 2 and 6.

Group E, subgroup 1.

3/ This test is optional if performed as a 100 percent screen.

MIL-PRF-19500/562F
w/AMENDMENT 1

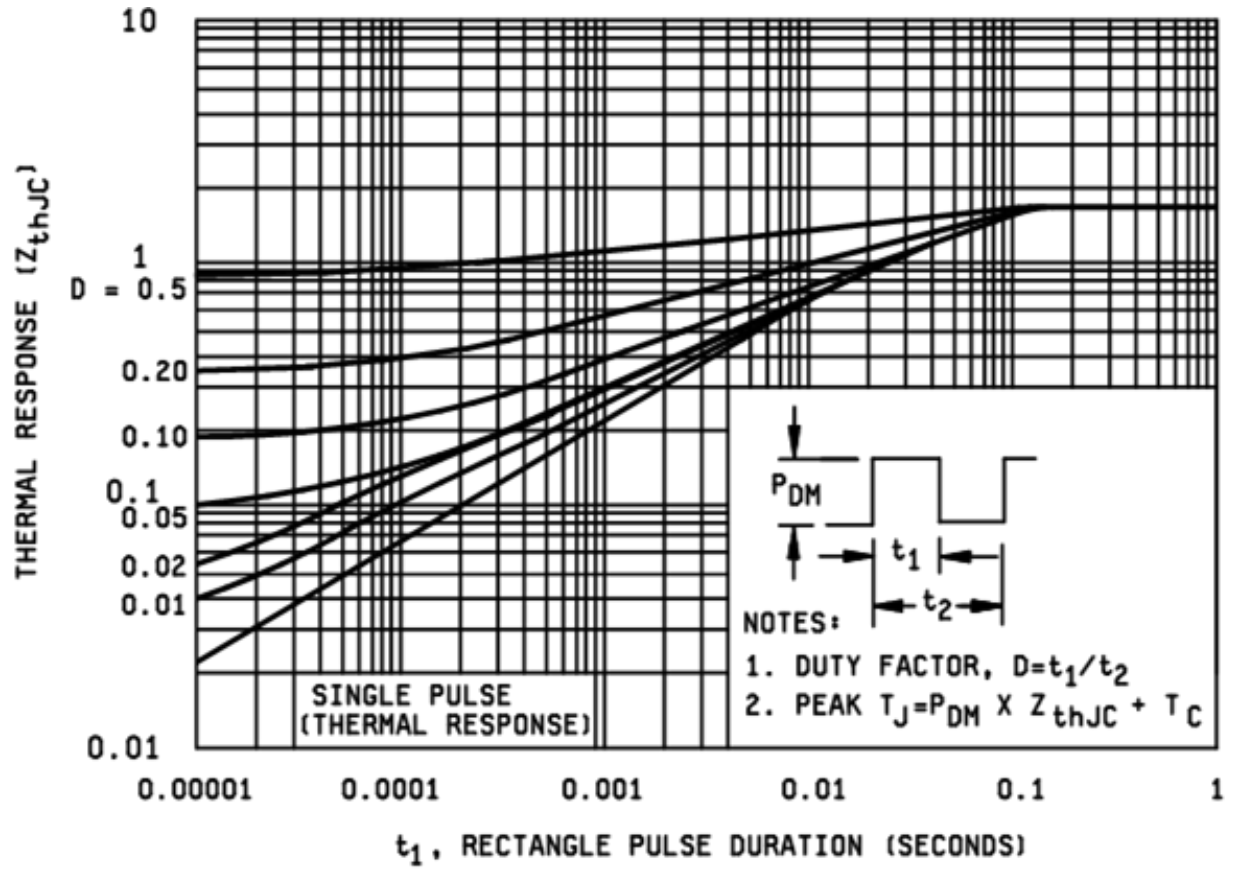
TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection <u>1/</u>	MIL-STD-750		Qualification inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 2/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

1/ JANHC and JANKC devices are qualified in accordance with [MIL-PRF-19500](#).

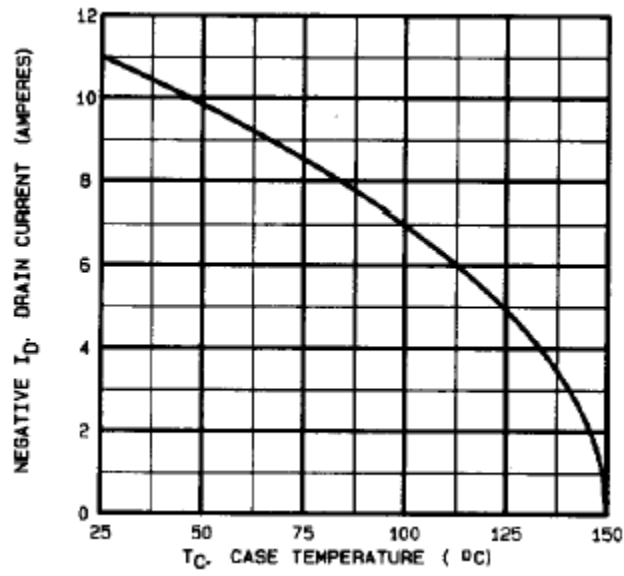
2/ A separate sample may be pulled for each test.

2N6804 and 2N6806

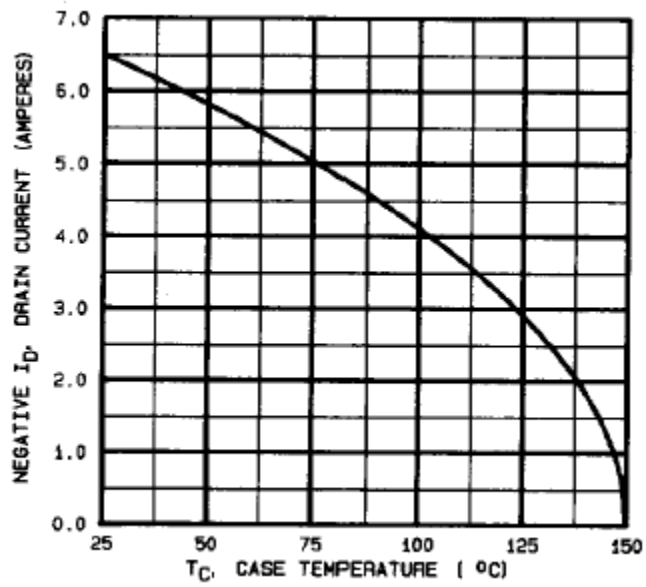


NOTE: These curves refer to devices packaged in a TO-204AA package only.

FIGURE 5. Transient thermal impedance.

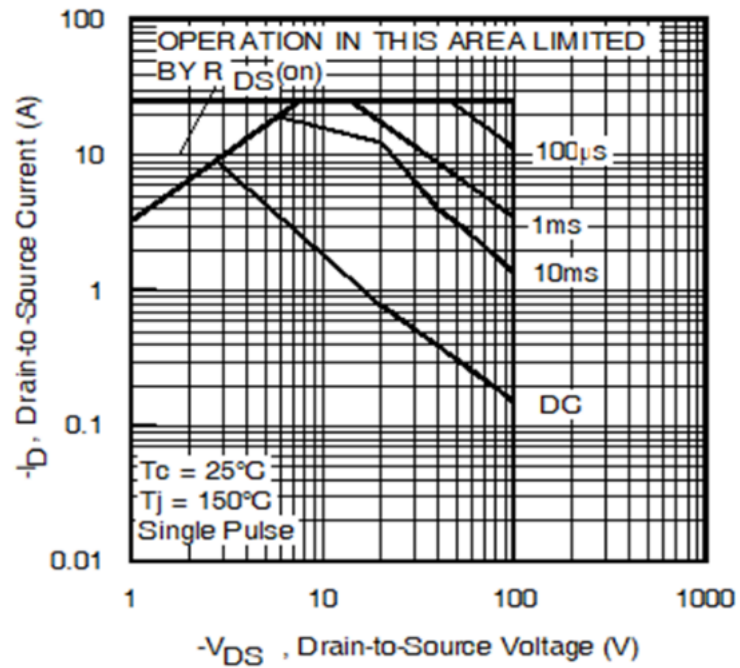


2N6804



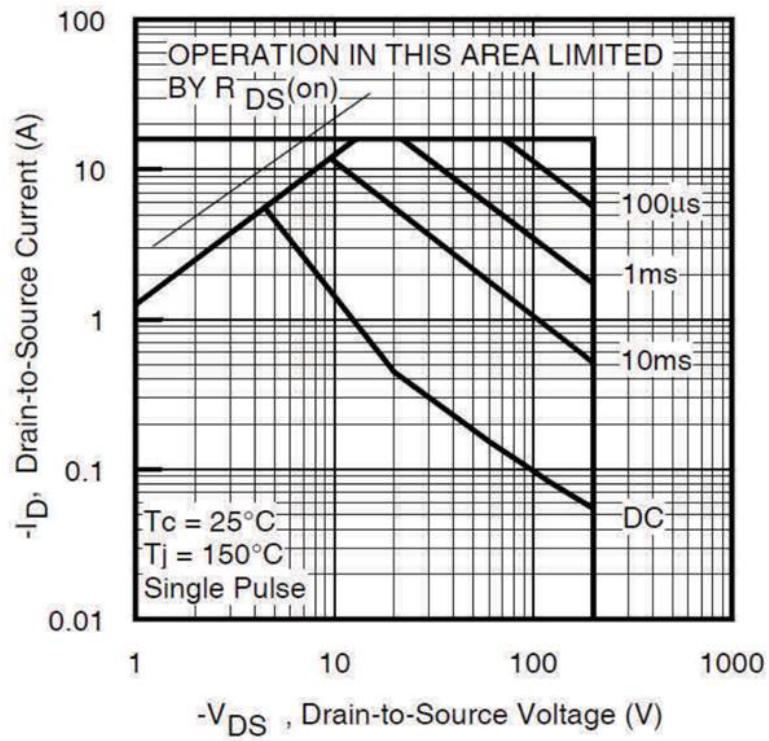
2N6806

FIGURE 6. Maximum drain current versus case temperature graphs.



NOTE: These curves refer to devices packaged in a TO-204AA package only.

FIGURE 7. Maximum safe operating area.



NOTE: These curves refer to devices packaged in a TO-204AA package only.

* FIGURE 7. Maximum safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.6.
- e. For die acquisition, the JANHC or JANKC letter version should be specified (see figures 3 and 4).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QPDSIS-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

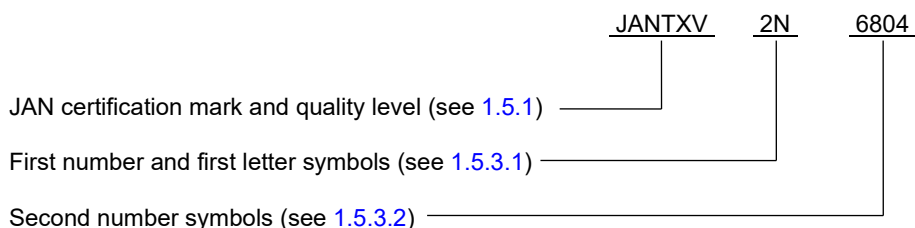
6.4 Cross-reference and complement list. Parts from this specification may be used to replace the following commercial Part or Identifying Number (PIN's). The term Part or Identifying Number (PIN) is equivalent to the term part number which was previously used in this specification.

Preferred types	Commercial types	Complement
2N6804	IRF9130, IRF9131, IRF9132, IRF9133	2N6756
2N6806	IRF9230, IRF9231, IRF9232, IRF9233	2N6758

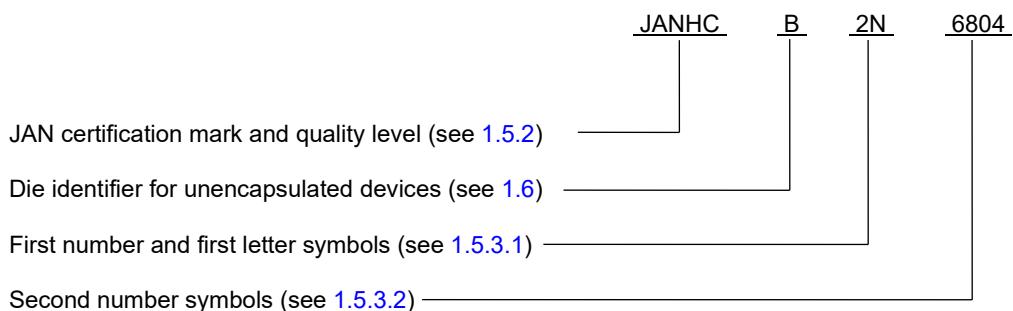
MIL-PRF-19500/562F
w/AMENDMENT 1

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6804	JANTX2N6804	JANTXV2N6804	JANS2N6804
JAN2N6806	JANTX2N6806	JANTXV2N6806	JANS2N6806

6.6.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (example JANHCA2N6804) will be identified on the QML.

JANC ordering information		
PIN	Manufacturers	
	69210	43611
2N6804	JANHCA6804 JANKCA6804	JANHCB2N6804 JANKCB2N6804
2N6806	JANHCA6806 JANKCA6806	

*

MIL-PRF-19500/562F
w/AMENDMENT 1

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

* 6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA -CC

Preparing activity:
DLA - CC

(Project 5961- 2024-016)

Review activities:

Army - AR, MI
* Navy - AS
Air Force - 19, 70

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.