

The documentation and process conversion measures necessary to comply with this document shall be completed by 9 February 2023.

INCH-POUND

MIL-PRF-19500/547F
w/AMENDMENT 2
9 November 2022
SUPERSEDING
MIL-PRF-19500/547F
w/AMENDMENT 1
4 September 2020

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, N-CHANNEL, SILICON, POWER,
LOW-THRESHOLD LOGIC LEVEL, HIGH FREQUENCY, HIGH SWITCHING SPEED,
DEVICE TYPES 2N6660 AND 2N6661, THROUGH HOLE AND SURFACE MOUNT PACKAGES,
QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, low-threshold logic level, high frequency, high switching speed MOSFET, power transistor. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Package outlines. The device package outlines are a three terminal metal can TO-205AD package (formerly TO-39) in accordance with [figure 1](#) and surface mount package with metal lid (UB) or ceramic lid (UBC) in accordance with [figure 2](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$	$R_{\theta JSP}$ (2)	V_{DS}	V_{DGR} (3)	V_{GS}	I_{D1} (4) $T_C = +25^\circ\text{C}$	I_{D2} (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM}	T_J and T_{STG}
	<u>W</u>	<u>mW</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>
2N6660	6.25	725	20		60	60	± 20	0.99	0.62	-0.99	3	-65 to +150
2N6661	6.25	725	20		90	90	± 20	0.86	0.54	-0.86	3	
2N6660UB	2.5	570		40	60	60	± 20	0.99	0.62	-0.99	3	
2N6661UB	2.5	570		40	90	90	± 20	0.86	0.54	-0.86	3	

- (1) Derate linearly by 0.05 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$ for 2N6660 and 2N6661. Derate linearly by 0.02 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$ for 2N6660UB and 2N6661UB.
- (2) See [figure 3](#) for thermal impedance curves.
- (3) $R_{GS} \leq 1\text{ M}\Omega$.
- (4) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

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AMSC N/A

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FSC 5961



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* 1.4 Primary electrical characteristics. $T_C = +25\text{ }^{\circ}\text{C}$ unless otherwise noted.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0\text{ V}$	$V_{GS(th)1}$ $V_{DS} = V_{GS}$	Max I_{DSS1} $V_{GS} = 0\text{ V}$	Max $r_{DS(on)} (1)$ $V_{GS} = 10\text{ V dc}$	
	$I_D = 10\text{ }\mu\text{A dc}$	$I_D = 1.0\text{ mA dc}$	$V_{DS} = 80\text{ percent}$ of rated V_{DS}	$T_J = +25\text{ }^{\circ}\text{C}$ at I_{D1}	$T_J = +150\text{ }^{\circ}\text{C}$ at I_{D2}
	<u>V dc</u>	<u>V dc</u> <u>Min</u> <u>Max</u>		<u>Ω</u>	<u>Ω</u>
2N6660, UB	60	0.8	2.0	1.0	3.0
2N6661, UB	90	0.8	2.0	1.0	4.0
					6.33
					8.44

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

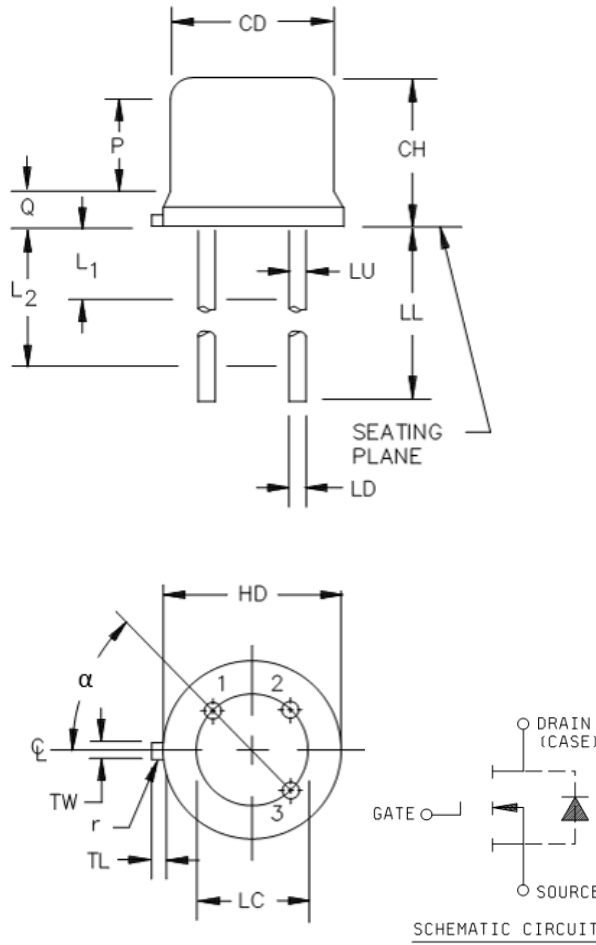
1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows: "6660" and "6661".

1.5.3 Suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

Blank	A blank designator identifies the package outline as a three terminal metal can TO-205-AD package (formerly TO-39) in accordance with figure 1.
UB	This designator identifies the package outline as a 4-terminal metal lid (used as a shield and connected to the fourth pad) SMD package in accordance with figure 2.
UBC	This designator identifies the package outline as a 4-terminal ceramic lid SMD package in accordance with figure 2.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

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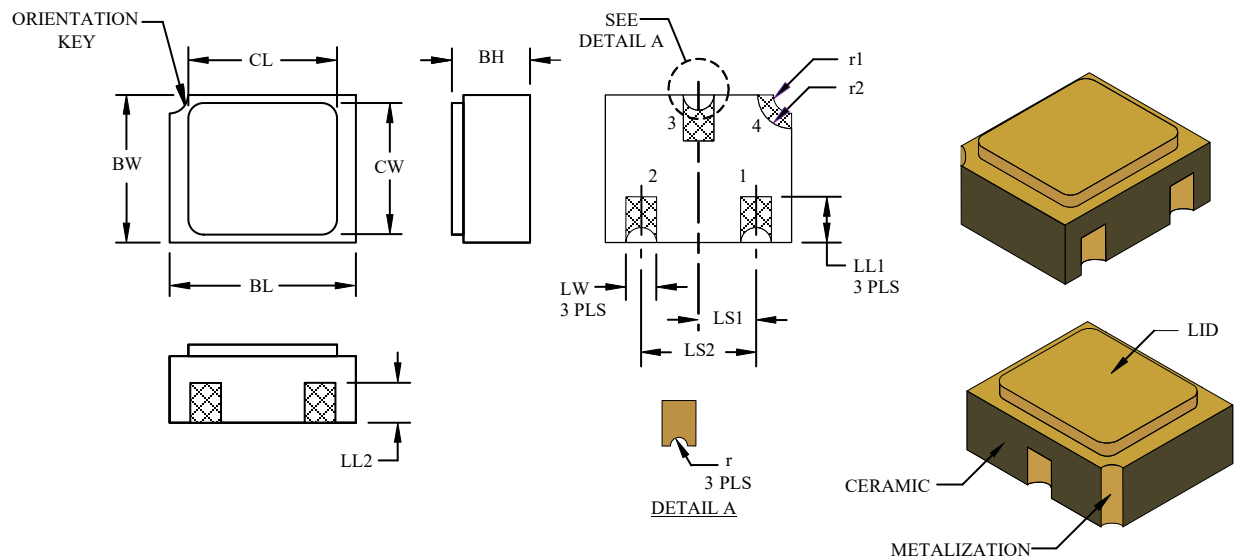
Symbol	Dimensions				Notes
	Inches	Inches	mm	mm	
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
TW	.028	.034	0.71	0.86	2
TL	.029	.045	0.74	1.14	3
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8
LC	0.200	TP	5.08	TP	6
LU	.016	.019	0.41	0.48	7, 8
L1		.050		1.27	7, 8
L2	.250		6.35		7, 8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	9
α	45°	TP	45°	TP	6

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, dimension TW shall be held for a minimum length of .011 inch (0.28 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 +.001, -.000 inch (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between dimensions L1 and L2. Dimension LD applies between dimensions L2 and LL minimum. Diameter is uncontrolled in dimension L1 and beyond dimension LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
- * 10. Terminal 1 = Source, 2 = Gate, 3 = Drain. The Drain is electrically connected to the case.

* FIGURE 1. Physical dimensions of TO-205-AD package.

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Symbol	Dimensions				Notes	Symbol	Dimensions				Notes
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BL	.115	.128	2.92	3.25		LL2	.009	.036	0.23	0.89	6
BW	.085	.108	2.16	2.74		LS1	.035	.040	0.89	1.02	
BH	.040	.056	1.02	1.42	4	LS2	.071	.079	1.80	2.01	
BH	.055	.069	1.40	1.75	5	LW	.016	.024	0.41	0.61	6
CL		.128		3.25		r		.008		0.20	
CW		.108		2.74		r1		.012		0.30	7
LL1	.022	.038	0.56	0.97	6	r2		.022		0.56	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Hatched areas on package denote metallized areas.
3. Pad 1 = Gate, 2 = Source, 3 = Drain, 4 = shielding connected to the lid (UB only) or lid braze ring (UBC only).
4. Dimension BH for UB packages with medal lid.
5. Dimension BH for UBC packages with ceramic lid.
6. Three places.
7. For design reference only.

FIGURE 2. Physical dimensions for UB and UBC style surface mount package.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in **MIL-PRF-19500** and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in **MIL-PRF-19500**.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in **MIL-PRF-19500**, on figures 1 (TO-205AD) and 2 (UB and UBC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with **MIL-PRF-19500**, **MIL-STD-750**, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be acceptable.

3.5 Marking. Marking shall be in accordance with **MIL-PRF-19500**.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4 and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

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3.8 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is applied drain to source.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and herein. Alternate flow is allowed for qualification inspection in accordance with [MIL-PRF-19500](#).

4.2.1 Group E inspection. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

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4.3 Screening (quality levels JANS, JANTX and JANTXV only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurements for JANS level	Measurements for JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
9	Subgroup 2 of table I herein. I_{DSS1} , I_{GSSF1} , I_{GSSR1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$. Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$. Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A.	Method 1042 of MIL-STD-750, test condition A.
13	Subgroups 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 1$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value or ± 0.5 ohm, whichever is greater. $\Delta V_{GS(TH)1} = \pm 10$ percent of initial value or ± 0.3 V dc.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 10$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 1$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value or ± 0.5 ohm, whichever is greater. $\Delta V_{GS(TH)1} = \pm 10$ percent of initial value or ± 0.3 V dc.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , t_{MD} (and V_H where appropriate). See group E, table II, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#), and herein.

4.4.2.1 Quality level JANS.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1051	Test condition G.
B4	1042	Test condition D; 2,000 cycles. The heating cycle shall be 1 minute minimum. $V_{DS} = 10 \text{ V dc}$, $P_T = \text{see } 1.4$ at $T_A = +25 \text{ }^\circ\text{C} \pm 3 \text{ }^\circ\text{C}$.
B5	1042	Accelerated steady-state operation life; test condition C; $T_A = +25 \text{ }^\circ\text{C}$, $-5 \text{ }^\circ\text{C}$, $+10 \text{ }^\circ\text{C}$, $V_{DS} = 10 \text{ V min.}$; I_D adjusted to meet a junction temperature of $140 \text{ }^\circ\text{C}$, $-0 \text{ }^\circ\text{C}$, $+10 \text{ }^\circ\text{C}$, $t = 240 \text{ hours}$.
B5	2037	Test condition D (Al-Au die interconnects only).

4.4.2.2 Quality levels JAN, JANTX, and JANTXV.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced air cooling on the device shall be permitted during the on cycle; $t_{on} = 30 \text{ seconds minimum}$.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C5	3161	Thermal resistance, see 4.5.2 , $R_{\theta JC(max)} = 20 \text{ }^\circ\text{C/W}$.
C6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced air cooling on the device shall be permitted during the on cycle; $t_{on} = 30 \text{ seconds minimum}$.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , t_{MD} (and V_H where appropriate). See table E-IX of [MIL-PRF-19500](#), group E, subgroup 4.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See <u>4.3.2</u>	$Z_{\theta JC}$			°C/W
* Breakdown voltage, drain to source 2N6660, UB 2N6661, UB	3407	Bias condition C; $V_{GS} = 0$ V; $I_D = 10$ μ A dc	$V_{(BR)DSS}$	60 90		V dc
* Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$; $I_D = 1.0$ mA dc	$V_{GS(th)1}$	0.8	2.0	V dc
Gate current	3411	Bias condition C; $V_{DS} = 0$ V; $V_{GS} = +20$ V dc	I_{GSSF1}		+100	nA dc
Gate current	3411	Bias condition C; $V_{DS} = 0$ V; $V_{GS} = -20$ V dc	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C; $V_{GS} = 0$; $V_{DS} = 80$ percent of rated V_{DS} (see <u>1.3</u>)	I_{DSS1}		1.0	μ A dc
Static drain to source on-state resistance 2N6660, UB 2N6661, UB	3421	Condition A; $V_{GS} = 10$ V dc; pulsed (see <u>4.5.1</u>); $I_D = 1.0$ A dc	$r_{DS(on)1}$		3.0 4.0	ohms ohms
Static drain to source on-state resistance 2N6660, UB 2N6661, UB	3421	Condition A; $V_{GS} = 5$ V dc; pulsed (see <u>4.5.1</u>); $I_D = 0.3$ A dc	$r_{DS(on)2}$		5.0 5.3	ohms ohms
Forward voltage (source drain diode) 2N6660, UB 2N6661, UB	4011	Condition A, pulsed (see <u>4.5.1</u>); $V_{GS} = 0$ V $I_S = 0.99$ A dc $I_S = 0.86$ A dc	V_{SD}	0.7 0.7	1.6 1.4	V(pk) V(pk)
Forward transconductance 2N6660, UB 2N6661, UB	3475	Pulsed (see <u>4.5.1</u>), $V_{DS} = V_{GS} = 7.5$ V dc $I_{D1} = 525$ m A dc $I_{D2} = 475$ m A dc	g_{FS}	170		ms

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation		T _C = +125 °C				
Gate current	3411	Bias condition C, V _{DS} = 0 V; V _{GS} = +20 V dc or -20 V dc	I _{GSS2}		±500	nA dc
Drain current	3413	Bias condition C, V _{GS} = 0 V, V _{DS} = -80 percent of rated V _{DS} (see 1.3)	I _{DSS2}		100	µA dc
Static drain to source on-state resistance 2N6660, UB 2N6661, UB	3421	V _{GS} = 10 V dc; condition A; pulsed (see 4.5.1); I _D = 1.0 A dc	r _{DS(on)3}		5.6 7.5	ohms
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = 1.0 mA dc	V _{GS(th)2}	0.3		V dc
Low temperature operation:		T _C = -55°C				
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} ; I _D = 1.0 mA	V _{GS(th)3}		2.5	V dc
<u>Subgroup 4</u>						
Switching time test	3472	R _{GS} = 23 Ω, R _L = 23 Ω, V _{GEN} = 10 V				
Turn-on delay time		V _{DD} = 25 V dc; I _D ≅ 1 A dc,	t _{d(on)}		10	ns
Turn-off delay time		V _{DD} = 25 V dc; I _D ≅ 1 A dc	t _{d(off)}		10	ns
Small signal common source short-circuit input capacitance	3431	V _{DS} = 25 V dc; V _{GS} = 0 V; f = 1 MHz	C _{iss}		50	pF
Small signal common source short-circuit output capacitance		V _{DS} = 25 V dc; V _{GS} = 0 V; f = 1 MHz	C _{oss}		40	pF
Small signal common source short-circuit reverse transfer capacitance	3433	V _{DS} = 25 V dc; V _{GS} = 0 V; f = 1 MHz	C _{rss}		10	pF

See footnotes at end of table.

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TABLE I. Group A inspection – Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area		See figure 4				
High voltage test		V_{DS} = 80 percent of rated V_{DS} (see 1.3); I_D as specified on figure 4 ; t_p = 10 ms				
Electrical measurements		See table I , subgroup 2				
<u>Subgroups 6 and 7</u>						
Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test required for the following subgroups:

- Group B, subgroups 3, 4 and 5 (JANS).
- Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071	Fine and gross leak	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2</u>			45 devices, c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hour	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size, N/A
Thermal impedance curves		See MIL-PRF-19500	
<u>Subgroup 10</u>			22 devices, c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	

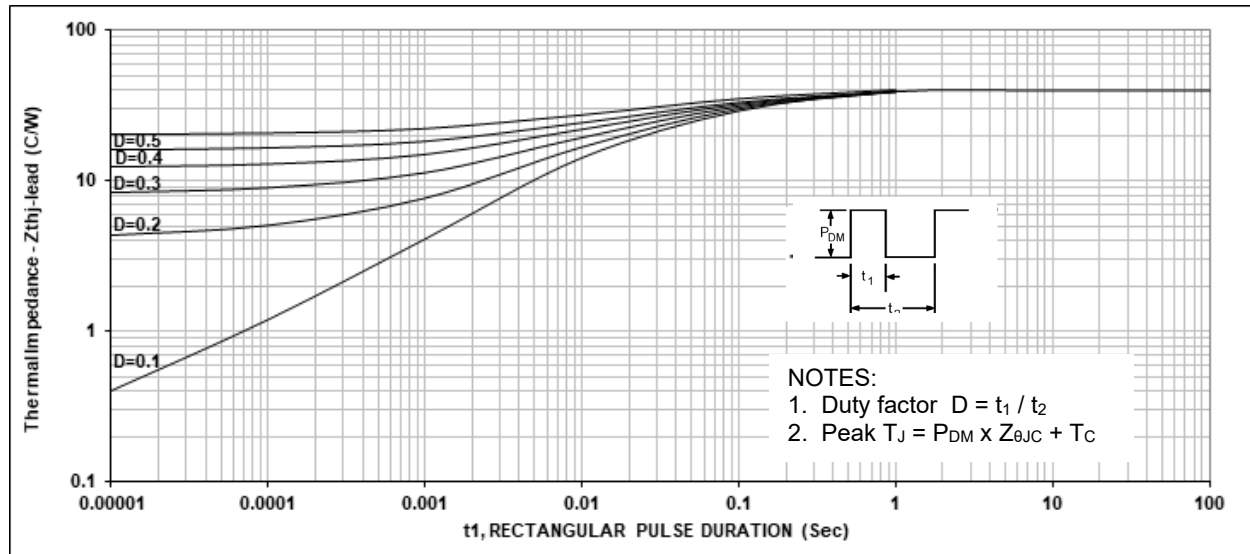


FIGURE 3. Thermal impedance graph ($R_{\theta JS}$) for 2N6660UB and 2N6661UB.

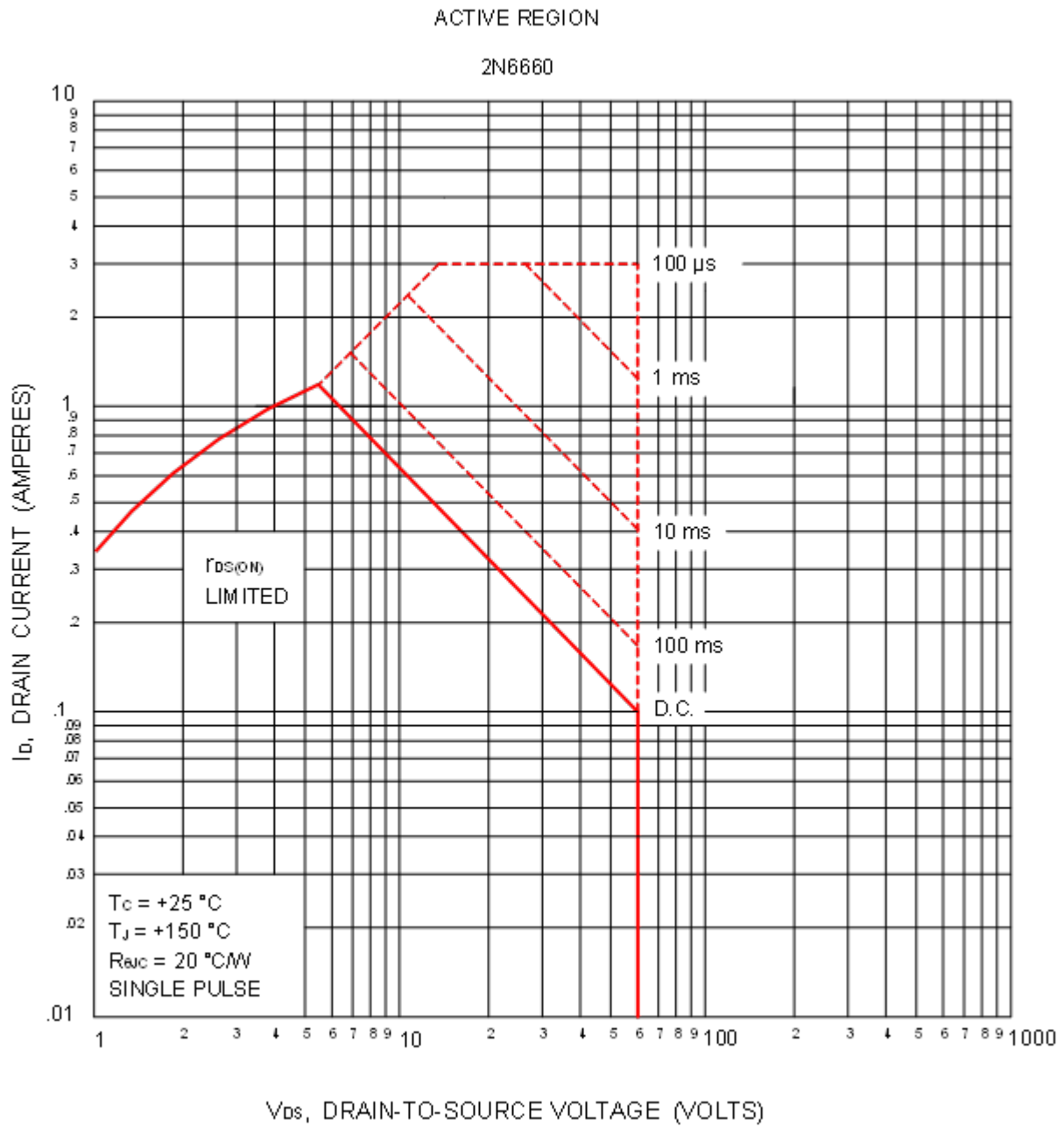


FIGURE 4. Maximum safe operating area.

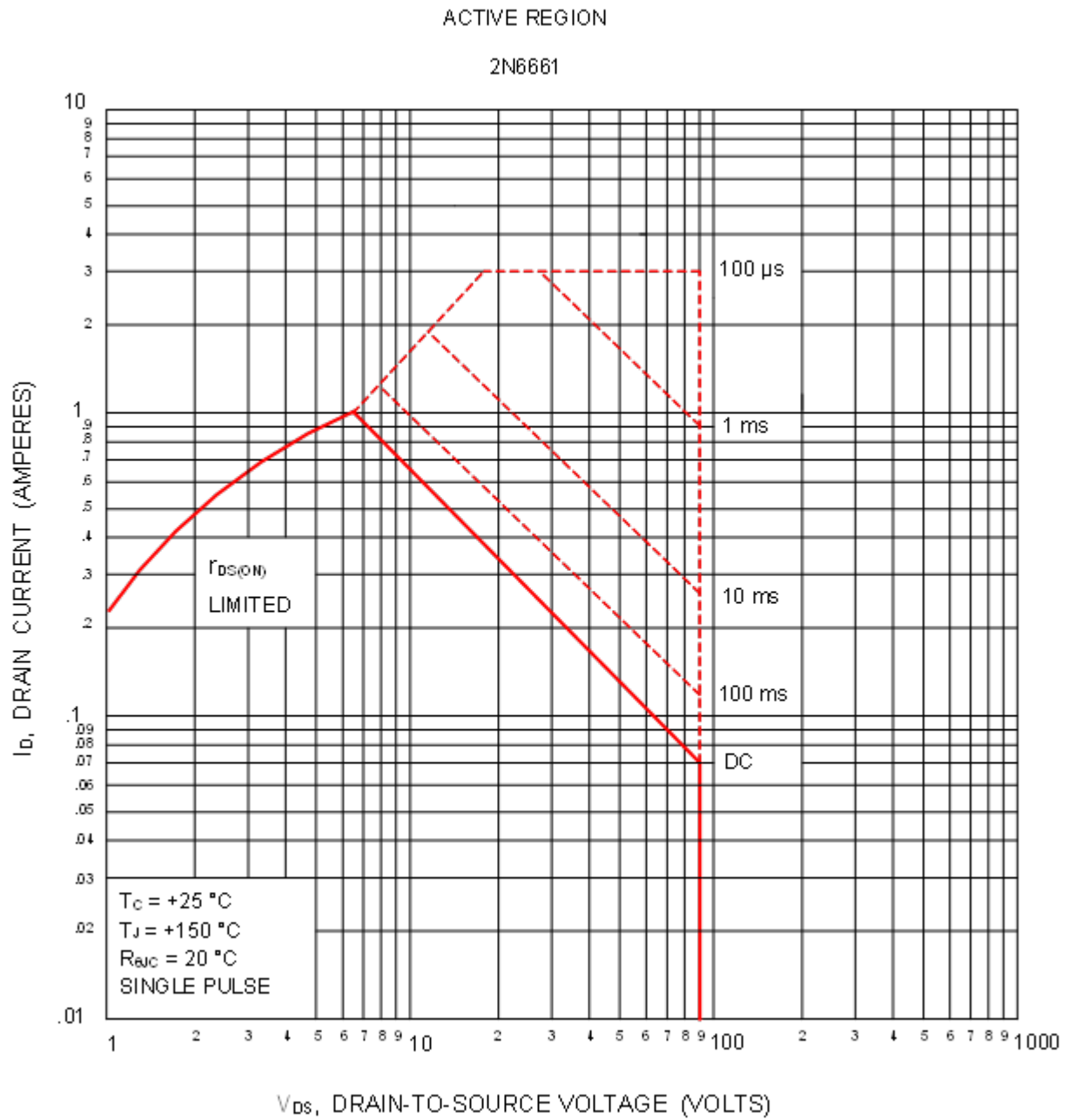


FIGURE 4. Maximum safe operating area - Continued.

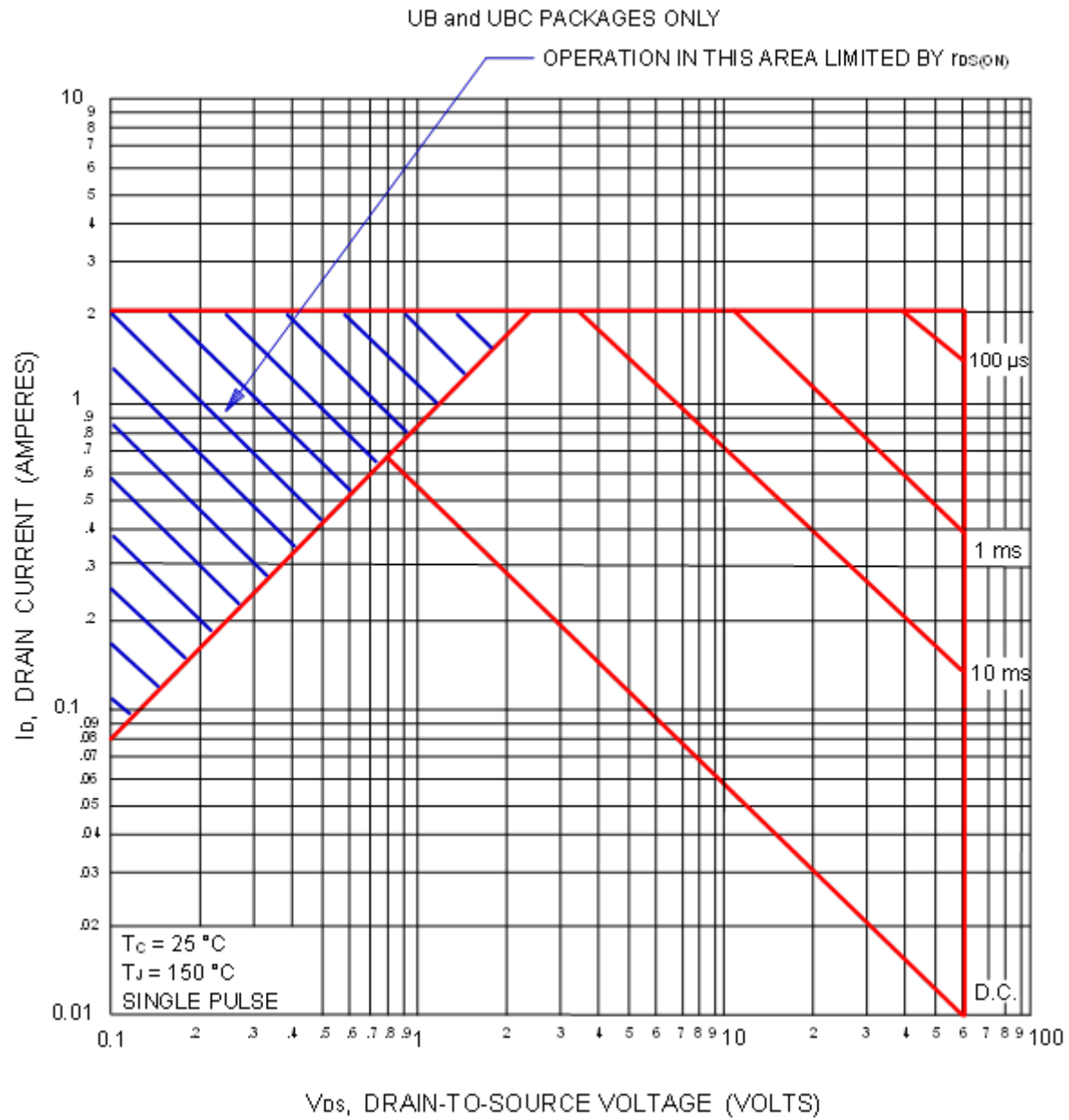


FIGURE 4. Maximum safe operating area - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

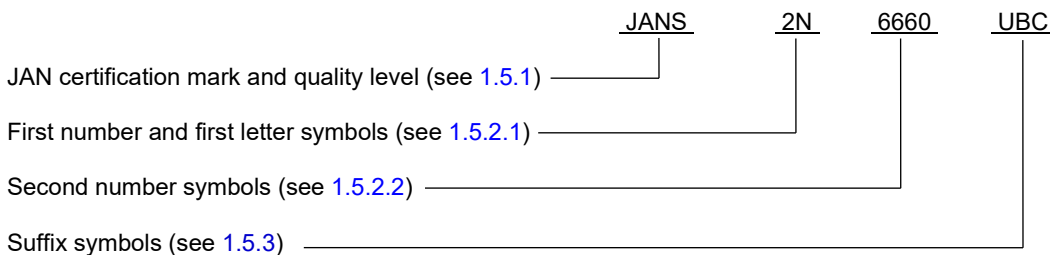
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see [5.1](#)).
- c. Lead finish (see [3.4.1](#)).
- d. The complete PIN, see [1.5](#) and [6.4](#).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



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6.5 List of PINs. The following is a list of all possible PINs for the devices available on this specification sheet.

Quality level "JAN"	Quality level "JANTX"	Quality level "JANTXV"	Quality level "JANS"
TO-205-AD Package			
JAN2N6660	JANTX2N6660	JANTXV2N6660	JANS2N6660
JAN2N6661	JANTX2N6661	JANTXV2N6661	JANS2N6661
Surface Mount UB and UBC Packages			
JAN2N6660UB	JANTX2N6660UB	JANTXV2N6660UB	JANS2N6660UB
JAN2N6661UB	JANTX2N6661UB	JANTXV2N6661UB	JANS2N6661UB
JAN2N6660UBC	JANTX2N6660UBC	JANTXV2N6660UBC	JANS2N6660UBC
JAN2N6661UBC	JANTX2N6661UBC	JANTXV2N6661UBC	JANS2N6661UBC

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
 Army – CR
 * Navy – SH
 Air Force – 85
 NASA – NA
 DLA – CC

Preparing activity:
 DLA – CC

(Project 5961-2022-087)

Review activity:
 Army – AR
 Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.