The documentation and process conversion measures necessary to comply with this document shall be completed by 10 July 2026.

INCH-POUND

MIL-PRF-19500/533N
w/AMENDMENT 2
10 March 2026
SUPERSEDING
MIL-PRF-19500/533N
w/AMENDMENT 1
20 November 2020

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICES, DIODE, SILICON, VOLTAGE REGULATOR,
TYPES 1N6309 THROUGH 1N6355; 5, 2, AND 1 PERCENT VOLTAGE TOLERANCE,
ENCAPSULATED (AXIAL LEAD THROUGH-HOLE AND SURFACE MOUNT PACKAGES) AND
UN-ENCAPSULATED (DIE), QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for microminiature 500 mW, silicon, metallurgically bonded, voltage regulator diodes with voltage tolerances of 5 percent, 2 percent (C), and 1 percent (D). Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance (JANHC and JANKC) are provided for unencapsulated devices.

1.2 Package outlines and die topography. The device packages for the encapsulated device types are as follows: DO-35 in accordance with figure 1, US surface mount in accordance with figure 2, UB surface mount in accordance with figure 3, and UB2 surface mount in accordance with figure 4. The dimensions and topography for JANHC and JANKC unencapsulated die in accordance with figures 5, 6, 7, and 8.

1.3 Maximum ratings. Maximum ratings are as shown in maximum and primary test ratings (see 3.6.1 herein) and as follows:

a. P_{TL} = 500 mW (DO-35) at T_L = + 75°C, L = .375 inch (9.53 mm); both ends of case or diode body to heat sink at L = .375 inch (9.53 mm). (Derate I_Z to 0 at +175°C.)

b. P_{TEC} = 500 mW (US surface mount) at T_{EC} = +125°C. (Derate to 0 at +175°C.)

c. $P_{T(PCB)}$ = 500 mW, T_A = +55°C (see note 1.) (Derate to 0 at +175°C.)
-65°C ≤ T_J ≤ +175°C; -65°C ≤ T_{STG} ≤ +175°C.

d. $P_{SP(IS)}$ = 500 mW (UB) at $T_{SP(IS)}$ = 125°C. (Derate to 0 at +175°C.)
-65°C ≤ T_J ≤ +175°C; -65°C ≤ T_{STG} ≤ +175°C.

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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1.3 Maximum ratings. – continued.

(1) For derating, see figures 10, 11, 12, 13, and 14.

(2) T_A = +55°C before derating for both axial and US on printed circuit board (PCB). The details for determining ratings when axial leaded or US devices are mounted horizontally on a PCB and in still air are as follows. Base material is FR4 .0625 inch (1.59 mm) thick, 1-layer 1-oz copper. PCB pad size for US devices = .067 inch (1.70 mm) x .105 inch (2.67 mm); PCB land sizes for axial leaded devices is .092 inch (2.34 mm) diameter with L ≤ .187 inch (4.75 mm) lead length. Strips connected to the lands and pads are .030 inch (0.76 mm) x 1 inch (25.4 mm) long.

1.4 Primary electrical characteristics. Primary electrical characteristics are shown in maximum and primary test ratings (see 3.6.1 herein) and as follows:

a. 2.4 V dc ≤ V_Z ≤ 200 V dc (nominal).

b. Noise density, see 4.5.6 and figure 9.

c. 1N6309 through 1N6355 devices are ±5 percent voltage tolerance.

d. 1N6309C through 1N6355C devices are ±2 percent voltage tolerance.

e. 1N6309D through 1N6355D devices are ±1 percent voltage tolerance.

f. For thermal impedance curves, see figures 15, 16, 17, 18, and 19.

g. Axial leaded DO-35 (non-surface mount).

(1) For types, 1N6309 through 1N6320, at L = .375 inch (9.53 mm) $R_{\theta JL}$ = 150°C/W (maximum). See figure 10 for derating and figure 15 for thermal impedance.

(2) For types, 1N6321 through 1N6355, at L = .375 inch (9.53 mm) $R_{\theta JL}$ = 95.5°C/W (maximum). See figure 11 for derating and figure 16 for thermal impedance.

(3) For all non-surface mount types, at L = 0 inch, $R_{\theta JL}$ = 50°C/W (maximum).

h. Surface mount (US).

(1) 1N6309US through 1N6320US, $R_{\theta JEC}$ = 35°C/W (maximum). See figure 12 for derating and figure 17 for thermal impedance.

(2) 1N6321US through 1N6355US, $R_{\theta JEC}$ = 21°C/W (maximum). See figure 13 for derating.

(3) 1N6309US through 1N6355US, see figure 14 for derating.

(4) 1N6321US through 1N6355US, $R_{\theta JEC}$ = 21°C/W (maximum). See figure 17 for thermal impedance.

i. $R_{\theta JA}$ = 240°C/W junction to ambient including PCB. $R_{\theta JA}$ with a defined thermal resistance condition included is measured at I_Z = as defined in the characteristics and ratings table herein.

j. $R_{\theta JSP(IS)}$ = 90°C/W (maximum) junction to solder pad (infinite sink) (UB). See figure 18.

k. $R_{\theta JA(PCB)}$ = 250°C/W (maximum) junction to ambient (PCB) (UB). See figure 19.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN brand and quality level indicator.

1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows: "6309" through "6355".

1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN as applicable:

1.5.3.1 First suffix symbol (voltage tolerance). The lack of a suffix letter indicates that the device is a ±5 percent voltage tolerance. The letter "C" indicates that the device is a ±2 percent voltage tolerance. The letter "D" indicates that the device is a ±1 percent voltage tolerance.

1.5.3.2 Second suffix symbols (package designators). The following suffix symbols that designate the package outline for the devices covered by this specification sheet are as follows.

	A blank package designator suffix symbol indicates an axial through-hole mount package (see figure 1.).
US	Indicates a surface mount, square endcap package. (see figure 2)
UB	Indicates a 3 terminal, 4 pad surface mount. See figure 3 for internal configuration.
UB2	Indicates a 2 terminal, 4 pad surface mount. See figure 4 for internal configuration.

1.5.3.3 Internal circuit schematic designator suffix symbols (for UB and UB2 packages only). The suffix symbols that designate the internal circuit schematic (see schematics on figure 3) of the surface mount packages are as follows:

	A blank circuit schematic designator indicates a unidirectional single diode circuit for UB packages only or a standard polarity configuration for UB2 packages.
CA	Indicates dual diode with a common anode pin (UB package only).
CC	Indicates a dual diode with a common cathode pin (UB package only).
D	Indicates a dual diode doubler (UB package only).
R	Indicates a reverse polarity configuration (UB2 package only).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.5.5 Die identifiers for unencapsulated devices. The manufacturer die identifiers that are applicable for this specification sheet are "A", "B", "C", "D", and "E" (see 6.5).

2. APPLICABLE PUBLICATIONS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

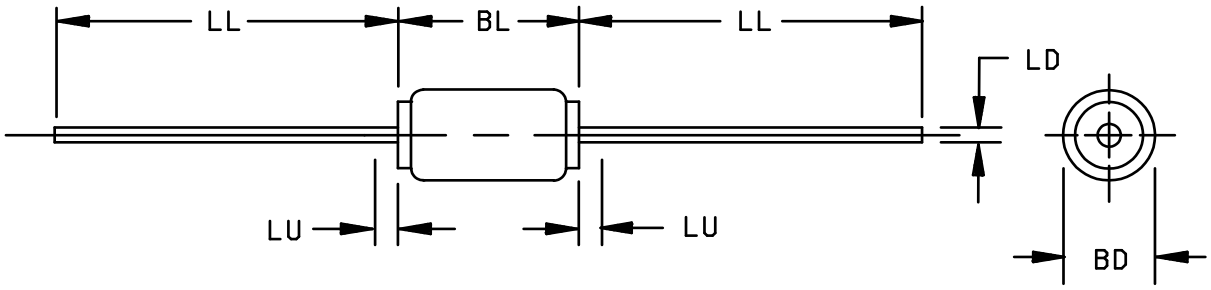
MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

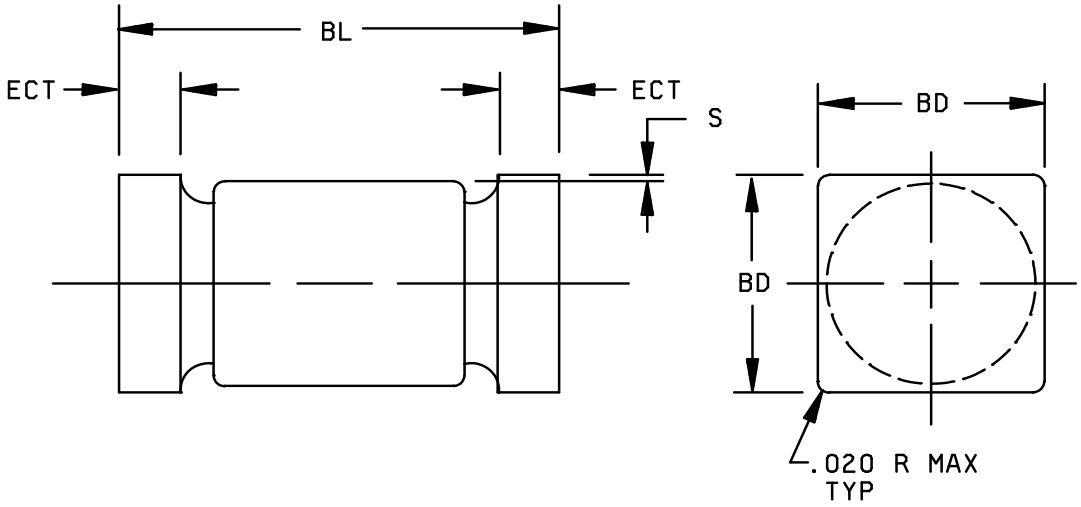


Ltr	Dimensions				Notes
	inch	inch	mm	mm	
	Min	Max	Min	Max	
BD	.060	.090	1.52	2.29	3
BL	.120	.200	3.05	5.08	4
LD	.018	.022	0.46	0.56	
LL	1.000	1.500	25.40	38.10	
LU		.050		1.27	4

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.
3. Dimension BD shall be measured at the largest diameter.
4. The BL dimension shall include the entire body including slugs.
5. Dimension LU shall include the sections of the lead over which the diameter is uncontrolled. Lead diameter not controlled in this zone to allow for flash, lead finish build-up and minor irregularities other than slugs. This uncontrolled area is defined as the zone between the edge of the diode body and extending .050 inch (1.27 mm) onto the leads.

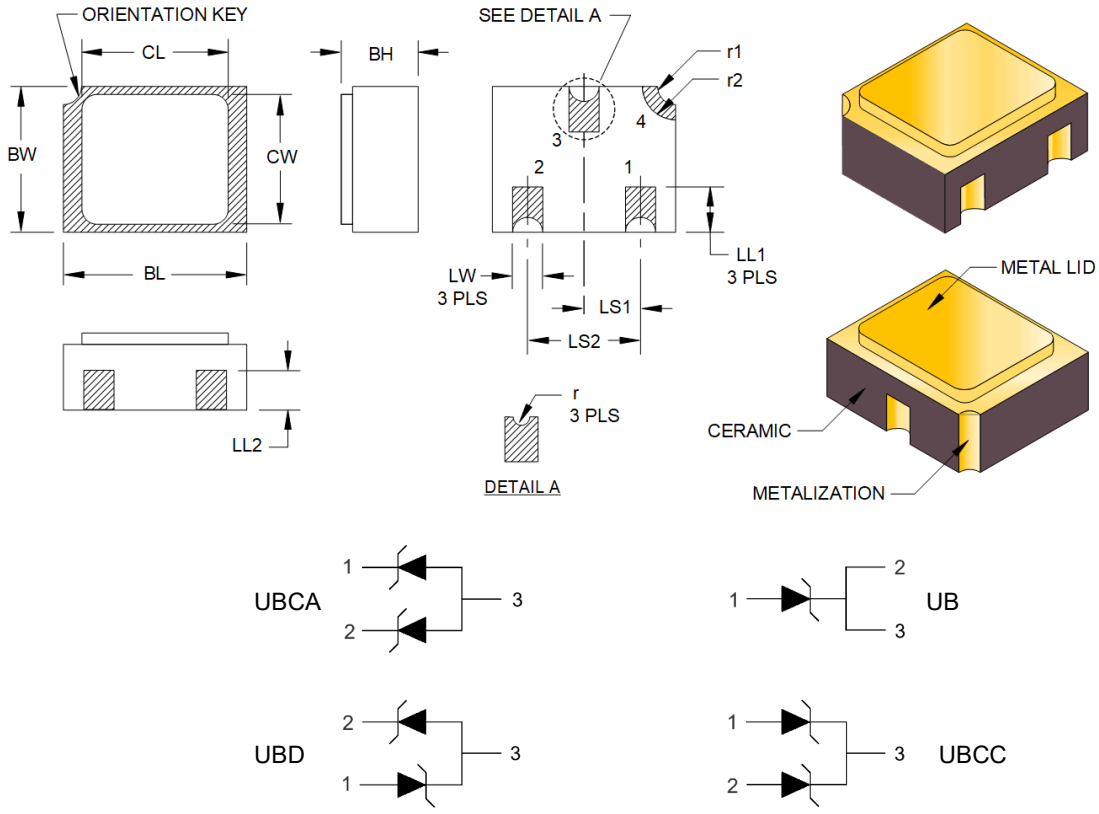
FIGURE 1. Physical dimensions for axial leaded DO-204AH package.



Symbol	Dimensions			
	inch	inch	mm	mm
	Min	Max	Min	Max
BD	.070	.085	1.78	2.16
BL	.165	.195	4.19	4.95
ECT	.019	.028	0.48	0.71
S	.003 min		0.08 min	

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.

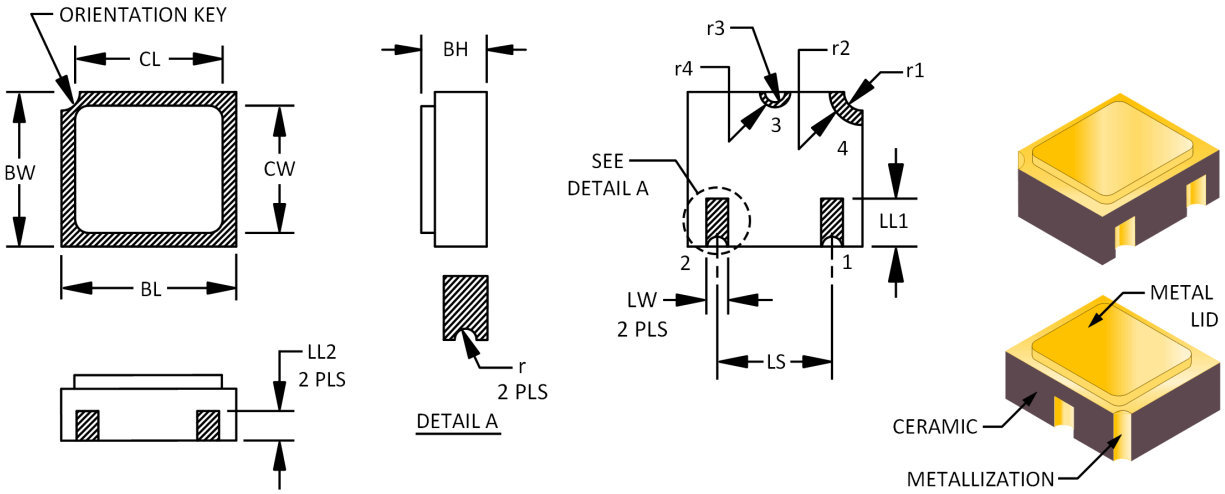
FIGURE 2. Physical dimensions for US surface mount device package.



Symbol	Dimensions				Symbol	Dimensions			
	inch	inch	mm	mm		inch	inch	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	.040	.056	1.02	1.42	LS1	.035	.039	0.89	0.99
BL	.115	.128	2.92	3.25	LS2	.071	.079	1.80	2.01
BW	.085	.108	2.16	2.74	LW	.016	.024	0.41	0.61
CL		.128		3.25	r		.008		0.20
CW		.108		2.74	r1		.012		0.31
LL1	.022	.038	0.56	0.97	r2		.022		0.56
LL2	.017	.035	0.43	0.89					

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Ceramic package only.
3. Hatched areas on package denote metallized areas. Pad 4 = shielding, connected to the lid.
4. Dimensions are pre-solder dip.

FIGURE 3. Physical dimensions, 3 terminal UB surface mount package.

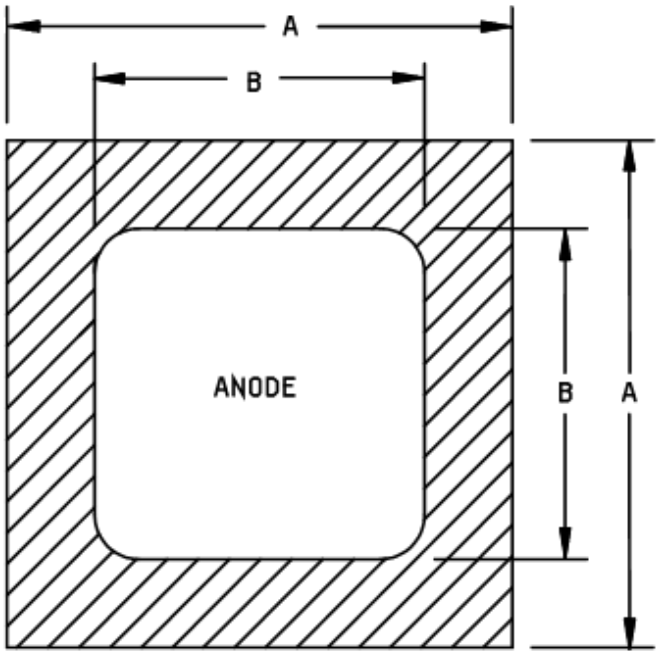


POLARITY

Symbol	Dimensions				Symbol	Dimensions			
	inch	inch	mm	mm		inch	inch	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	.046	.056	1.17	1.42	LS	.071	.079	1.80	2.01
BL	.115	.128	2.92	3.25	LW	.016	.024	0.41	0.61
BW	.085	.108	2.16	2.74	r	.008 TYP		0.20 TYP	
CL		.128		3.25	r1	.012 TYP		0.30 TYP	
CW		.108		2.74	r2	.022 TYP		0.56 TYP	
LL1	.022	.038	0.56	0.96	r3	.008 TYP		0.20 TYP	
LL2	.017	.035	0.43	0.89	r4	.012 TYP		0.30 TYP	

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Ceramic package only.
3. Hatched areas on package denote metallized areas. The corner pad = shielding, connected to the lid.
4. Dimensions are pre-solder dip.

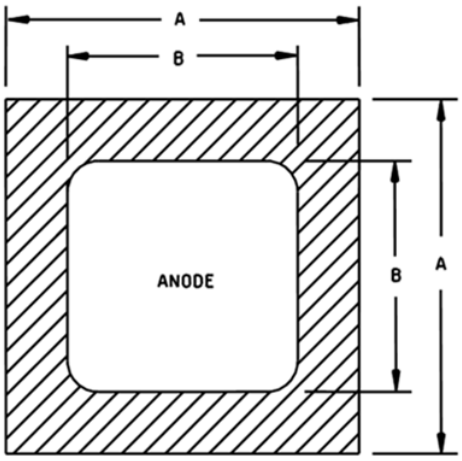
FIGURE 4. Physical dimensions, 2 terminal UB2 surface mount package.



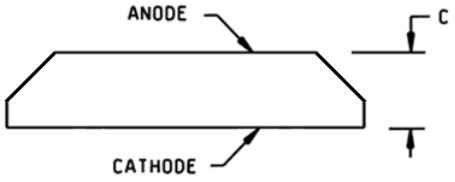
Ltr	Dimensions							
	JANHCA				JANHCC, JANKCC			
	inch	inch	mm	mm	inch	inch	mm	mm
	Min	Max	Min	Max	Min	Max	Min	Max
A	.021	.025	0.53	0.63	.019	.023	0.48	0.58
B	.013	.017	0.33	0.43	.013	.017	0.33	0.43

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. Circuit layout data: For zener operation, cathode must be operated positive with respect to anode.
3. The JANHCC and JANKCC die thickness is .010 (0.25 mm) ±.002 inches (±0.05 mm).
   Top (Anode) metallization: Minimum AL thickness = 12,000 Å for JANHCA and 25,000 Å for JANHCC and JANKCC.
   Back (Cathode) metallization: Minimum AU thickness = 3,000 Å for JANHCA, and 4,000 Å for JANHCC and JANKCC.

FIGURE 5. Physical dimensions JANHC and JANKC die (A and C versions).



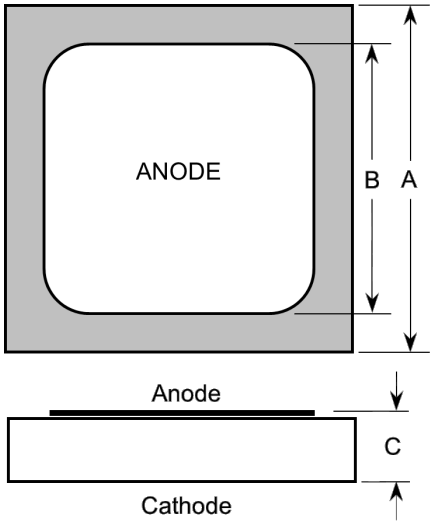
BACKSIDE IS CATHODE



Ltr	Dimensions			
	inch	inch	mm	mm
	Min	Max	Min	Max
A	.019	.023	0.483	0.584
B	.011	.015	0.279	0.381
C	.008	.012	0.203	0.305

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The physical characteristics of the die are as follows:
   Top (Anode) metallization: Al thickness = 34,000 Å minimum;
   Back (Cathode) metallization: Ti / Ni / Au thickness = 200 Å / 1,800 Å / 4,000 Å nominal.

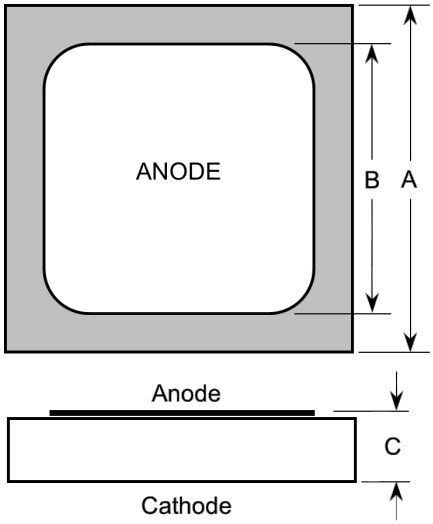
FIGURE 6. Physical dimensions JANHC and JANKC die (B versions).



Ltr	Dimensions			
	inch	inch	mm	mm
	Min	Max	Min	Max
A	.023	.027	0.584	0.686
B	.015	.019	0.381	0.483
C	.008	.012	0.203	0.305

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The physical characteristics of the die are as follows:
   Top (anode) metallization: Al thickness: 34,000 Å minimum.
   Back (cathode) metallization: Ti / Au thickness: Ti / Au (200 Å / 4,350 Å) nominal.

FIGURE 7. Physical dimensions JANHC and JANKC die (D versions).



Ltr	Dimensions			
	inch	inch	mm	mm
	Min	Max	Min	Max
A	.011	.015	0.28	0.38
B	.005	.009	0.13	0.23
C	.006	.010	0.15	0.25

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The physical characteristics of the die are:
   Top (anode) metallization: Al Thickness: 20,000 Å minimum.
   Back (cathode) metallization: Au: Thickness: 8,000 Å) nominal.

FIGURE 8. Physical dimensions JANHC and JANKC die (E versions).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

IS	Infinite sink mount.
$R_{\theta JSP(IS)}$	Thermal resistance junction to solder pads (infinite sink mount to PCB).
T_{EC}	Temperature of end-cap.
$T_{SP(IS)}$	Temperature of solder pads (infinite sink mount to PCB).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500 and herein: Axial leaded (DO -35) in accordance with figure 1, US in accordance with figure 2, four pad surface mount case outline UB in accordance with figure 3, three pad surface mount case outline UB2 in accordance with figure 4, and unencapsulated die in accordance with figures 5, 6, 7, and 8 for device types, JANHC and JANKC.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Diode construction.

3.4.2.1 Axial leaded and round body surface mount. All devices shall be metallurgically bonded, thermally matched, non-cavity, double-plug construction in accordance with MIL-PRF-19500 and herein.

3.4.2.1.1 Metalurgical bond for diodes with V_Z greater than 6.8 V dc. Category I bonds, as defined in accordance with MIL-PRF-19500 shall be utilized.

3.4.2.1.2 Metalurgical bond for diodes with V_Z less than or equal to 6.8 V dc. Category I or category III bonds, as defined in accordance with MIL-PRF-19500, shall be utilized.

3.4.2.2 Bottom solder pad surface mount. The UB and UB2 version devices die shall be eutectically mounted and wire bonded in a ceramic package.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. Manufacturer's identification and date code shall be marked on the devices. Initial container package marking shall be in accordance with MIL-PRF-19500. The prefixes JAN, JANTX, or JANTXV can be abbreviated as J, JX, or JV, respectively. (Example: The PIN for a square end-cap axial body surface mount device may be reduced to from JANTXV1N6309CUS to JV6309C). All marking which is omitted from the body of the device, except for polarity and serial numbers, shall appear on the initial container.

3.5.1 Polarity. For axial leaded devices, the polarity shall be indicated with a contrasting color band to denote the cathode end. For surface mount (US) devices, a minimum of three evenly spaced contrasting color dots around the periphery of the cathode end may be used. For 'UB' and 'UB2' devices, no polarity marking is required. No color coding will be permitted.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, table I, table II, table III, and table IV.

3.6.1 Maximum and primary test ratings. Maximum and primary test ratings for voltage regulator diodes are specified in table III herein.

3.6.2 Selection of tight tolerance devices. The C and D suffix devices shall be selected from JAN, JANTX, JANTXV, and JANS devices which have successfully completed all applicable screening, and table I, table II, and table III testing herein as 5-percent tolerance devices. All sublots of C and D suffix devices shall pass table I, subgroup 2, at tightened tolerances. Tighter tolerances for mounting clip temperature shall be maintained for reference purposes to establish correlation. For C and D tolerance levels, T_L = 25°C, +1°C, -3°C at .375 inch (9.53 mm) from body, or zero inches for surface mount devices or equivalent.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I and table II herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

d. Element evaluation of unencapsulated die (see 4.6).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and herein. Lot accumulation period shall be 3-months in lieu of 6-weeks.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or requalification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot to this revision to maintain qualification.

4.2.2 JANHC and JANKC devices. JANHC and JANKC devices shall be qualified in accordance with appendix G of MIL-PRF-19500.

4.3 Screening (JANTXV, JANTX, and JANS levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. Specified electrical measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTXV and JANTX level
(1) 3c	Required (see 4.3.1)	Required (see 4.3.1)
4	Not applicable	Not applicable
5	Applicable in UB and UB2 devices	Not applicable
6	Not applicable	Not applicable
8	Required	Not required
9	Required on nom V_Z > 10 V I_{R1}, V_{Z2} and Z_Z	Not applicable
10	Required on nom V_Z > 10 V	Not applicable
11	Required I_{R1}, V_{Z2}; ΔI_{R1} ≤ 100 percent of value or 50 nA dc, whichever is greater. ΔV_{Z2} ≤ ±1 percent of initial value	Required I_{R1} and V_{Z2}
12	Required, see 4.3.2	See 4.3.2
13	Required Scope display, see 4.5.7 Subgroup 2 and 3 of table I herein; ΔI_{R1} ≤ 100-percent of initial reading or 50 nA whichever is greater; ΔV_{Z2} ≤ 1 percent of initial reading	Subgroup 2 of table I herein; ΔI_{R1} ≤ 100 percent of initial reading or 50 nA whichever is greater; ΔV_{Z2} ≤ 1 percent of initial reading
15	Required	Not required
16	Required	Not required

(1) Shall be performed anytime after temperature cycling, screen 3a; TX and TXV do not need to be repeated in screening requirements.

4.3.1 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 as applicable of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate) see table II, subgroup 4 (see figures 15, 16, 17, 18, and 19).

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows (see 4.5.8): $I_{Z(min)}$ = 100 percent of column 7 of table IV. Test conditions in accordance with method 1038 of MIL-STD-750, condition B. Adjust I_Z or T_A to achieve the required T_J. T_J = 125°C minimum. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) or table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein. Delta measurements shall be in accordance with table III herein.

4.4.2.1 Quality level JANS (table E-VIA of MIL-PRF-19500).

Subgroup	Method	Condition
B3	1056	0°C to +100°C, 25 cycles, n = 22, c = 0.
B3	1051	-55°C to +175°C, 100 cycles, n = 22, c = 0.
B3	4066	Condition A, T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750. I_{ZSM} = column 9 of table IV herein (shall be performed on each sublot).
B3	1071	Fine leak and gross leak shall be performed for UB/UB2 suffix devices. Test condition E shall be performed for non-UB/UB2 suffix devices. NOTE: For non-transparent devices, hermetic seal test may be performed after electrical measurements.
B3	2101	Decap analysis scribe and break only. Not applicable for UB and UB2 devices.
B3	2075	For UB and UB2 only.
B4	1037	I_Z = shall be equal to 100 percent of column 7 of table IV minimum, 2,000 cycles.
B5	1027	I_Z = 100 percent of column 7 of table IV minimum for 96 hours; adjust T_A or I_Z to achieve T_J minimum. Option 1: T_J = +275°C minimum; t = 96 hours. n =22, c = 0. or Option 2: T_J = +175°C minimum; t = 1,000 hours. n = 45, c = 0.

4.4.2.2 Quality levels JAN, JANTX and JANTXV (table E-VIB of MIL-PRF-19500).

Subgroup	Method	Condition
B2	1056	0°C to +100°C, 10 cycles, n = 22, c = 0.
B2	1051	-55°C to +175°C, 25 cycles, n = 22, c = 0.
B2	1071	Fine leak and gross leak shall be performed for UB/UB2 suffix devices. Test condition E shall be performed for non-UB/UB2 suffix devices. NOTE: For non-transparent devices, hermetic seal test may be performed after electrical measurements.
B3	1027	$I_{Z(min)}$ shall be equal to 100 percent of column 7 of table IV minimum. Adjust T_A or I_Z to achieve T_J = 150°C minimum (see 4.5.8).
B3	2101	Decap analysis scribe and break only. Not applicable for UB and UB2 devices.
B3	2075	For UB and UB2 only.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Delta measurements shall be in accordance with table III herein.

Subgroup	Method	Condition
C2	1056	0°C to +100°C, 10 cycles, n = 22, c = 0.
C2	2036	Axial leaded devices: (Not applicable to US, UB and UB2 suffix devices) Tension: Condition A; 6 pounds (2.72 Kg); t = 15 seconds ±3 s. Lead fatigue: Condition E, 8 ounces (0.227 Kg), t = 15 seconds ±3 s.
C2	2038	US devices: Condition B; 6 pounds (2.72 Kg); t = 15 seconds ±3 s. Not applicable for UB and UB2 packaged devices.
C2	1071	Fine leak and gross leak shall be performed for UB/UB2 suffix devices. Test condition E shall be performed for non-UB/UB2 suffix devices. NOTE: For non-transparent devices, hermetic seal test may be performed after electrical measurements.
C5	4081	$R_{\theta JL}$;see 1.4.g; $R_{\theta JEC}$; n = 22, c = 0 (see 4.3.1), see 1.4.h.
C6	1027	$I_{Z(min)}$ shall be equal to 100 percent of column 7 of table IV. Adjust T_A or I_Z to achieve T_J = 150°C minimum (see 4.5.8).
C7		Not applicable.
C8	4071	(For JAN, JANTX, and JANTXV only); I_{Z2} = column 4 of table IV; T_1 = +25°C ±5°C, T_2 = +125°C (see 4.5.5); α_{VZ} = col. 14 of table IV; n = 22 devices, c = 0.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Delta measurements shall be in accordance with table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Surge current (I_{ZSM}). The peak currents shown in column 9 of table IV shall be applied in the reverse direction and these shall be superimposed on the current (I_Z = column 4 of table IV); a total of five (5) surges at 1 minute intervals. Each individual surge shall be one-half square-wave-pulse of 8.3 ms duration, or an equivalent sine wave, with the same effective rms current. T_A = +25°C ±5°C.

4.5.3 Regulator voltage measurements. The test current shall be applied until thermal equilibrium is attained (90 ±2 seconds minimum) prior to reading the breakdown voltage. For this test, the diode shall be suspended by its leads with mounting clips whose inside edge is located at .375 inch (9.53 mm) from the body and the mounting clips shall be maintained at a temperature of +25°C +8°C, -2°C. US suffix devices shall be mounted at the end-caps (lead length = 0 inch). This measurement may be performed after a shorter time following application of the test current than that which provides thermal equilibrium if correlation to stabilized readings can be established to the satisfaction of the qualifying activity.

4.5.4 Voltage regulation. For values of V_{Z2} (nominal) from 6.8 V dc to 200 V dc, current at 10 percent of I_{ZM} (column 7 of table IV) shall be maintained for a period of 90 ±5 seconds, and then V_Z shall be recorded. The current shall then be increased to 50 percent of I_{ZM} (column 7 of table IV) and maintained for a period of 90 ±5 seconds, then V_Z shall be recorded. The voltage change shall not exceed the applicable limits as shown in column 8 of table IV. During this test, the diode shall be suspended by its leads with mounting clips whose inside edge is located between .375 inch (9.53 mm) and .500 inch (12.70 mm) from the device body and the mounting clips shall be maintained at a temperature of +25°C +8°C, -2°C. US suffix devices shall be mounted by the end-caps. For values of V_{Z2} (nominal) from 2.4 V dc to 6.2 V dc, the lower test current shall be 2 mA dc and the higher current shall be 20 mA dc.

4.5.5 Temperature coefficient of regulator voltage (α_{VZ}). The device shall be temperature stabilized with current applied prior to reading regulator voltage at the specified ambient temperature.

4.5.6 Noise density. Noise density shall be measured using a noise density test circuit as shown on figure 9. Place a low-noise resistor, equivalent in value to the dynamic impedance of the device under test (DUT), in the test clips and adjust test current (I_{ZT}) to 400 µA dc and measure output noise voltage. Remove the resistor, insert DUT in test clips, readjust test current to 400 µA dc and measure output noise voltage again. To obtain noise density (ND), subtract rms resistor output noise voltage from rms diode output noise voltage and divide by product of overall system gain and square root of bandwidth. All measurements shall be made at +25°C.

4.5.7 Scope display evaluation. Scope display evaluation shall be in accordance with condition A (stable) of method 4023 of MIL-STD-750. Scope display in table I, subgroup 4 shall be performed on a scope. The reverse current over the knee shall be 500 µA peak.

4.5.7.1 Scope display option. At the suppliers option, 100-percent scope display evaluation may be discontinued after three consecutive lots are 100-percent tested with zero failures. Any table I failure shall require 100-percent scope display testing be reinstated.

4.5.8 Free air power burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each DUT still sees the full P_T (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. Use method 3100 of MIL-STD-750 to measure T_J.

4.6 Element evaluation of unencapsulated die. The element evaluation of unencapsulated die shall be in accordance with appendix G of MIL-PRF-19500. The test of subgroups 3 and higher shall be performed in any convenient package. For subgroup 4, the burn-in duration for the JANKC level shall follow the JANS requirements and the JANHC shall follow the JANTX requirements.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit 2/	Limit 2/	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance	3101	See 4.3.1	$Z_{\theta JX}$			°C/W
Forward voltage	4011	Condition B, I_F = 1 A dc, pulsed (see 4.5.1)	V_F		1.4	V dc
Reverse current leakage	4016	Condition A or B, V_R = column 10 of table IV	I_{R1}		Column 11	µA dc
Regulator voltage (see 4.5.3)	4022	I_{Z1} = 250 µA dc	V_{Z1}	Column 3		V dc
Regulator voltage (see 4.5.3)	4022	I_{Z2} = column 4 of table IV	V_{Z2}	Column 2 -5, -2, -1 percent	Column 2 +5, +2, +1 percent	V dc
Subgroup 3						
High-temperature operation		T_A = +150°C				
Reverse current	4016	Condition A or B, V_R = column 10 of table IV	I_{R2}		Column 12	µA dc
Subgroup 4						
Small-signal reverse breakdown impedance	4051	I_Z = column 4 of table IV, I_{SIG} = 10 percent of I_{Z2}	Z_{ZT}		Column 5	ohms
Knee impedance	4051	I_{ZK} = 250 µA dc, I_{SIG} = 25 µA rms	Z_{ZK}		Column 6	ohms
Noise density (see 4.5.6)		I_{Z1} = 400 µA dc	N_D		Column 13	$\mu V/\sqrt{Hz}$

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit 2/	Limit 2/	Unit
	Method	Conditions		Min	Max	
Subgroup 4 – continued						
Scope display evaluation	4023	Condition A See 4.5.7, n = 116, c = 0				
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	Condition A, (see 4.5.2); I_{ZSM} = column 9 of table IV herein (shall be performed on each sublot)				
Electrical measurements		See table I, subgroup 2 herein				
Subgroup 7						
Not applicable						
Subgroup 8		n = 22, c = 0				
Voltage regulation		See 4.5.4	$V_{Z(reg)}$		Column 8	V dc
Temperature coefficient of regulator voltage	4071	JANS level, I_Z = column 4 of table IV, T_1 = +25°C ±5°C; T_2 = +125°C (see 4.5.5)	α_{VZ}		Column 14	%/°C

1/ For sampling plan, see MIL-PRF-19500.
2/ Column references are to table IV herein.

TABLE II. Group E inspection qualification and requalification (all product assurance levels).

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 1			n = 22, c = 0
Thermal shock	1056	20 cycles, condition D except low temperature shall be achieved using liquid nitrogen (-195°C). Perform a visual examination for cracked glass	
Electrical measurements		See table I, subgroup 2	
Subgroup 2			n = 22, c = 0
Intermittent operating life	1037	$I_Z = I_{ZM}$ (column 7 of table IV) at T_A = room ambient for 10,000 cycles. No forced air cooling on the device shall be permitted	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500	Sample size N/A
Subgroups 5 and 6			
Not applicable			
Subgroup 7			n = 45
Resistance to glass cracking	1057	Step stress to destruction by increased cycles or up to a maximum of 25 cycles	

TABLE III. Group B, and C electrical and delta end-point measurements. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limit 5/	Limit 5/	Unit
		Method	Conditions		Min	Max	
1.	Thermal impedance	3101	See 4.3.1	$\Delta Z_{\theta JX}$		10 percent of initial reading max.	°C/W
2.	Regulator voltage	4022	I_Z = column 4 of table IV (see 4.5.3)	ΔV_{Z2}	±1 percent of initial value.		
3.	Reverse current	4016	Condition A or B, V_R = column 10 of table IV	ΔI_{R1}	100 percent of initial value or 50 nA dc, whichever is greater.		
4.	Small-signal breakdown impedance	4051	I_Z = column 4 of table IV, I_{SIG} = 10 percent of I_Z	ΔZ_Z	±35 percent of initial value or 2 ohms, whichever is greater.		

1/ Devices which exceed the table I limits herein shall not be accepted.
2/ The electrical measurements for Group B Inspections in table E-VIA (JANS) of MIL-PRF-19500 are as follows:
Subgroup 3, see table III herein, steps 1, 2, 3, and 4.
3/ The electrical measurements for Group B Inspections in table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500 are as follows:
a. Subgroup 2, see table III herein, steps 1 and 2.
b. Subgroup 3, see table III herein, steps 2.
4/ The electrical measurements for Group C Inspections in table E-VII of MIL-PRF-19500 are as follows:
Subgroup 2, see table III herein, steps 1 and 2.
5/ Column references are to table IV herein.

TABLE IV. Characteristics and ratings.

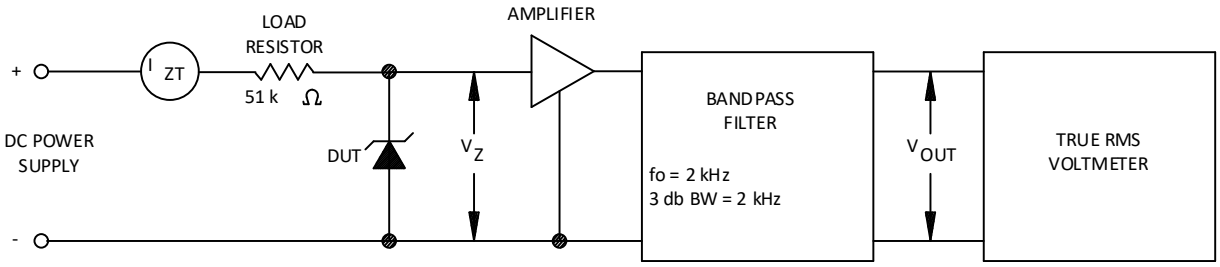
Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14
Type	V_{Z2} nom at I_{Z2} 1/	V_{Z1} min at I_{Z1} 250 µA	I_{Z2} test current	Z_{ZT} at I_{Z2}	Z_{ZK} at 250 µA	I_{ZM}	$V_{Z(reg)}$	I_{ZSM} surge 2/	V_R	I_{R1} at +25°C	I_{R2} at T_A = +150°C	N_D at 400 µA 1-3 kHz	αvz
	V	V	mA	Ω	Ω	mA	V	A	V	µA	µA	$\mu v\sqrt{Hz}$	%/°C
1N6309	2.4	1.1	20	30	1,200	177	1.50	2.50	1.0	100	200	1	-.085
1N6310	2.7	1.2	20	30	1,300	157	1.50	2.20	1.0	60	150	1	-.080
1N6311	3.0	1.3	20	29	1,400	141	1.50	2.00	1.0	30	100	1	-.075
1N6312	3.3	1.5	20	27	1,400	128	1.60	1.80	1.0	5	20	1	-.070
1N6313	3.6	1.8	20	25	1,400	117	1.60	1.65	1.0	3	12	1	-.065
1N6314	3.9	2.0	20	23	1,700	108	1.60	1.50	1.0	2	12	1	-.060
1N6315	4.3	2.4	20	20	1,700	99	0.90	1.40	1.0	2	12	1	-.045 +.020
1N6316	4.7	2.8	20	17	1,700	90	0.50	1.27	1.5	5	12	1	-.028 +.032
1N6317	5.1	3.3	20	14	1,300	83	0.40	1.17	2.0	5	12	1	-.020 +.035
1N6318	5.6	4.3	20	8	1,200	76	0.40	1.10	2.5	5	10	2	+.050
1N6319	6.2	5.2	20	3	800	68	0.30	0.97	3.5	5	10	5	+.060
1N6320	6.8	6.0	20	3	400	63	0.35	1.23	4.0	2	50	5	+.062
1N6321	7.5	6.6	20	4	400	57	0.40	1.16	5.0	2	30	5	+.068
1N6322	8.2	7.5	20	5	400	52	0.40	1.07	6.0	1	10	20	+.075
1N6323	9.1	8.4	20	6	500	47	0.50	0.97	7.0	1.00	10	40	+.076
1N6324	10.0	9.1	20	6	500	43	0.50	0.89	8.0	1.00	10	80	+.079
1N6325	11.0	10.0	20	7	550	39	0.50	0.83	8.5	1.00	10	100	+.082
1N6326	12.0	11.0	20	7	550	35	0.55	0.77	9.0	1.00	10	100	+.083
1N6327	13.0	11.9	12	8	550	33	0.55	0.71	9.9	0.05	10	100	+.083
1N6328	15.0	13.8	8.5	10	600	28	0.70	0.62	11.0	0.05	10	100	+.084
1N6329	16.0	14.7	7.8	12	600	27	0.75	0.58	12.0	0.05	10	100	+.084
1N6330	18.0	16.6	7.0	14	600	24	0.85	0.52	14.0	0.05	10	100	+.085
1N6331	20.0	18.5	6.2	18	500	21	0.95	0.47	15.0	0.05	10	100	+.086
1N6332	22.0	20.4	5.6	20	500	19	1.05	0.43	17.0	0.05	10	100	+.087
1N6333	24.0	22.3	5.2	24	500	18	1.15	0.39	18.0	0.05	10	100	+.088
1N6334	27.0	25.2	4.6	27	500	16	1.30	0.35	21.0	0.05	10	100	+.090
1N6335	30.0	28.0	4.2	32	500	14	1.45	0.31	23.0	0.05	10	100	+.091
1N6336	33.0	30.9	3.8	40	600	13	1.60	0.28	25.0	0.05	10	100	+.092
1N6337	36.0	33.7	3.4	50	600	12.0	1.75	0.260	27.0	0.05	10	100	+.093
1N6338	39.0	36.6	3.2	55	700	11.0	1.90	0.240	30	0.05	10	100	+.094
1N6339	43.0	40.4	3.0	65	800	9.9	2.10	0.220	33	0.05	10	80	+.095

See footnote at end of table.

TABLE IV. Characteristics and ratings - Continued.

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14
Type	V_{Z2} nom at I_{Z2} 1/	V_{Z1} min at I_{Z1} 250 µA	I_{Z2} test current	Z_{ZT} at I_{Z2}	Z_{ZK} at 250 µA	I_{ZM}	$V_{Z(reg)}$	I_{ZSM} surge 2/	V_R	I_{R1} at +25°C	I_{R2} at T_A = +150°C	N_D at 400 µA 1-3 kHz	αvz
	V	V	mA	Ω	Ω	mA	V	A	V	µA	µA	$\mu v\sqrt{Hz}$	%/°C
1N6340	47.0	44.2	2.7	75	900	9.0	2.25	0.200	36	0.05	10	80	+.095
1N6341	51.0	48.0	2.5	85	1,000	8.3	2.50	0.180	39	0.05	10	80	+.096
1N6342	56.0	52.7	2.2	100	1,200	7.6	2.70	0.170	43	0.05	10	80	+.097
1N6343	62.0	58.4	2.0	125	1,300	6.8	2.90	0.150	47	0.05	10	80	+.099
1N6344	68.0	64.1	1.8	155	1,500	6.3	3.20	0.130	52	0.05	10	80	+.101
1N6345	75.0	70.8	1.7	180	1,600	5.7	3.40	0.125	56	0.05	10	80	+.103
1N6346	82.0	77.4	1.5	220	1,800	5.2	3.80	0.115	62	0.05	10	80	+.105
1N6347	91.0	86.0	1.4	270	2,100	4.7	4.20	0.100	69	0.05	10	80	+.108
1N6348	100.0	94.5	1.3	340	2,400	4.3	4.40	0.095	76	0.05	10	80	+.110
1N6349	110.0	104.0	1.1	500	2,800	3.9	4.80	0.085	84	0.05	10	80	+.110
1N6350	120.0	113.0	1.0	600	3,200	3.5	5.20	0.080	91	0.05	10	80	+.110
1N6351	130.0	122	0.95	850	4,100	3.3	5.60	0.070	99	0.05	10	80	+.110
1N6352	150.0	141	0.85	1,000	4,500	2.8	7.00	0.065	114	0.05	10	80	+.110
1N6353	160.0	151	0.80	1,200	5,000	2.7	7.50	0.060	122	0.05	10	80	+.110
1N6354	180.0	170	0.68	1,500	5,600	2.4	9.00	0.050	137	0.05	10	80	+.110
1N6355	200.0	189	0.65	1,800	6,500	2.1	12.00	0.045	152	0.05	10	80	+.110

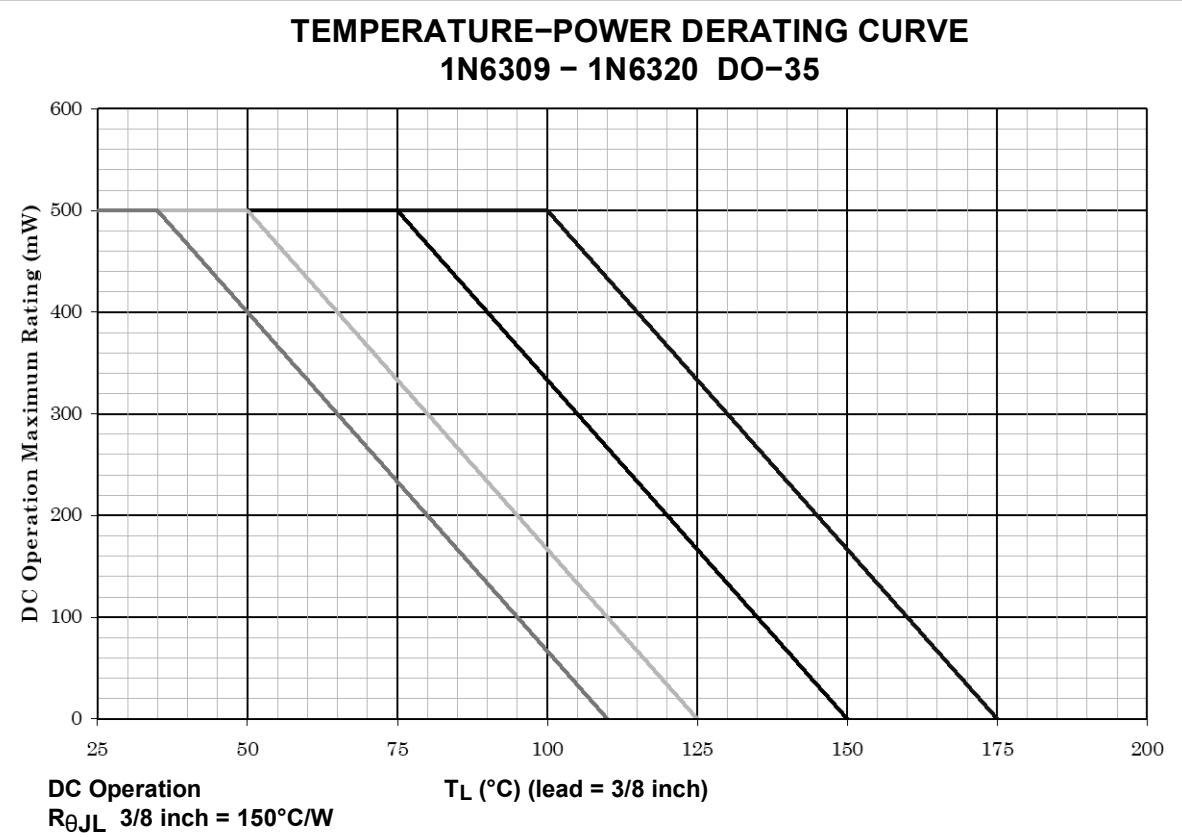
1/ 1N6309D through 1N6355D are 1 percent voltage tolerance. 1N6309C through 1N6355C are 2 percent voltage tolerance. 1N6309 through 1N6355 are 5 percent voltage tolerance.
2/ The surge energy should be reduced by 50% for all Zener chips encased in an UB package.



NOTES:

1. Input voltage and lead resistance should be high so that zener can be driven from a constant current source.
2. Input impedance of band pass filter should be high compared with the dynamic impedance of the DUT.
3. Filter bandwidth characteristics shall be as follows:
    a. fo = 2,000 Hz.
    b. Shape factor, -40 db to -3 db, approximately 2.
    c. Passband at the -3 db is 1,000 Hz ±50 Hz to 3,000 Hz ±150 Hz.
    d. Passband at the -40 db is 500 Hz ±50 Hz to 6,000 Hz ±600 Hz.

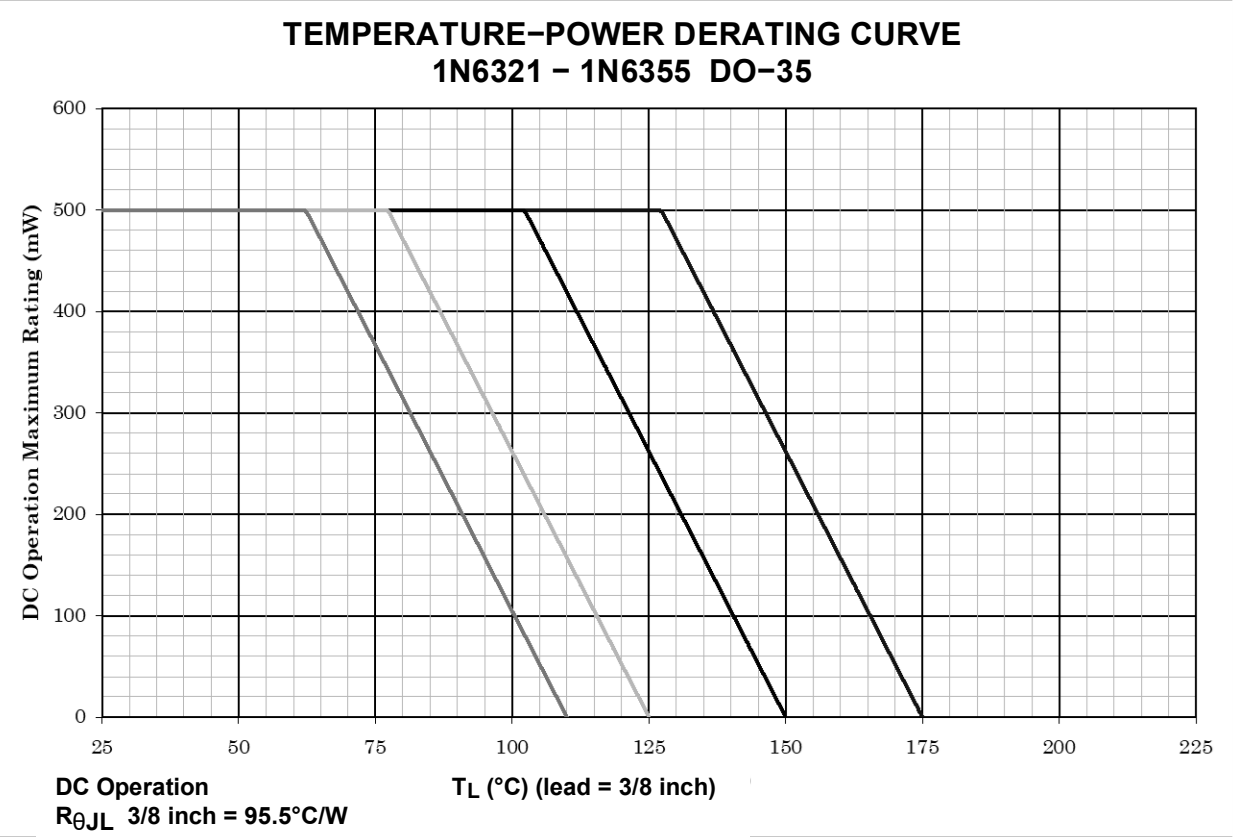
FIGURE 9. Circuit for determination of noise density.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified (see 1.3 herein).
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

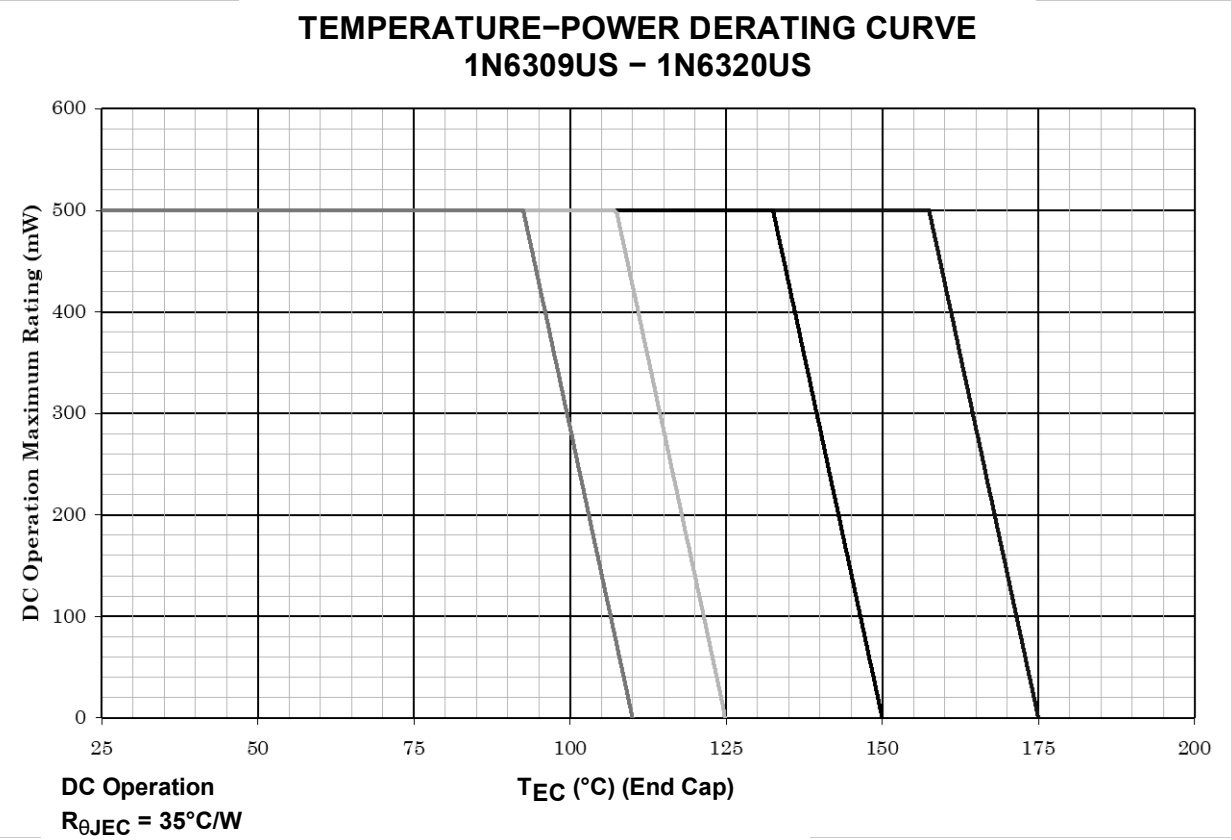
FIGURE 10. Temperature-power derating curve (T_L) 1N6309 through 1N6320 for axial leaded DO-35.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified (see 1.3 herein).
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

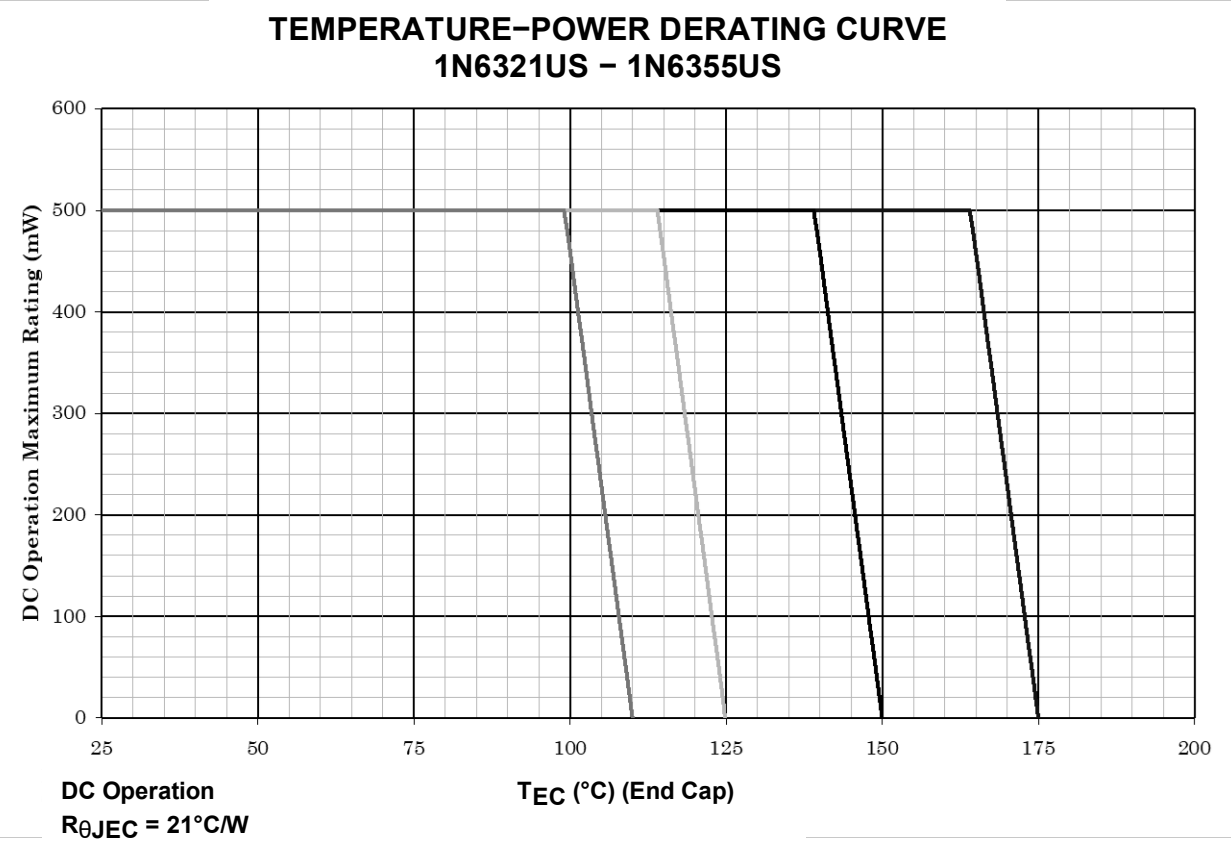
FIGURE 11. Temperature-power derating curve (T_L) for 1N6321 through 1N6355 for axial leaded DO-35.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified (see 1.3 herein).
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

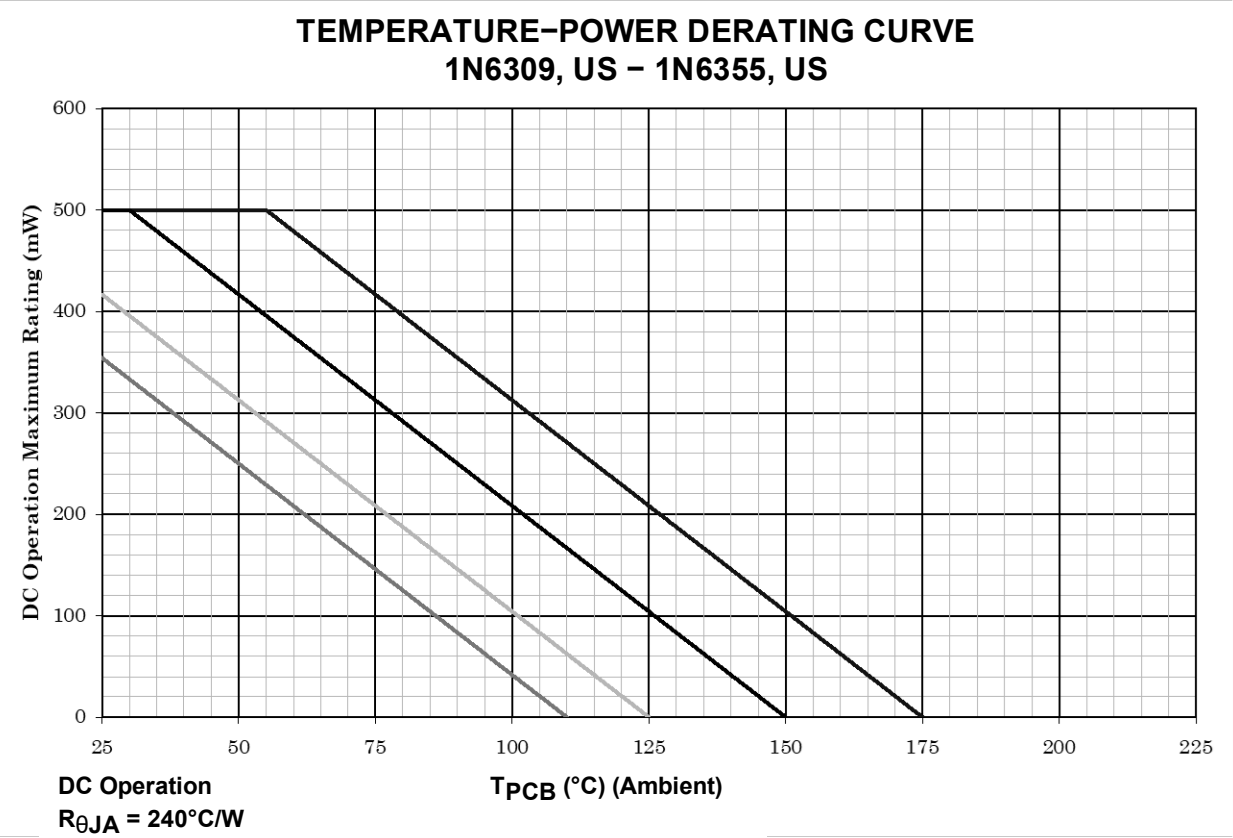
FIGURE 12. Temperature-power derating curve (T_{EC}) for 1N6309US through 1N6320US surface mount.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified (see 1.3 herein).
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

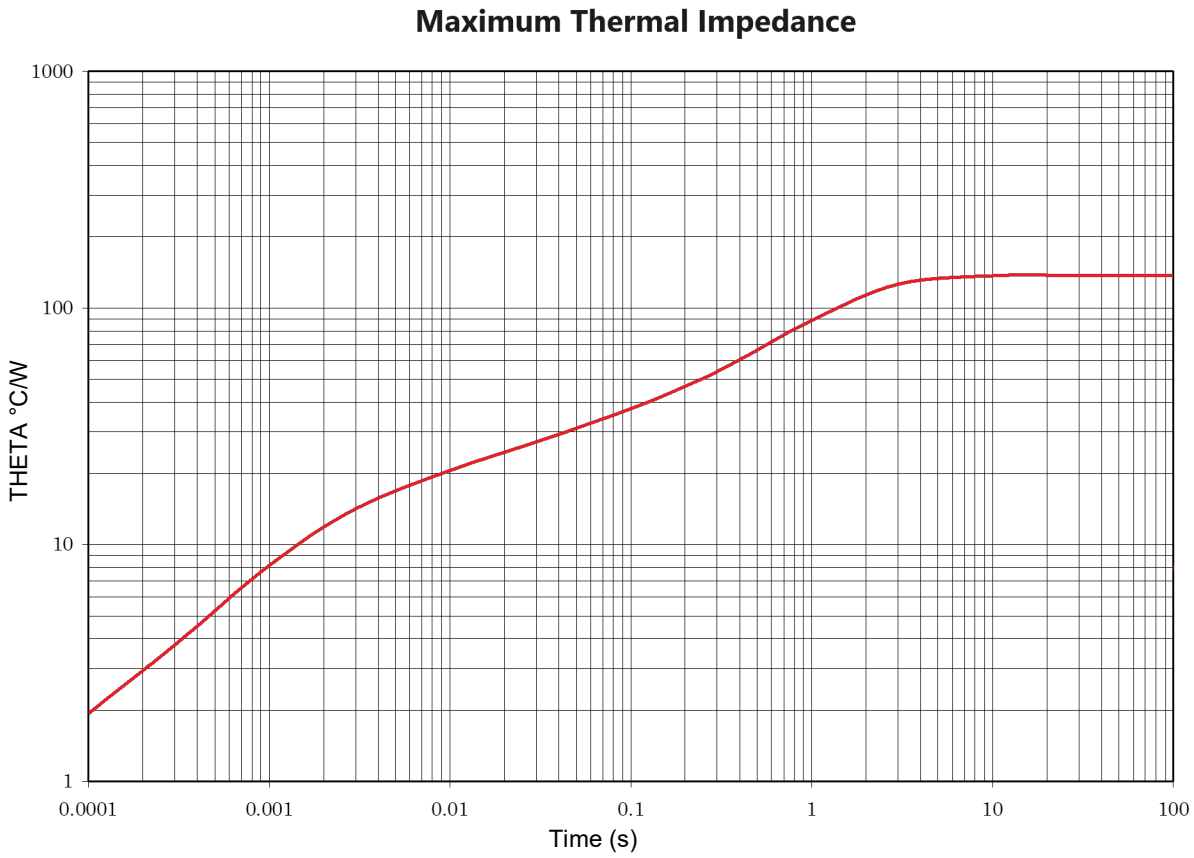
FIGURE 13. Temperature-power derating curve (T_{EC}) for 1N6321US through 1N6355US surface mount.



NOTES:

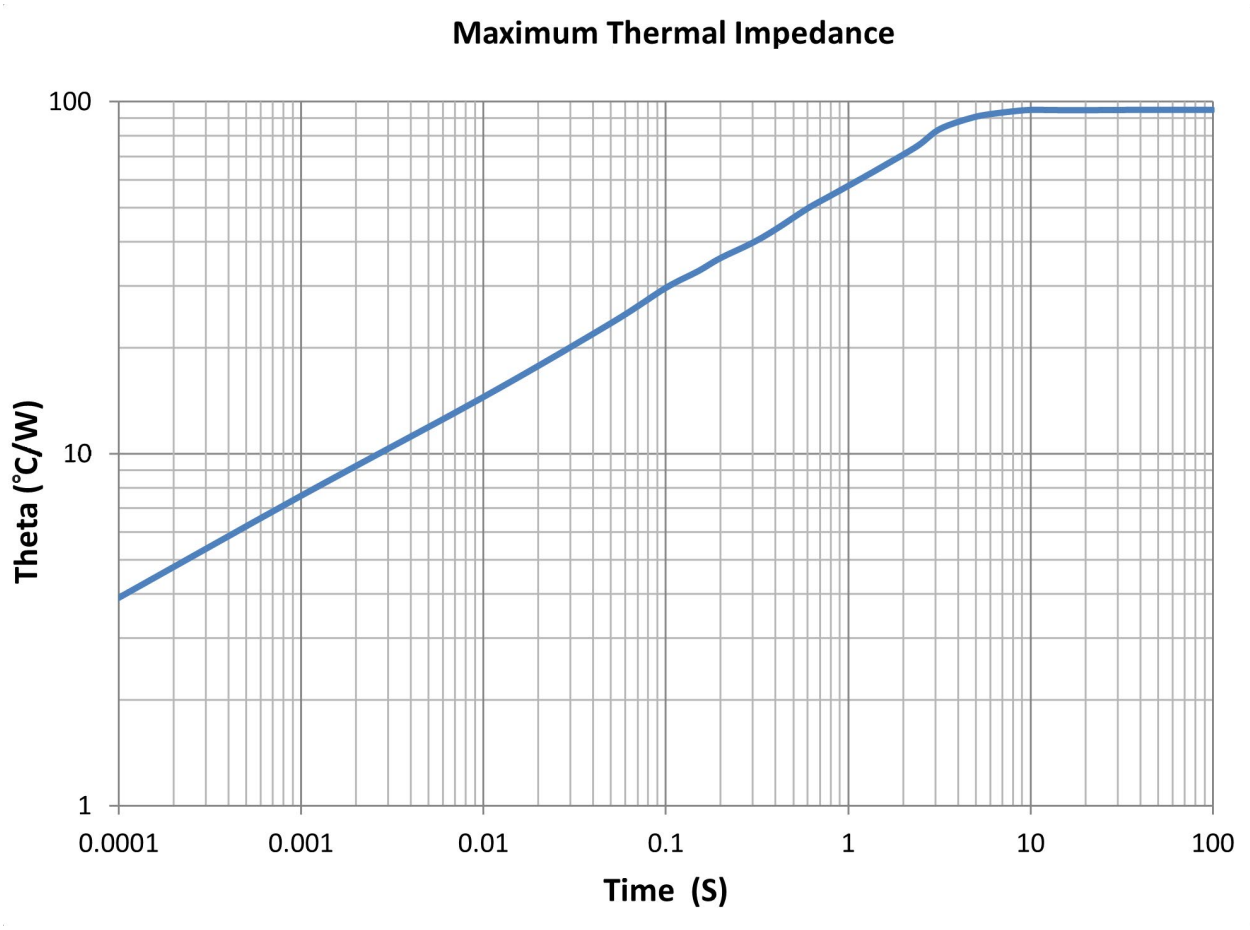
1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified (see 1.3 herein).
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show current rating where most users want to limit T_J in their application.

FIGURE 14. Temperature-power derating curve (T_{PCB}) for 1N6309US through 1N6355US surface mount.



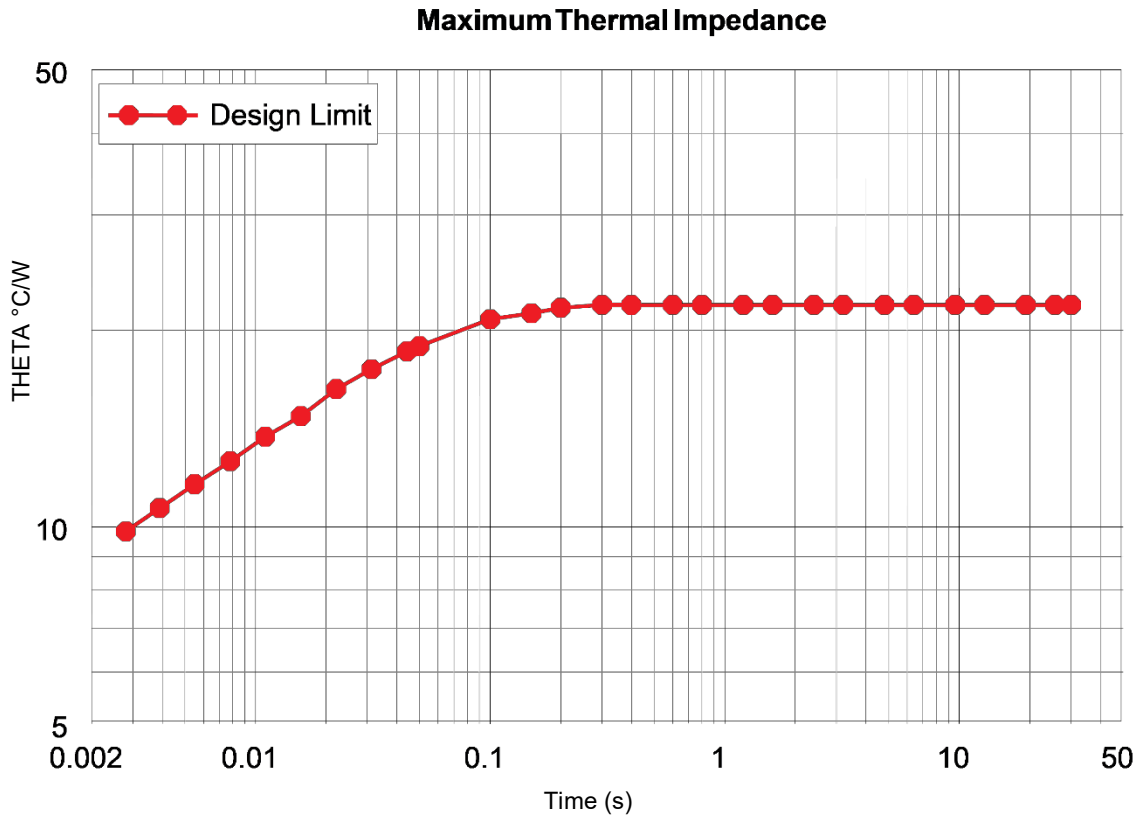
NOTES:
1. Thermal impedance $Z_{\theta JX}$ is measured at 10 ms.
2. Thermal resistance junction-to-lead = 150°C/W.

FIGURE 15. Thermal impedance graph for DO-35 devices 1N6309 through 1N6320.



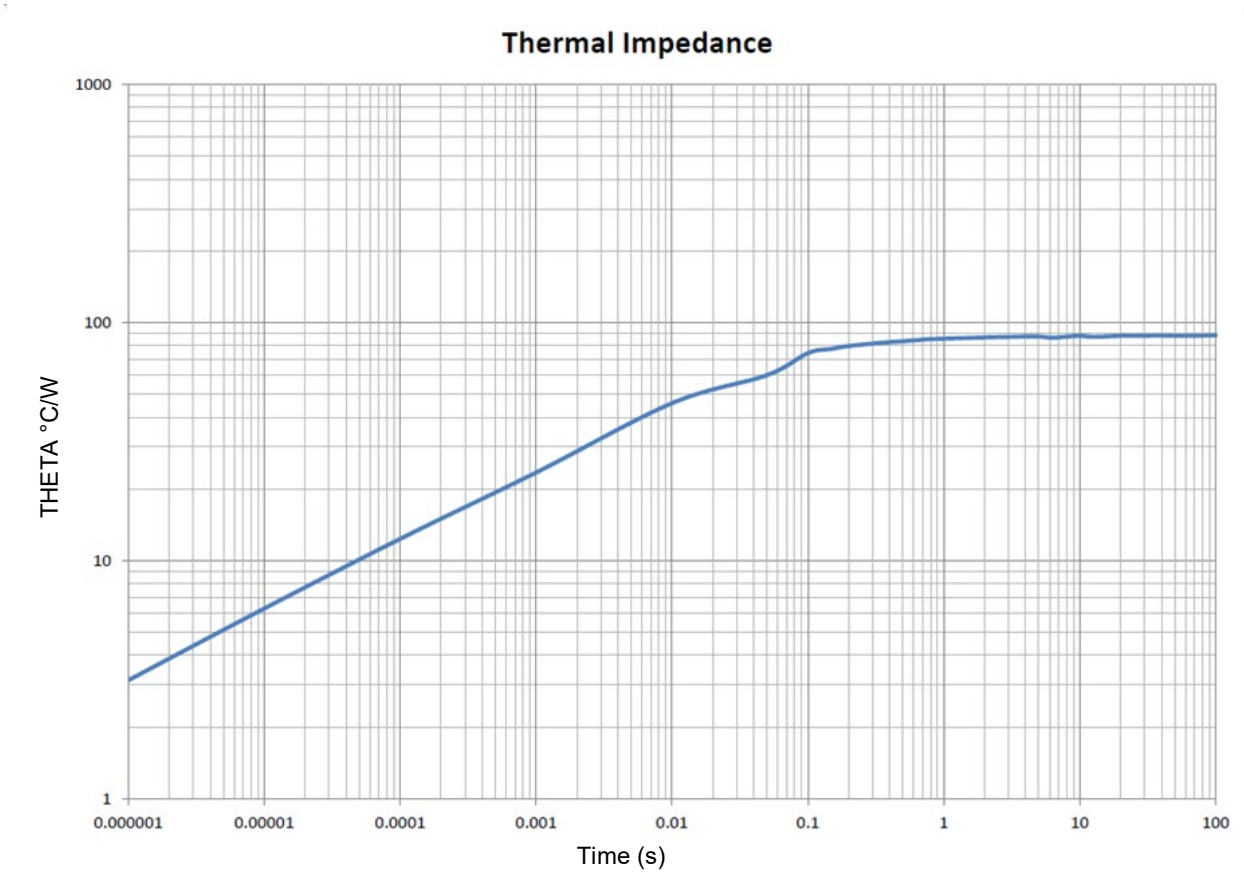
NOTES:
1. Thermal impedance $Z_{\theta JX}$ is measured at 10 ms.
2. Thermal resistance junction-to-lead = 95.5°C/W.

FIGURE 16. Thermal impedance graph for DO-35 devices 1N6321 through 1N6355.



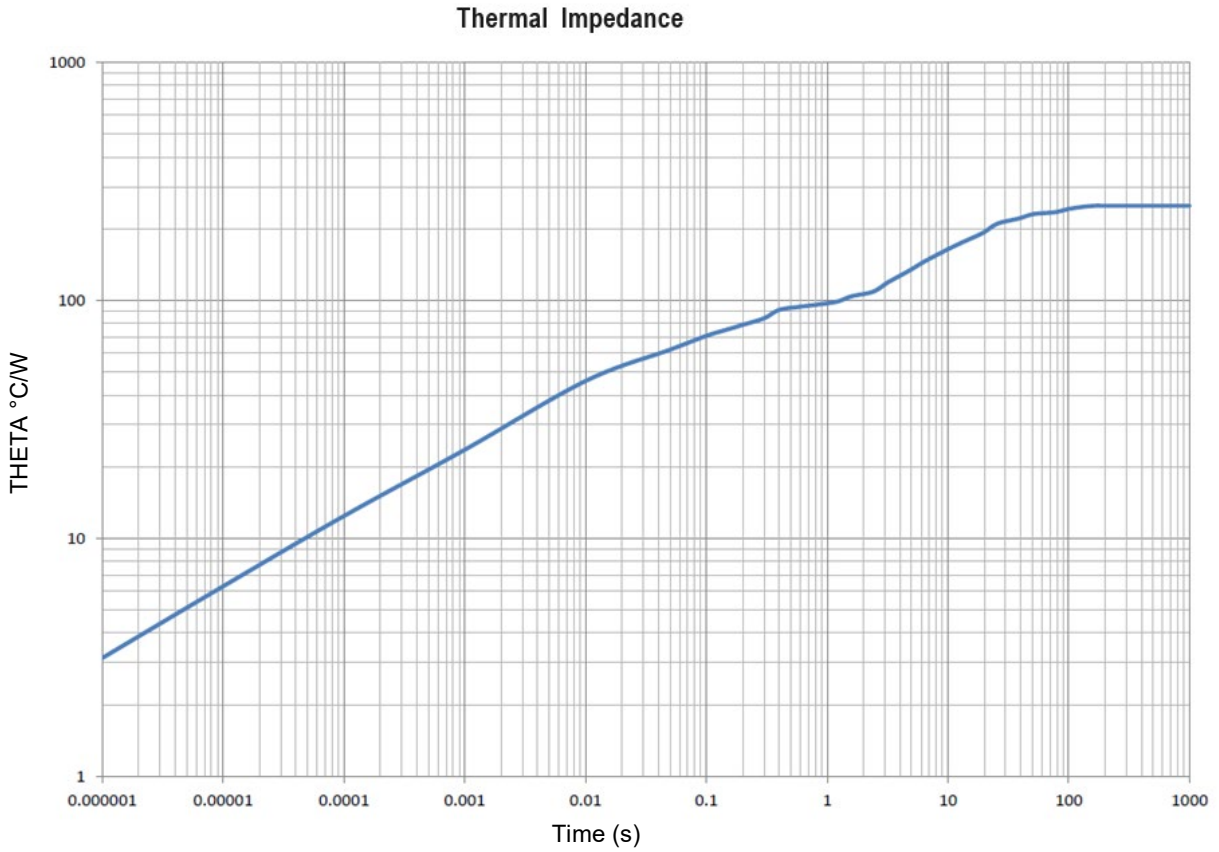
NOTES:
1. Thermal impedance $Z_{\theta JX}$ is measured at 10 ms.
2. Thermal resistance junction-to-lend cap $R_{\theta JEC}$ = 21°C/W.

FIGURE 17. Thermal impedance graph for US devices 1N6321US through 1N6355US.



NOTES:
1. Thermal impedance $Z_{\theta JX}$ = 45°C/W at 10 ms.
2. Thermal resistance junction-to-solder pad infinite sink, $R_{\theta JSP(IS)}$ = 90°C/W.

FIGURE 18. Thermal impedance graph (junction-to-solder pad infinite sink) for UB packages.



NOTES:
1. Thermal impedance $Z_{\theta JX}$ = 45°C/W maximum at 10 ms.
2. Thermal resistance junction-to-ambient (printed circuit board), $R_{\theta JA(PCB)}$ = 250°C/W.

FIGURE 19. Thermal impedance graph (junction-to-ambient) for UB packages.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

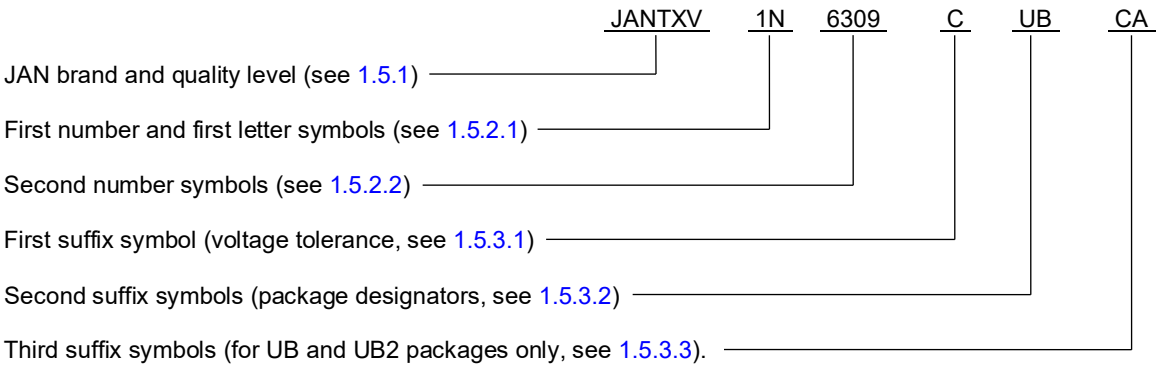
c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

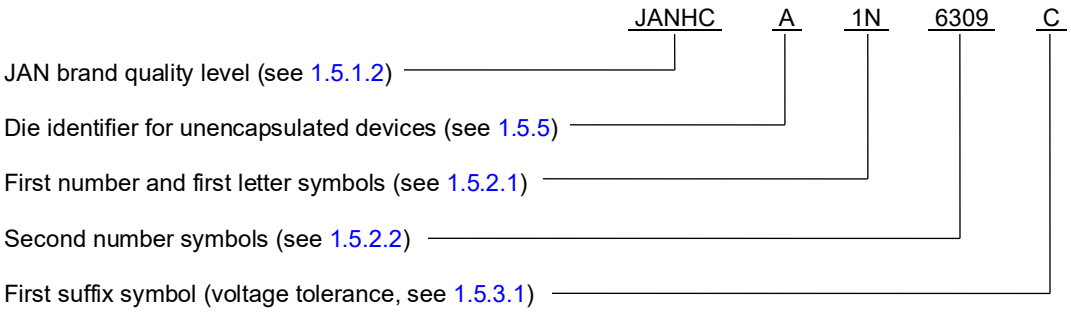
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Weapons Support, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.4.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.5 List of PINs.

6.5.1 Encapsulated device types. The following is a list of possible PINs available on this specification sheet.

PINs for types 1N6309, representing pins 1N6309 through 1N6355 (1) (2)

JAN1N6309	JANTX1N6309	JANTXV1N6309	JANS1N6309
JAN1N6309US	JANTX1N6309US	JANTXV1N6309US	JANS1N6309US
JAN1N6309UB	JANTX1N6309UB	JANTXV1N6309UB	JANS1N6309UB
JAN1N6309UB2	JANTX1N6309UB2	JANTXV1N6309UB2	JANS1N6309UB2
JAN1N6309UB2R	JANTX1N6309UB2R	JANTXV1N6309UB2R	JANS1N6309UB2R
JAN1N6309UBCA	JANTX1N6309UBCA	JANTXV1N6309UBCA	JANS1N6309UBCA
JAN1N6309UBCC	JANTX1N6309UBCC	JANTXV1N6309UBCC	JANS1N6309UBCC
JAN1N63093UBD	JANTX1N6309UBD	JANTXV1N6309UBD	JANS1N6309UBD

(1) Only device type 1N6309 is shown in this listing. Device type 1N6309 represents one of 47 device type number within the following range (1N6309 through 1N6355). Each device type is available with the any of the options listed in the table.
(2) All PINs listed represent only the ±5 percent voltage tolerance devices. A voltage tolerance suffix will be included immediately after the device type designation (1N6309) for those devices with tighter tolerances.

6.5.2 List of unencapsulated device types and suppliers of JANHC and JANKC die. The qualified JANHC and JANKC die suppliers with the applicable letter version (example JANHCA1N6309) will be identified on the QML.

JANHC and JANKC ordering information (1)			
PIN	Manufacture CAGE		
	43611	13409	52GC4
PINs for types 1N6309, representing pins 1N6309 through 1N6355	JANHCA1N6309 JANKCA1N6309	JANHCB1N6309 JANKCB1N6309 JANHCD1N6309 JANKCD1N6309	JANHCC1N6309 JANKCC1N6309 JANHCE1N6309 JANKCE1N6309

(1) 1N6309 represents one device type number within the following range (1N6309 through 1N6355).

6.6 Substitution information.

6.6.1 Substitutability of 2 percent and 1 percent tolerance devices. Devices of tighter tolerance are a direct one way substitute for the looser tolerance devices (example: JANTX1N6309D substitutes for JANTX1N6309).

6.6.2 Cross reference substitution list. Quality level S devices required for space flight applications are listed herein. A PIN for PIN replacement table for axial leaded packages is as follows and these devices are directly interchangeable.

JANS PINs that were specified within MIL-S-19500/533 dated 7 April 1981	JANS superseded PIN that were specified within MIL-S-19500/127J dated 8 May 1980	JANS PINs that were specified within MIL-S-19500/533 dated 7 April 1981	JANS superseded PIN that were specified within MIL-S-19500/127J dated 8 May 1980
1N6309, C, D	1N4370A-1, C-1 or D-1	1N6318, C, D	1N752A-1, C-1 or D-1
1N6310, C, D	1N4371A-1, C-1 or D-1	1N6319, C, D	1N753A-1, C-1 or D-1
1N6311, C, D	1N4372A-1, C-1 or D-1	1N6320, C, D	1N754A-1, C-1 or D-1
1N6312, C, D	1N746A-1, C-1 or D-1	1N6321, C, D	1N755A-1, C-1 or D-1
1N6313, C, D	1N747A-1, C-1 or D-1	1N6322, C, D	1N756A-1, C-1 or D-1
1N6314, C, D	1N748A-1, C-1 or D-1	1N6323, C, D	1N757A-1, C-1 or D-1
1N6315, C, D	1N749A-1, C-1 or D-1	1N6324, C, D	1N758A-1, C-1 or D-1
1N6316, C, D	1N750A-1, C-1 or D-1	1N6326, C, D	1N759A-1, C-1 or D-1
1N6317, C, D	1N751A-1, C-1 or D-1		

6.7 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC die suppliers with the applicable letter version (example JANHCA1N6309) will be identified on the QML.

JANHC and JANKC ordering information (1)			
PIN	Manufacture CAGE		
	43611	13409	52GC4
PINs for types 1N6309, representing pins 1N6309 through 1N6355	JANHCA1N6309 JANKCA1N6309	JANHCB1N6309 JANKCB1N6309 JANHCD1N6309 JANKCD1N6309	JANHCC1N6309 JANKCC1N6309 JANHCE1N6309 JANKCE1N6309

(1) 1N6309 represents one device type number within the following range (1N6309 through 1N6355). Each device type is available with the any of the options listed in the table.

6.8 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

CONCLUDING MATERIAL

Custodians:
Army − CR
Navy − SH
Air Force − 85
NASA − NA
DLA − CC

Review activities:
Navy − AS
Air Force − 19

Preparing activity:
DLA - CC

(Project 5961−2026−013)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.