

The documentation and process conversion measures necessary to comply with this document shall be completed by 18 December 2024.

INCH-POUND

MIL-PRF-19500/518E
w/AMENDMENT 1
18 July 2024
SUPERSEDING
MIL-PRF-19500/518E
24 May 2019

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, POWER,
TYPES 2N3766 AND 2N3767,
QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN silicon, power transistors. Three levels of product assurance (JAN, JANTX and JANTXV) are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The device package outline is a TO-213AA in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^{\circ}\text{C}$.

Type	P_T (1)	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}	$R_{\theta JC}$
	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>$^{\circ}\text{C}$</u>	<u>$^{\circ}\text{C/W}$</u>
2N3766	25	80	60	6	2	4	-65 to +200	7
2N3767	25	100	80	6	2	4	-65 to +200	7

(1) Between $T_C = +25^{\circ}\text{C}$ and $T_C = +200^{\circ}\text{C}$, linear derating factor (average) = 143 m/W $^{\circ}\text{C}$.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A
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FSC 5961



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1.4 Primary electrical characteristics.

Type	h _{FE2} (1)		h _{FE3} (1)		C _{obo}		h _{fe}		V _{BE(sat)}	
	V _{CE} = 5 V dc I _C = 500 mA dc		V _{CE} = 10 V dc I _C = 1 A dc		V _{CB} = 10 V dc I _E = 0 0.1 MHz ≤ f ≤ 1 MHz		V _{CE} = 10 V dc I _C = 500 mA dc f = 10 MHz		I _C = 1 A dc I _B = 0.1 A dc	
	Min	Max	Min	Max	Min pF	Max pF	Min	Max	Min V dc	Max V dc
2N3766	40	160	20			50	1	8		1.5
2N3767	40	160	20			50	1	8		1.5

Type	V _{CE(sat)1}		V _{CE(sat)2}		Switching			
	I _C = 1 A dc I _B = 0.1 A dc		I _C = 500 mA dc I _B = 50 mA dc		t _{on}		t _{off}	
					(see table 1 and figure 2 herein)			
	<u>Min</u> V dc	<u>Max</u> V dc	<u>Min</u> V dc	<u>Max</u> V dc	Min <u>μs</u>	Max <u>μs</u>	Min <u>μs</u>	Max <u>μs</u>
2N3766		2.5		1.0		0.25		2.5
2N3767		2.5		1.0		0.25		2.5

(1) Pulsed (see [4.5.1](#)).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

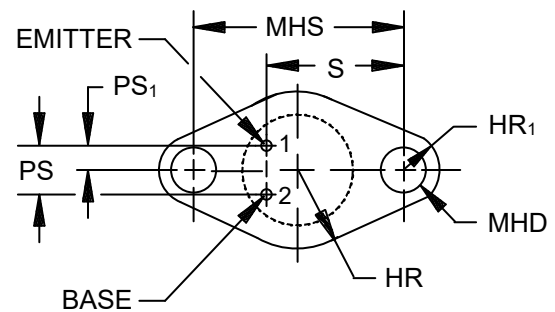
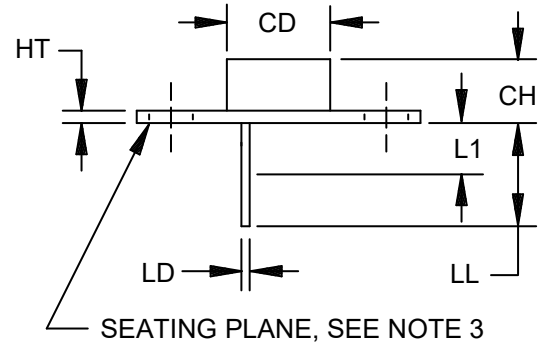
1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows: "3766" and "3767".

1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.620		15.76	4
CH	.250	.340	6.35	8.64	
HR		.350		8.89	5
HR ₁	.115	.145	2.92	3.68	5
HT	.050	.075	1.27	1.91	7
LD	.028	.034	0.71	0.86	8, 9
LL	.360	.500	9.14	12.70	8, 9
L ₁		.050		1.27	8, 9
MHD	.142	.152	3.61	3.86	6
MHS	.958	.962	24.33	24.43	
PS	.190	.210	4.83	5.33	10
PS ₁	.093	.107	2.36	2.72	10
S	.570	.590	14.48	14.99	



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Pin 1 is the emitter and pin 2 is the base. The collector shall be electrically connected to the case.
3. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .520 inch (13.20 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
4. Body contour is optional within zone defined by dimension CD.
5. The radius applies to two places, at both sides (dimension HR) or ends (dimension HR₁) of the package.
6. Applies to two holes, at both ends.
7. Dimension HT does not include sealing flanges.
8. Applies to both terminals.
9. Dimension LD applies between dimensions L₁ and LL. Lead diameter shall not exceed twice dimension LD within dimension L₁.
10. These dimensions should be measured at points .050 inch (1.27 mm) +.005 inch (0.13 mm) -.000 inch (0.00 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.

* FIGURE 1. Physical dimensions TO-213AA (formerly TO-66) package.

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the encapsulated devices shall be as shown on figure 1.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

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4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3)
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (quality levels JANTX and JANTXV only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANTX and JANTXV levels
3c (1)	Thermal impedance (see 4.3.2).
11	I_{CEX1} and h_{FE2} .
12	See 4.3.1.
13	Subgroup 2 of table I herein. ΔI_{CEX1} = 100 percent of initial value or 1 μA dc, whichever is greater; Δh_{FE2} = 25 percent of initial value.

- (1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions shall be as follows: $T_J = +187.5^\circ C \pm 12.5^\circ C$, $V_{CB} \geq 10$ V dc, $T_A \leq +35^\circ C$.

* 4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate).

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If the alternate procedure for screening of quality levels JANTX and JANTXV is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2, of table I herein, inspection only.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-IV of MIL-PRF-19500, and table I herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIC (small die flow) of MIL-PRF-19500 and herein.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1039	Steady-state power: Test condition B, 340 hours, $V_{CB} \geq 10$ V dc, $T_J = 175^\circ\text{C}$ min. No heat sink or forced-air cooling on the devices shall be permitted. $n = 45$ devices, $c = 0$.
2	1039	The steady-state power test of step 1 shall be extended to 1,000 hours for each die design. Samples shall be selected from a wafer lot every 12 months of wafer production; however, group B shall not be required more than once for any single wafer lot. $n = 45$, $c = 0$.
3	1032	High-temperature life (non-operating), $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$

4.4.2.1 Sample selection. Samples selected for small die flow group B inspection shall be in accordance with all of the following requirements:

- a. Samples shall be selected from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection.
- b. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (step 1) may be tested prior to the application of final lead finish.
- c. Separate samples may be used for each step.

4.4.2.2 Failures. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during small die flow group B inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A, weight = 10 lbs (4.54 kg), $t = 15$ seconds.
C5	3131	Thermal resistance, see 4.3.2, $R_{\theta JC(max)} = 7^\circ\text{C/W}$.
C6		Not applicable

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Coil selection for safe operating area (SOA) tests. In selecting coils for use in clamped and unclamped inductive SOA tests, prime consideration should be given to the commercially available coil. However, due to the extreme critical nature of the coil in these circuits and wide tolerance of some commercially available coils (+100 percent, -50 percent), it shall be the semiconductor manufacturer's responsibility to prove upon request compliance or equivalency of any coil used (commercial or in-plant designed) to be within (+20 percent, -10 percent) of the specified inductance at the rated current and dc resistance.

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TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u> 2/						
Visual and mechanical 3/ examination	2071					
Solderability 3/	2026					
Resistance to solvent 3/ 4/	1022					
Salt atmosphere 5/	1041					
Temp cycling 3/	1051	Test condition C, 25 cycles				
Hermetic seal	1071					
Fine leak						
Gross leak						
Electrical measurements		Group A, subgroup 2				
Bond strength 3/	2037					
<u>Subgroup 2</u>						
Thermal impedance 6/	3131	See 4.3.2	$Z_{\theta JC}$			°C/W
Collector to emitter breakdown voltage	3011	Bias condition D, $I_C = 100$ mA dc, pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N3766				60		V dc
2N3767				80		V dc
Collector to emitter cutoff current	3041	Bias condition D	I_{CEO}		500	μA dc
2N3766		$V_{CE} = 60$ V dc				
2N3767		$V_{CE} = 80$ V dc				
Emitter-base cutoff current	3061	Bias condition D, $V_{EB} = 6$ V dc	I_{EBO}		500	μA dc
Collector to emitter cutoff current	3041	Bias condition A, $V_{BE} = -1.5$ V dc	I_{CEX1}			
2N3766		$V_{CE} = 80$ V dc			10	μA dc
2N3767		$V_{CE} = 100$ V dc			10	μA dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Collector to base cutoff current 2N3766 2N3767	3036	Bias condition D $V_{CB} = 80 \text{ V dc}$ $V_{CB} = 100 \text{ V dc}$	I_{CBO}		10 10	$\mu\text{A dc}$ $\mu\text{A dc}$
Base to emitter non-saturated voltage	3066	Test condition B, $V_{CE} = 10 \text{ V dc}$, $I_C = 1.0 \text{ A dc}$, pulsed (see 4.5.1)	V_{BE}		1.5	V dc
Base to emitter saturated voltage	3066	Test condition A, $I_C = 1.0 \text{ A dc}$, $I_B = 0.1 \text{ A dc}$, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.5	V dc
Collector to emitter saturated voltage	3071	$I_C = 1.0 \text{ A dc}$, $I_B = 0.1 \text{ A dc}$, pulsed (see 4.5.1)	$V_{CE(sat)1}$		2.5	V dc
Collector to emitter saturated voltage	3071	$I_C = 0.5 \text{ A dc}$, $I_B = 0.05 \text{ A dc}$, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.0	V dc
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$, $I_C = 50 \text{ mA dc}$, pulsed (see 4.5.1)	h_{FE1}	30		
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$, $I_C = 500 \text{ mA dc}$, pulsed (see 4.5.1)	h_{FE2}	40	160	
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$, $I_C = 1 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE3}	20		
<u>Subgroup 3</u>						
High-temperature operation:		$T_A = +150^{\circ}\text{C}$				
Collector to emitter cutoff current 2N3766 2N3767	3041	Bias condition A, $V_{BE} = -1.5 \text{ V dc}$ $V_{CE} = 50 \text{ V dc}$ $V_{CE} = 70 \text{ V dc}$	I_{CEX2}		1.0 1.0	mA dc mA dc
Low-temperature operation:		$T_A = -55^{\circ}\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 5.0 \text{ V dc}$, $I_C = 0.5 \text{ A dc}$, pulsed (see 4.5.1)	h_{FE4}	13		

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Pulse response:	3251	Test condition A, except test circuit and pulse requirements in accordance with figure 2 herein. $V_{CC} = 30 \text{ V dc}$, $I_C = 0.5 \text{ A dc}$, $I_{B1} = 0.05 \text{ A dc}$	t_{on}		0.25	μs
Turn-on time						
Turn-off time						
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}$, $I_C = 500 \text{ mA dc}$, $f = 10 \text{ MHz}$	$ h_{fe} $	1	8	
Open capacitance (open circuit)	3236	$V_{CB} = 10 \text{ V dc}$, $I_E = 0$, $0.1 \text{ MHz} \leq f \leq 1.0 \text{ MHz}$	C_{obo}		50	pF
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}$, power application $t = 1 \text{ s}$, 1 cycle, (see figure 3)				
Test 1						
Test 2						
Test 3						
2N3766	3053	Load condition B, $T_A = +25^\circ\text{C}$, $V_{CC} = 20 \text{ V dc}$, $t_p \approx 1.5 \text{ ms}$, $R_{BB1} = 5 \text{ }\Omega$, (vary to obtain I_C), duty cycle ≤ 5 percent, $I_C \approx 4 \text{ A dc}$, $R_{BB2} = 100 \text{ }\Omega$, $V_{BB2} = 1.5 \text{ V dc}$, $V_{BB1} \approx 10 \text{ V dc}$, $L = 5 \text{ mH}$, at 4A, R of inductor = $.5 \text{ }\Omega$, and $R_{LOAD} = R$ of inductor 7/ Clamp voltage = 60 V dc Clamp voltage = 80 V dc Device fails if clamp voltage is not reached.				
2N3767						
Safe operating area (clamped switching)						
2N3766						
2N3767						
Electrical measurements		See table I , subgroup 2 herein, I_{CEX1} and h_{FE2} electrical tests				

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroups 6 and 7</u> Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For resubmission of failed subgroup A1, double the sample size of the failed test or sequence of tests.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

5/ Required only for laser marked devices using corrosion prone base metals for the marking surface.

6/ This test required for the following end-point measurements only:

Group B, all steps (JAN, JANTX, and JANTXV).

Group C, subgroup 2.

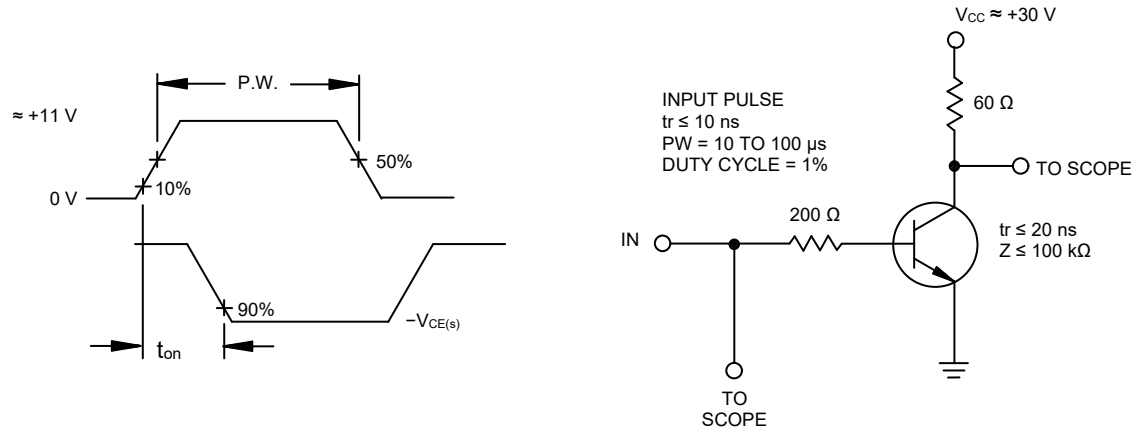
Group E, subgroup 1.

7/ L = 5 mH (2 each Essex Stancor C-2688 in parallel 1 A, 0.5 ohm, or equivalent (see [4.5.2](#)).

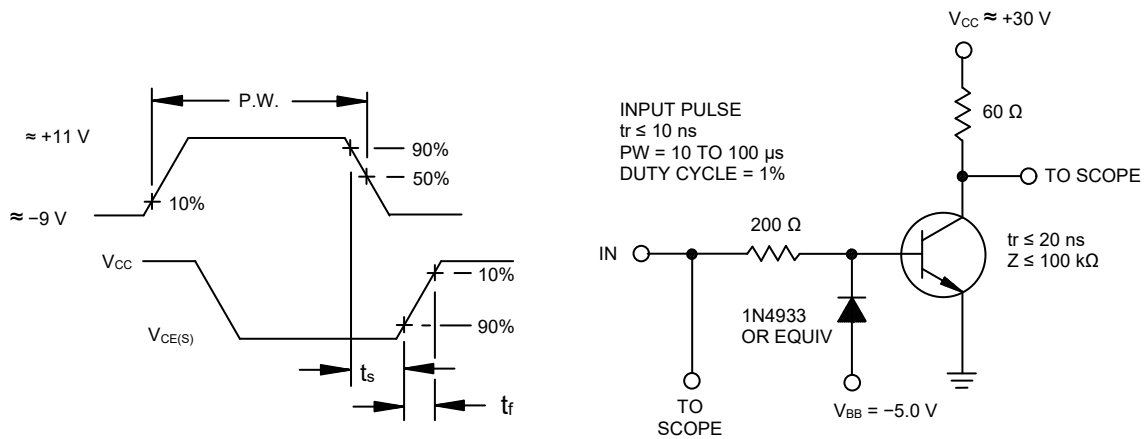
* TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling	1051	500 cycles, condition D.	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2</u>			45 devices, c = 0
Steady-state dc blocking life	1039 or 1049	Condition A, 500 hours.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See table E-IX of MIL-PRF-19500 , subgroup 4.	
<u>Subgroup 6</u>			
ESD	1020		
<u>Subgroup 8</u>			45 devices, c = 0
Reverse stability	1033	Condition A.	

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TURN-ON (t_{on}) TIME TEST CIRCUIT



TURN-OFF (t_{off}) TIME TEST CIRCUIT

FIGURE 2. Switching time test circuit.

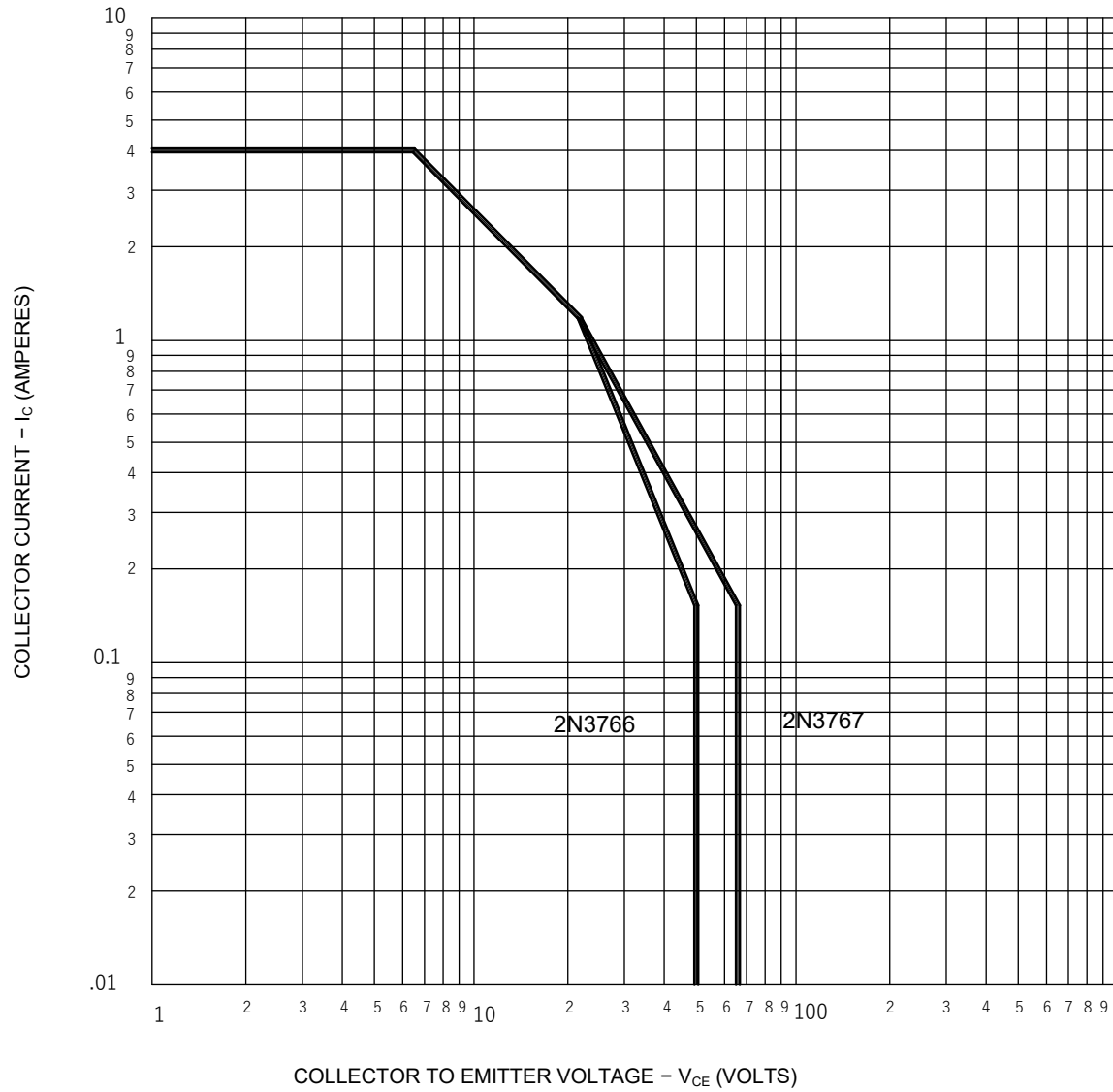


FIGURE 3. Maximum safe operating area graph (continuous dc) for types 2N3766 and 2N3767.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

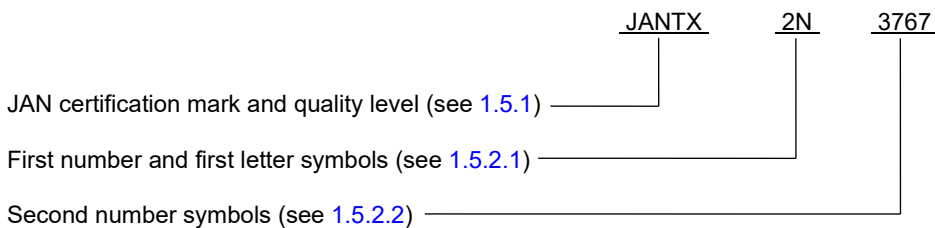
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see [5.1](#)).
- c. Lead finish (see [3.4.1](#)).
- d. The complete PIN, see [1.5](#) and [6.4](#).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database ([QML-19500](#)) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of all possible PINs for the devices available on this specification sheet.

Quality level JAN	Quality level JANTX	Quality level JANTXV
JAN2N3766	JANTX2N3766	JANTXV2N3766
JAN2N3767	JANTX2N3767	JANTXV2N3767

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6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:

Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2024-067)

Review activities:

Army - AR
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.