

The documentation and process conversion measures necessary to comply with this document shall be completed by 9 May 2025.

INCH-POUND

MIL-PRF-19500/504G
w/AMENDMENT 2
9 December 2024
SUPERSEDING
MIL-PRF-19500/504G
w/AMENDMENT 1
4 March 2024

PERFORMANCE SPECIFICATION SHEET

- * TRANSISTOR, NPN, SILICON, POWER DARLINGTON,
THROUGH-HOLE MOUNT PACKAGE, TYPES 2N6283 AND 2N6284,
JAN, JANTX, JANTXV, JANHC, AND JANKC

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

- * 1.1 Scope. This specification covers the performance requirements for NPN silicon power Darlington transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device. Two levels of product assurance are provided for unencapsulated die (JANHC and JANKC).

- * 1.2 Package outlines. The device package outlines are as follows: TO-204AA (similar to TO-3) in accordance with [figure 1](#) for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are in accordance with figures 2.

- 1.3 Maximum ratings. Unless otherwise specified, $T_c = +25^{\circ}\text{C}$.

Types	P_T		$R_{\theta JC}$ max	V_{CB0}	V_{CE0}	V_{EB0}	I_c	I_B	T_J and T_{STG}
	$T_c = +25^{\circ}\text{C}$ (1)	$T_c = +100^{\circ}\text{C}$ (2)							
	<u>W</u>	<u>W</u>	<u>$^{\circ}\text{C}/\text{W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>$^{\circ}\text{C}$</u>
2N6283	175	87.5	0.857	80	80	7	20	0.5	-65 to +200
2N6284	175	87.5	0.857	100	100	7	20	0.5	-65 to +200

- * (1) Derate linearly at 1.17 W/ $^{\circ}\text{C}$ above $T_c > +25^{\circ}\text{C}$ (see [figure 3](#)).
(2) Derate linearly at .875 W/ $^{\circ}\text{C}$ above $T_c > +100^{\circ}\text{C}$.
* (3) Continuous DC only; up to 40 A for pulse widths ≤ 5 ms. See [Figure 5](#) and [Figure 6](#).

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MIL-PRF-19500/504G
w/AMENDMENT 2

1.4 Primary electrical characteristics. Unless otherwise specified, $T_c = +25^\circ\text{C}$.

Limit	h_{FE1} (1)	h_{FE2} (1)	$V_{CE(sat)1}$	$V_{CE(sat)2}$	$V_{BE(sat)}$	Pulse response (2)	
	$V_{CE} = 3\text{ V dc}$ $I_C = 1\text{ A dc}$	$V_{CE} = 3\text{ V dc}$ $I_C = 10\text{ A dc}$	$I_C = 20\text{ A dc}$ $I_B = 200\text{ mA dc}$	$I_C = 10\text{ A dc}$ $I_B = 40\text{ mA dc}$	$I_C = 20\text{ A dc}$ $I_B = 200\text{ mA dc}$	t_{on}	t_{off}
Min	1,500	1,250	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>μs</u>	<u>μs</u>
Max		18,000	3.0	2.0	4.0	2	10

Limit	C_{obo} $V_{CB} = 10\text{ V dc}$ $I_E = 0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$ h_{fe} $ $V_{CE} = 3\text{ V dc}$ $I_C = 10\text{ A dc}$ $f = 1\text{ MHz}$
Min	<u>pF</u>	8
Max	350	80

(1) Pulsed (see 4.5.1).

* (2) See figure 4 for the pulse response circuit.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level.

* 1.5.1.1 Quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices that are applicable for this specification sheet are "JANHC" and "JANKC".

1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6283" and "6284".

1.5.3 Suffix symbols. Suffix symbols are not applicable for this specification sheet.

* 1.5.4 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A"(see 6.5.2 and figure 2).

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

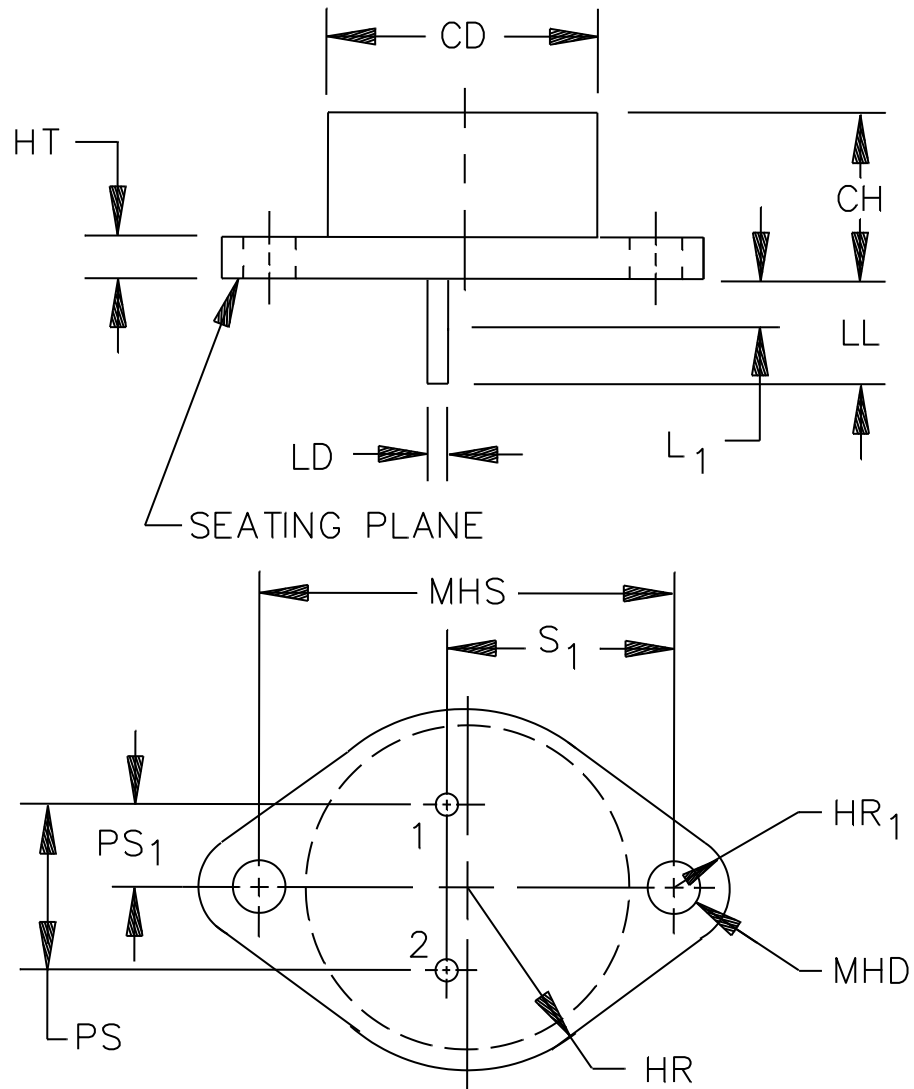


FIGURE 1. Physical dimensions (TO-204AA, similar to TO-3).

MIL-PRF-19500/504G
w/AMENDMENT 2

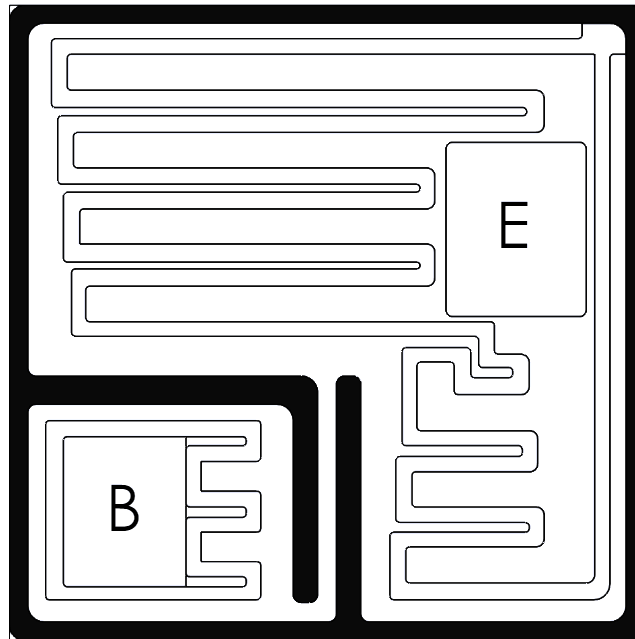
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.23	2
CH	.250	.360	6.35	9.14	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	3
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	4, 5
LL	.312	.500	7.92	12.7	4
L ₁		.050		1.27	4, 5
MHD	.151	.161	3.84	4.09	6
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	7, 8
PS ₁	.205	.225	5.21	5.72	4, 7, 8
S ₁	.655	.675	16.64	17.15	7

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Body contour is optional within zone defined by dimension CD.
3. At both ends.
4. Both terminals.
5. Dimension LD applies between L₁ and LL. Lead diameter shall not exceed twice dimension LD within dimension L₁. Diameter is uncontrolled in dimension L₁.
6. Two holes.
7. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below the seating plane. When gauge is not used, measurement shall be made at seating plane.
8. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
9. Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.

FIGURE 1. Physical dimensions (TO-204AA, similar to TO-3) - Continued.

MIL-PRF-19500/504G
w/AMENDMENT 2



NOTES

1. Chip size 0.198 x 0.198 inch $\pm$.002 inch (5.029 x 5.029 mm $\pm$ 0.05 mm).
2. Chip thickness.....0.014 inch $\pm$.002 inch (0.36 mm $\pm$.05 mm).
3. Top metal.....Aluminum 51,000 Å minimum, 60,000Å nominal.
4. Back metal Ti/Ni/Ag 8,050 Å minimum, 11,500Å nominal.
5. Backside Collector.
6. Bonding pad.....B = 0.039 x 0.047 inch (0.991 x 1.194 mm).
E = 0.043 x 0.054 inch (1.092 x 1.372 mm).

* FIGURE 2. Physical dimensions, JANHC and JANKC die (A Version).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list ([QML-19500](#)) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

I_M	-	The measurement current applied to forward bias the junction for measurement of V_{BE} .
I_H	-	The collector current applied to the device under test during the heating period.
t_H	-	The duration of the applied heating power pulse.
t_{sw}	-	Sample window time during which final V_{BE} measurement is made.

* 3.4 Interface requirements and physical dimensions. The Interface requirements and physical dimensions shall be as specified in [MIL-PRF-19500](#) [figure 1](#) (TO-204AA, similar to TO-3) and [figure 2](#).

3.4.1 Lead finish. The lead finish shall be solderable in accordance with [MIL-STD-750](#), [MIL-PRF-19500](#), and herein. Where a choice of lead finish or formation is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Polarity. The polarity of the device type shall be as shown on [figure 1](#).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

MIL-PRF-19500/504G
w/AMENDMENT 2

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

* 4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANTX and JANTXV levels only
3c (1)	Thermal impedance, see 4.3.2
11	I _C EX1 and h _{FE} 1
12	See 4.3.2
13	See subgroup 2 of table I herein. $\Delta I_{C}EX1$ = 100 percent of initial value or 2 μ A dc, whichever is greater. $\Delta h_{FE}1$ = $\pm$ 40 percent of initial value.

(1) Thermal impedance shall be performed anytime after temperature cycling, screen 3a, and does not need to be repeated in screening requirements.

* 4.3.1 Screening of unencapsulated die (JANHC and JANKC). Screening of JANHC and JANKC unencapsulated die shall be in accordance with appendix G of MIL-PRF-19500. Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

MIL-PRF-19500/504G
w/AMENDMENT 2

* 4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with test method 3131 of [MIL-STD-750](#) using the guidelines in that test method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). The thermal impedance limit used in screen 3c and subgroup 2 of [table I](#) herein shall be set statistically by the supplier. See [table II](#), subgroup 4 herein.

* 4.3.3 Power burn-in conditions. The power burn-in conditions shall be as follows: $T_J = +162.5^\circ\text{C} \pm 12.5^\circ\text{C}$; $V_{CE} \geq 10$ V dc. NOTE: No heat sink or forced air cooling on the devices shall be permitted.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and herein.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1037	For solder die attach: $T_A \leq +35^\circ\text{C}$, $V_{CE} \geq 10$ V dc; 2,000 cycles.
B3	1027	For eutectic die attach: $T_A \leq +35^\circ\text{C}$ adjust P_T to achieve $T_J = +150^\circ\text{C}$ minimum, $V_{CE} \geq 10$ V dc.
B5	3131	Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A, weight = 10 lbs (4.54 Kg), $t = 15$ s.
* C5	3131	See 4.3.2 , $R_{\theta JC} = 0.857^\circ\text{C/W}$ (maximum).
C6	1037	For solder die attach: $T_A \leq +35^\circ\text{C}$, $V_{CE} \geq 10$ V dc; 6,000 cycles.
C6	1026	For eutectic die attach: $T_A \leq +35^\circ\text{C}$ adjust P_T to achieve $T_J = +150^\circ\text{C}$ minimum, $V_{CE} \geq 10$ V dc.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse response measurements. The conditions for pulse response measurement shall be as specified in section 4 of [MIL-STD-750](#).

* 4.6 Element evaluation of unencapsulated die. The element evaluation of unencapsulated die shall be in accordance with appendix G of [MIL-PRF-19500](#).

MIL-PRF-19500/504G
w/AMENDMENT 2

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to emitter breakdown voltage 2N6283 2N6384	3011	Bias condition D, $I_C = 100$ mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	80 100		V dc V dc
Collector to emitter cutoff current 2N6283 2N6284	3041	Bias condition D $V_{CE} = 40$ V dc $V_{CE} = 50$ V dc	I_{CEO}		1.0	mA dc
Emitter to base cutoff current	3061	Bias condition D, $V_{EB} = 7$ V dc	I_{EBO}		2.5	mA dc
Collector to emitter cutoff current 2N6283 2N6284	3041	Bias condition A, $V_{BE} = -1.5$ V dc $V_{CE} = 80$ V dc $V_{CE} = 100$ V dc	I_{CEX1}		0.01	mA dc
Base emitter voltage (nonsaturated)	3066	Test condition B, $V_{CE} = 3$ V dc; $I_C = 10$ A dc	$V_{BE(on)}$		2.8	V dc
Base emitter voltage (saturated)	3066	Test condition A, $I_C = 20$ A dc; $I_B = 200$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		4.0	V dc
Collector to emitter saturation voltage	3071	$I_C = 20$ A dc; $I_B = 200$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		3.0	V dc
Collector to emitter saturation voltage	3071	$I_C = 10$ A dc; $I_B = 40$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		2.0	V dc
Forward-current transfer ratio	3076	$V_{CE} = 3$ V dc; $I_C = 1$ A dc; pulsed (see 4.5.1)	h_{FE1}	1,500		
Forward-current transfer ratio	3076	$V_{CE} = 3$ V dc; $I_C = 10$ A dc; pulsed (see 4.5.1)	h_{FE2}	1,250	18,000	
Forward-current transfer ratio	3076	$V_{CE} = 3$ V dc; $I_C = 20$ A dc; pulsed (see 4.5.1)	h_{FE3}	500		

See footnotes at end of table.

MIL-PRF-19500/504G
w/AMENDMENT 2

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:		T _A = +150°C				
Collector to emitter cutoff current 2N6283 2N6284	3041	Bias condition A, V _{BE} = -1.5 V dc V _{CE} = 80 V dc V _{CE} = 100 V dc	I _C EX2		5.0	mA dc
Collector to emitter saturation voltage	3071	I _C = 10 A dc; I _B = 40 mA dc; pulsed (see 4.5.1)	V _{CE(sat)} 3		2.0	V dc
Low temperature operation:		T _A = -55°C				
Forward-current transfer ratio	3076	V _{CE} = 3 V dc; I _C = 10 A dc; pulsed (see 4.5.1)	h _{FE} 4	200		
<u>Subgroup 4</u>						
Pulse response						
Turn-on time		(See figure 4); V _{CC} = 30 V dc; I _C = 10 A dc; I _B = 40 mA dc	t _{on}		2.0	μs
Turn-off time		(See figure 4); V _{CC} = 30 V dc; I _C = 10 A dc; I _{B1} = I _{B2} = 40 mA dc	t _{off}		10	μs
Magnitude of common emitter small-signal, short-circuit forward- current transfer ratio	3306	V _{CE} = 3 V dc; I _C = 10 A dc; f = 1.0 MHz	h _{fe}	8	80	
Small-signal, short-circuit forward-current transfer ratio	3206	V _{CE} = 3 V dc, I _C = 10 A dc; f = 1 kHz	h _{fe}	700		
Open-circuit output capacitance	3236	V _{CB} = 10 V dc; I _E = 0; 100 kHz ≤ f ≤ 1 MHz	C _{obo}		350	pF

See footnotes at end of table.

MIL-PRF-19500/504G
w/AMENDMENT 2

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
Subgroup 5 Safe operating area (continuous dc)	3051	T _C = +25°C +10°C, -0°; t = 1 s; 1 cycle; (see figure 5)				
Test 1 (Both device types)		V _{CE} = 8.75 V dc; I _c = 20 A dc				
Test 2 (Both device types)		V _{CE} = 30 V dc; I _c = 5.8 A dc				
Test 3 2N6283 2N6284		V _{CE} = 80 V dc; I _c = 100 mA dc V _{CE} = 100 V dc; I _c = 100 mA dc				
Safe operating area (switching)	3053	Load condition C, (unclamped inductive load); (see figure 6 and figure 7); T _A = +25°C; R _s ≤ 0.1 Ω; t _r + t _f ≤ 15 ns; duty cycle ≤ 2 percent;				
Test 1		t _p = 80 μs; (vary to obtain I _c); R _{BB1} ≥ 50 Ω; V _{BB1} ≥ 10 V dc; R _{BB2} = ∞; V _{BB2} = 0; I _c = 20 A dc; V _{cc} ≥ 50 V dc; The coil used shall provide a minimum inductance of 1 mH at 20 A. (For reference only, two coils in parallel (Super Electric Corporation type S16884 or equivalent).)				
Test 2		t _p = 1 ms; (vary to obtain I _c); R _{BB1} ≥ 50 Ω; V _{BB1} ≥ 10 V dc; R _{BB2} = ∞; V _{BB2} = 0; I _c = 500 mA dc; V _{cc} ≥ 50 V dc; The coil used shall provide a minimum inductance of 100 mH at 500 mA. (For reference only, two coils in series, 80 mH and 20 mH windings. Reference coils, Super Electric Corporation type S16884 or equivalent).				

See footnotes at end of table.

MIL-PRF-19500/504G
w/AMENDMENT 2

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> - Continued. Safe operating area (switching) 2N6283 2N6284 End-point electrical measurements <u>Subgroups 6 and 7</u> Not applicable	3053	Load condition B, (clamped inductive load); $T_A = +25^{\circ}\text{C}$; $t_r + t_f \leq 1.0 \mu\text{s}$; duty cycle ≤ 2 percent; $t_p = 1 \text{ ms}$; (vary to obtain I_C); $R_s = 0.1 \Omega$; $R_{BB1} = 50 \Omega$; $V_{BB1} = 10 \text{ V dc}$; $R_{BB2} = 100 \Omega$; $V_{BB2} = 1.5 \text{ V dc}$; $V_{CC} = 25 \text{ V dc}$; $I_C = 20 \text{ A dc}$; $R_L \leq 2 \Omega$; $L = 5 \text{ mH}$ (Four coils in parallel, 20 mH windings) (Triad c-48u or equivalent). Clamp voltage = $-80 +0, -5 \text{ V dc}$ Clamp voltage = $-100 +0, -5 \text{ V dc}$ Device fails if clamp voltage not reached. See subgroup 2 of this table.				

1/ For sampling plan, see MIL-PRF-19500.

2/ For end-point measurements, this test is required for the following subgroups:
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

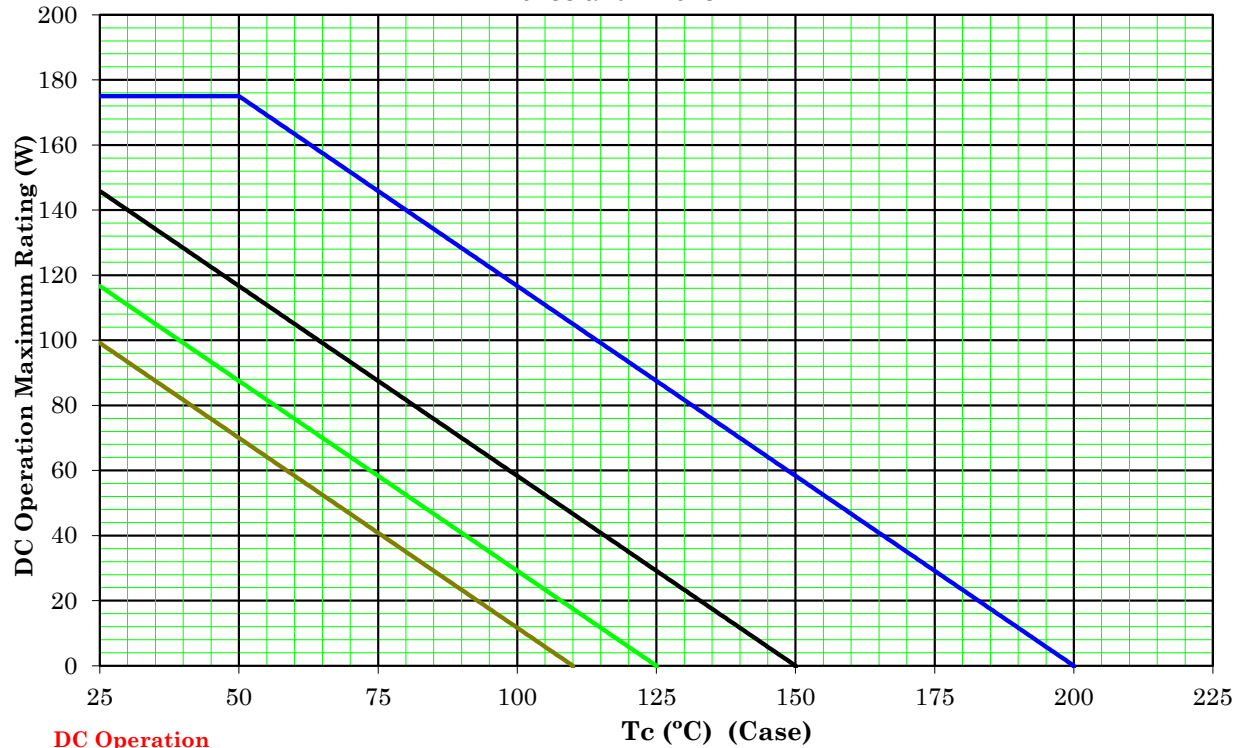
MIL-PRF-19500/504G
w/AMENDMENT 2

TABLE II. Group E inspection (all quality levels) - for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak			
Gross leak			
End-point electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Blocking life	1048	Test temperature = +125°C, V _{CB} = 80 percent rated, t = 1,000 hours.	
End-point electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 8</u>			45 devices c = 0
Reverse voltage leakage stability	1033	Condition B.	

Temperature-Power Derating Curve

2N6283 and 2N6284



DC Operation

Thermal Resistance Junction to Case = 0.857°C/W

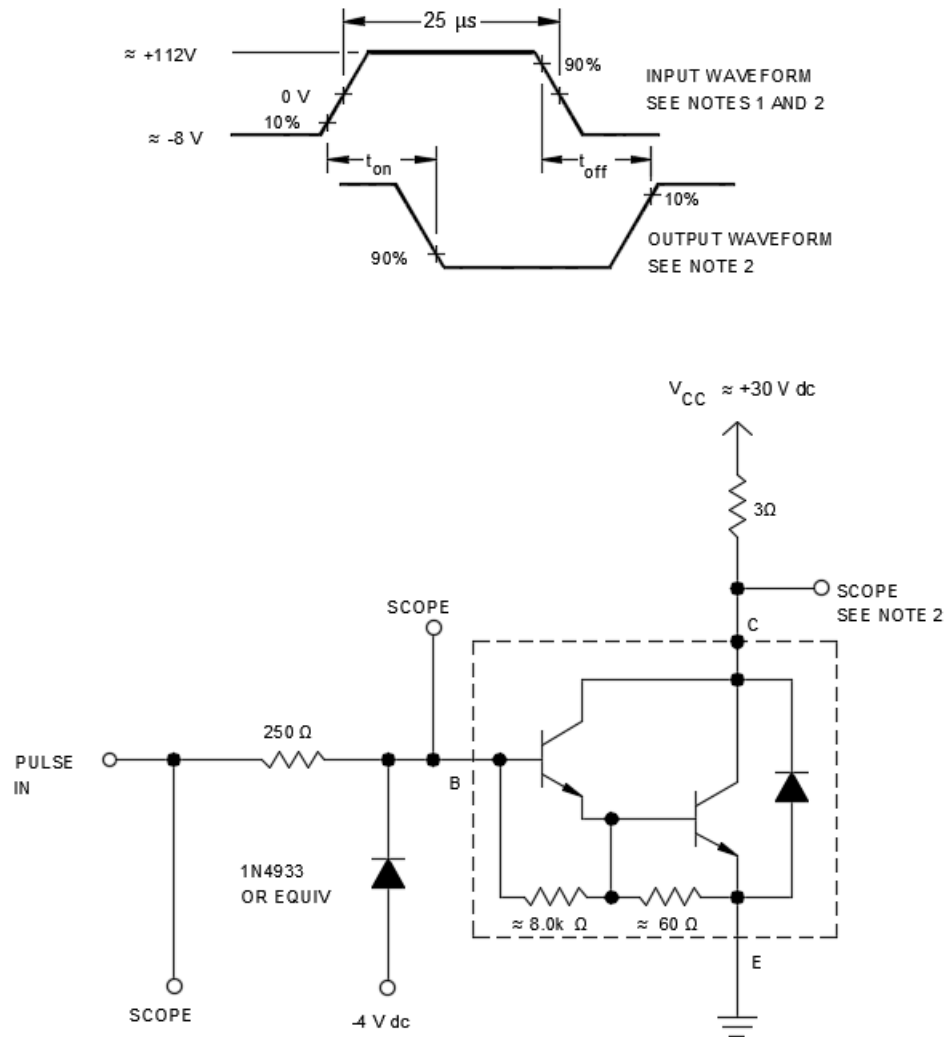
Note: Max Finish-Alloy Temp = 175.0°C

NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3 herein).
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

* FIGURE 3. Temperature-power derating curve for types 2N6283 and 2N6284.

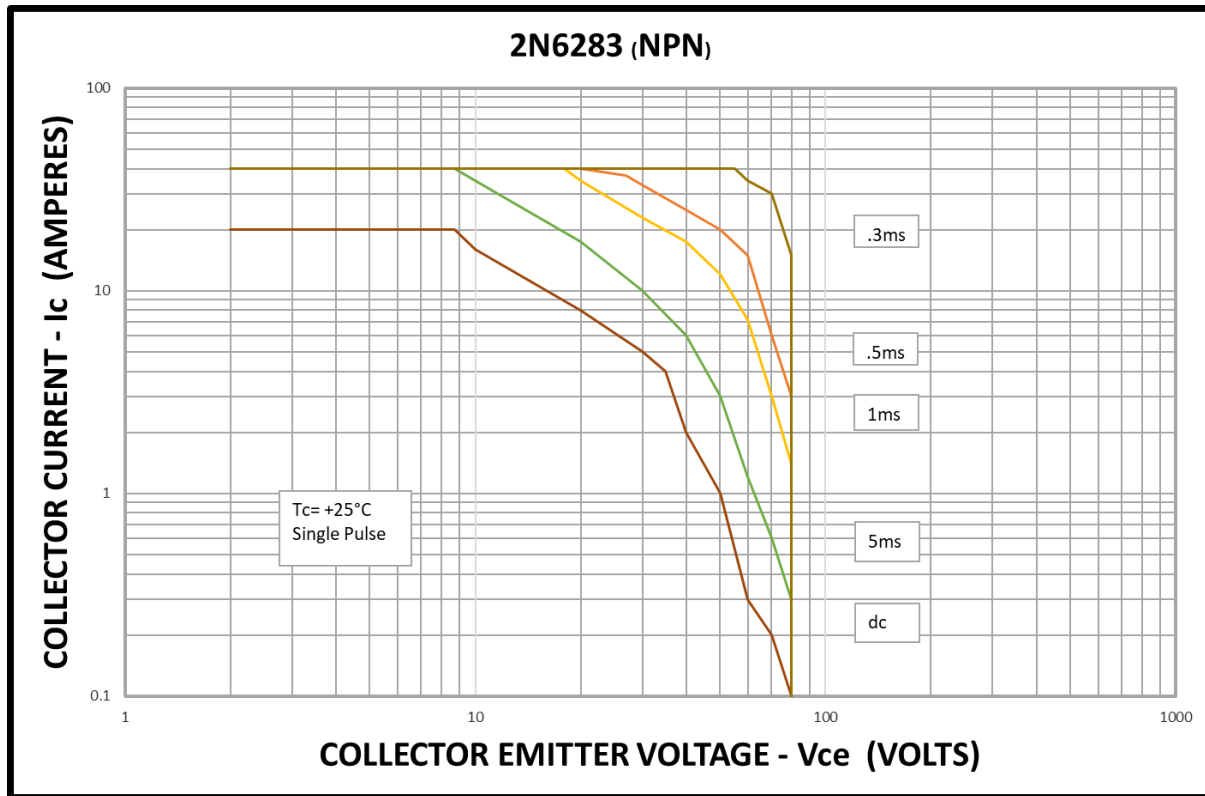
MIL-PRF-19500/504G
w/AMENDMENT 2



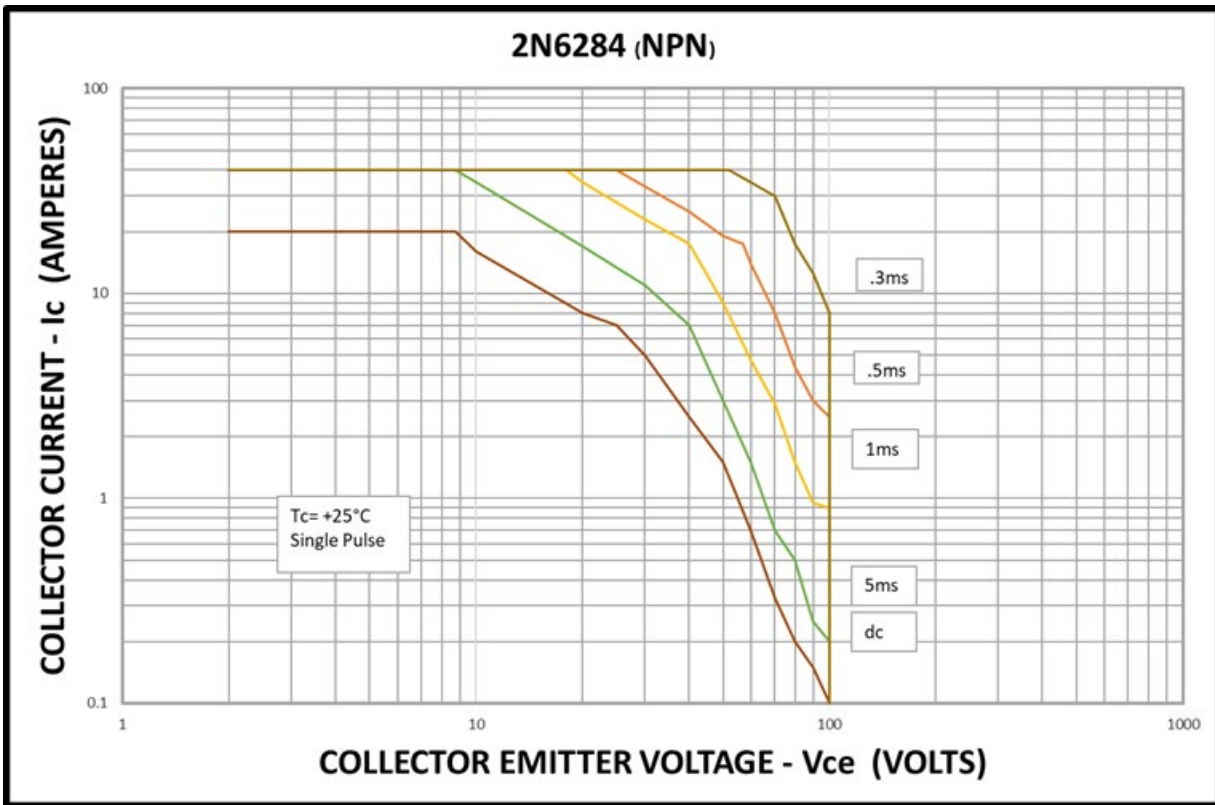
NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:
 $t_r \leq 20$ ns, $t_f \leq 20$ ns, $Z_{out} = 50$ ohms, $PW = 25$ μ s, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics:
 $t_r \leq 20$ ns, $Z_{in} \geq 20$ k Ω , $C_{in} \leq 11.5$ pf.
3. Resistors shall be non-inductive types.
4. The dc power supplies may require additional by-passing in order to minimize ringing.

* FIGURE 4. Pulse response test circuit.

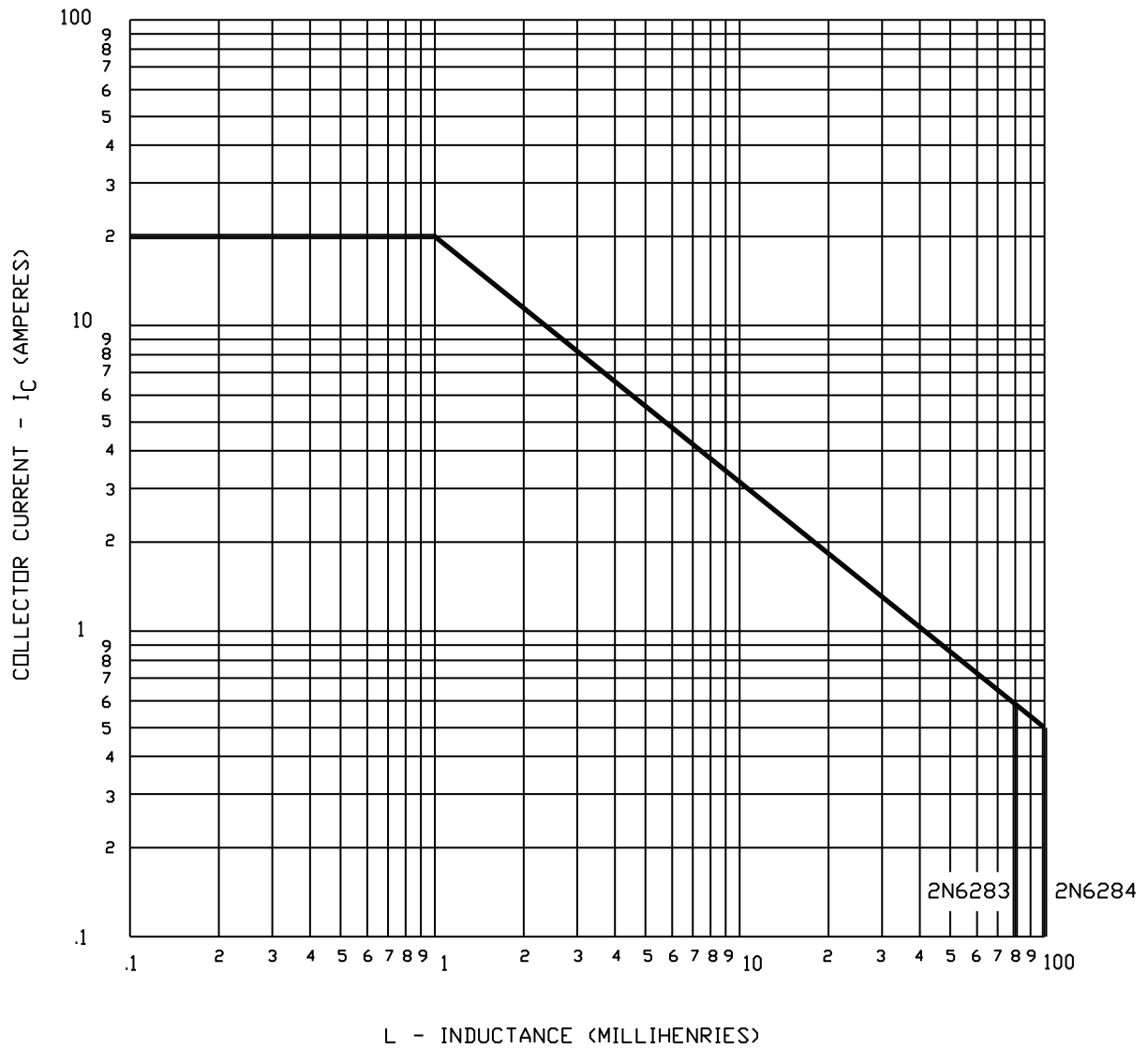


* FIGURE 5. Maximum safe operating area graph.



* FIGURE 6. Maximum safe operating area graph.

MIL-PRF-19500/504G
w/AMENDMENT 2



* FIGURE 7. Safe operating area for switching between saturation and cutoff (unclamped inductive load).

MIL-PRF-19500/504G
w/AMENDMENT 2

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of material is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

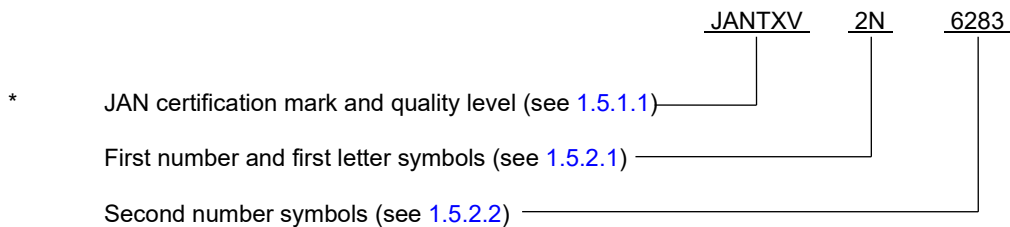
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

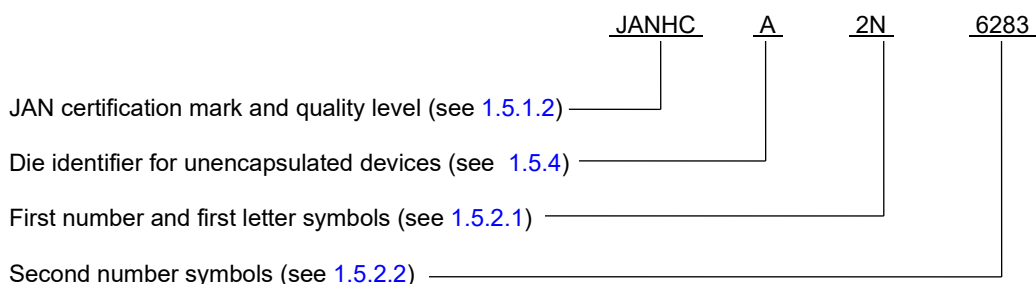
6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



MIL-PRF-19500/504G
w/AMENDMENT 2

* 6.4.2 Unencapsulated devices. The PINs for unencapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

* 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for types 2N6283	PINs for types 2N6284
JAN2N6283	JAN2N6284
JANTX2N6283	JANTX2N6284
JANTXV2N6283	JANTXV2N6284

* 6.5.2 List of PINs for Unencapsulated devices. The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

PINs for die of quality level JANHC	PINs for die of quality level JANKC
JANHCA2N6283	JANKCA2N6283
JANHCA2N6284	JANKCA2N6284

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

MIL-PRF-19500/504G
w/AMENDMENT 2

6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Air Force - 85
DLA - CC

Preparing activity:
DLA - CC
(Project 5961-2024-101)

Review activities:
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.