

The documentation and process conversion measures necessary to comply with this document shall be completed by 2 December 2025.

INCH-POUND
MIL-PRF-19500/444P
w/AMENDMENT 4
2 September 2025
SUPERSEDING
MIL-PRF-19500/444P
w/AMENDMENT 3
7 September 2022

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SWITCHING, SCHOTTKY,
* TYPES 1N5711, 1N5712, 1N6857, 1N6858, THROUGH HOLE, SURFACE MOUNT AND
UNENCAPSULATED DIE, QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein
shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for Schottky barrier diodes. Four levels of product assurance are provided for each encapsulated device type as specified in [MIL-PRF-19500](#). Two levels of product assurance are provided for each unencapsulated device type.

* 1.2 Package outlines and die topography. The device package for the encapsulated device type are as follows: DO-35 in accordance with [figure 1](#), surface mount version UR in accordance with [figure 2](#), and surface mount versions UB in accordance with [figure 3](#). The UD dimensions are in accordance with [figure 4](#). The dimensions and topography for JANHC and JANKC unencapsulated die are as follows: A version die in accordance with [figure 5](#), B version die in accordance with [figure 6](#).

1.3 Maximum ratings. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Type (1)	V_{RWM}	I_{O1}	I_{O2} (2)	T_{STG} and T_J	$R_{\theta JL}$ (3)	$R_{\theta JEC}$ (UR)	$R_{\theta JSP}$ (UB/UD)
	<u>V(pk)</u>	<u>mA dc</u>	<u>mA dc</u>		<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>
1N5711-1	50	33 (4)	5	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	250	100	
1N5711UR-1	50	33 (5)	5				170
1N5711UB	50	33 (5)	5				170
* 1N6858UB	50	75 (5)	10				80
* 1N6858UD	50	75 (5)	10				
1N6858-1	50	75 (6)	10		250		
1N6858UR-1	50	75 (7)	10			100	
1N5712-1	16	75 (6)	20		250		
1N5712UR-1	16	75 (7)	20			100	
1N5712UB	16	75 (7)	20				170
1N6857-1	16	150 (8)	50		250		
1N6857UR-1	16	150 (9)	50			100	

See notes on next page.

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FSC 5961



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1.3 Maximum ratings – Continued.

- * (1) Electrical characteristics are for all package styles.
 (2) Maximum I_O rating to ensure τ_{CL} compliance (< 100 ps).
 (3) Lead length = .375 inch (9.52 mm).
 (4) At $T_L = +130^\circ\text{C}$ and $L = .375$ inch, derate I_O to 0 at $+150^\circ\text{C}$.
 (5) At T_{EC} and $T_{SP} = +140^\circ\text{C}$, derate I_O to 0 at $+150^\circ\text{C}$.
 (6) At $T_L = +110^\circ\text{C}$ and $L = .375$ inch, derate I_O to 0 at $+150^\circ\text{C}$.
 (7) At T_{EC} and $T_{SP} = +130^\circ\text{C}$, derate I_O to 0 at $+150^\circ\text{C}$.
 (8) At $T_L = +70^\circ\text{C}$ and $L = .375$ inch, derate I_O to 0 at $+150^\circ\text{C}$.
 (9) At T_{EC} and $T_{SP} = +110^\circ\text{C}$, derate I_O to 0 at $+150^\circ\text{C}$.

* 1.4 Primary electrical characteristics.

Type (1)	$V_{(BR)1}$ $I_R =$ 10 μA dc (min)	V_{F1} $I_F =$ 1 mA dc (max)	V_{F2} $I_F = 15$ mA dc (max)	I_{R1} $V_R =$ 50 V dc (max)	C $V_R = 0, f = 1$ MHz $V_{sig} = 50$ m V(pk) (max)	τ_{CL} (max)	τ_{CL} (max)	$Z_{\theta JX}$ (max)
	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>nA dc</u>	<u>pF</u>	<u>ps</u>	<u>mA</u>	<u>°C/W</u>
1N5711-1	70	0.410	1.0	200	2.0	100	5	40
1N5711UB	70	0.410	1.0	200	2.0	100	5	60
1N6858-1	70	0.360	0.65	200	4.5	100	10	40
1N6858UB	70	0.360	0.65	200	4.5	100	10	60
1N6858UD	70	0.360	0.65	200	4.5	100	10	50

Type (1)	$V_{(BR)1}$ $I_R =$ 10 μA dc (min)	V_{F1} $I_F =$ 1 mA dc (max)	V_{F2} $I_F =$ 35 mA dc (max)	I_{R1} $V_R =$ 16 V dc (max)	C $V_R = 0, f = 1$ MHz $V_{sig} = 50$ mv(pk) (max)	τ_{CL} (max)	τ_{CL} (max)	$Z_{\theta JX}$ (max)
	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>nA dc</u>	<u>pF</u>	<u>ps</u>	<u>mA</u>	<u>°C/W</u>
1N5712-1	20	0.410	1.0	150	2.0	100	20	40
1N5712UB	20	0.410	1.0	150	2.0	100	20	60
1N6857-1	20	0.350	0.75	150	4.5	100	50	40

- (1) Electrical characteristics are for all package styles.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level.

1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHNC" and "JANKC".

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1.5.2 Device type. The designation system for the device types of semiconductors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the semiconductor covered by this specification sheet are as follows: "5711", "5712", "6857", and "6858".

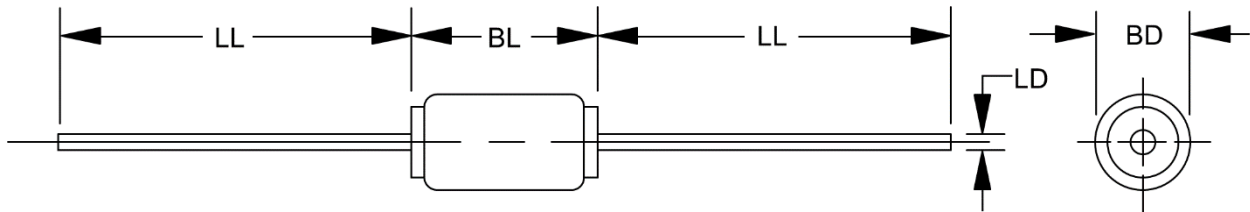
* 1.5.3 Suffix symbols. The following suffix symbol are incorporated in the PIN as applicable.

-1	Indicates an axial through hole DO-35 metallurgical bonded double plug construction (see figure 1).
UR-1	Indicates a surface mount DO-213AA using a metallurgical bonded double plug construction (see figure 2).
UB	Indicates a 3 terminal, 4 pad surface mount package. Unidirectional-(see figure 3).
UBCA	Indicates a 3 terminal, 4 pad surface mount package with ceramic lid. Dual diode with a common anode pin (see figure 3).
UBD	Indicates a 3 terminal, 4 pad surface mount package. Dual diode doubler (see figure 3).
UBCC	Indicates a 3 terminal, 4 pad surface mount package with ceramic lid. Dual diode with a common cathode pin (see figure 3).
UD	Indicates a 2 terminal, 3 pad surface mount package (see figure 4).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

* 1.5.5 Die identifier for unencapsulated devices (manufacturer and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A" and "B" (see [figure 5](#), [figure 6](#), and [6.5.2](#)).

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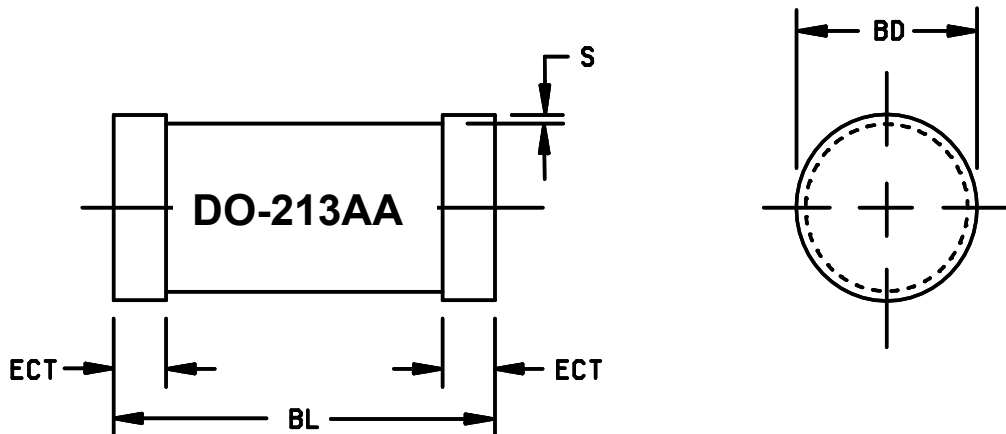
Symbol	Dimensions				Notes
	Inches	Inches	mm	mm	
	Min	Max	Min	Max	
BD	.068	.076	1.73	1.93	2, 3
BL	.125	.170	3.18	4.32	2
LD	.014	.022	0.36	0.56	
LL	1.000	1.500	25.40	38.10	

* NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions BL, BD, and LD include all components of the diode periphery except the sections of the leads over which the diameter is controlled.
3. Dimension BD shall be measured at the largest diameter.

1N5711-1, 1N5712-1, 1N6857-1, and 1N6858-1

FIGURE 1. Physical dimensions, (DO-35).



Symbol	Dimensions				Note
	Inches	Inches	mm	mm	
	Min	Max	Min	Max	
BD	.063	.067	1.60	1.70	2
BL	.130	.146	3.30	3.71	
ECT	.016	.022	0.41	0.55	
S	0		0		2

*

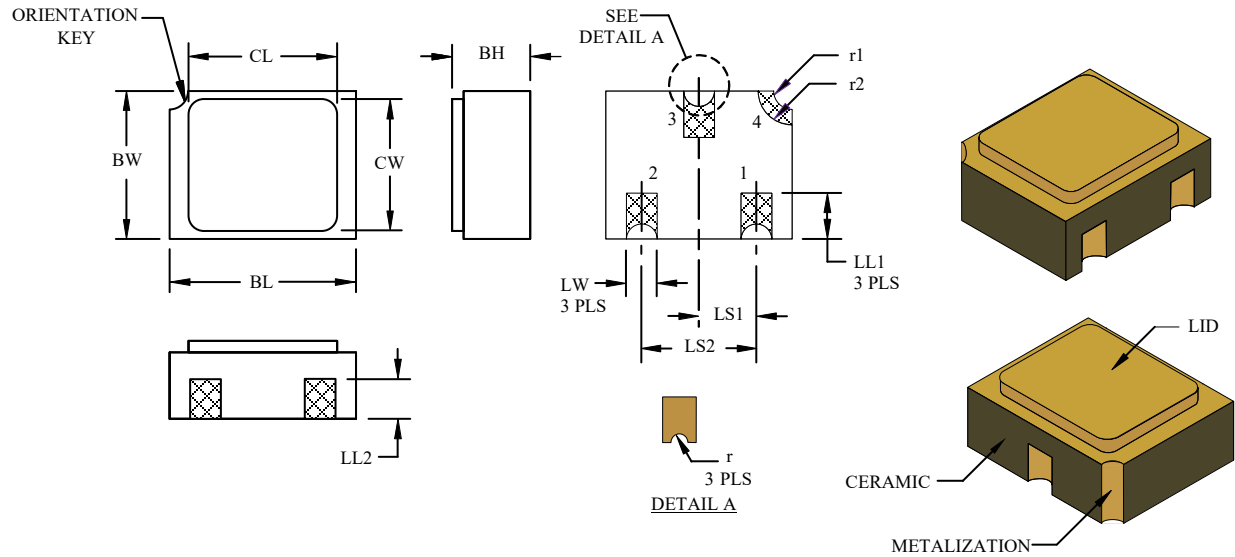
NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimension S is optional however the glass body diameter shall not exceed endcap diameter.

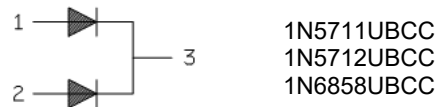
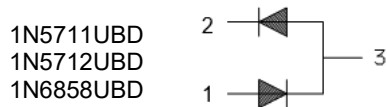
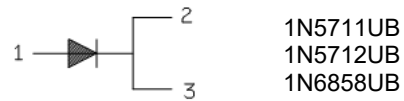
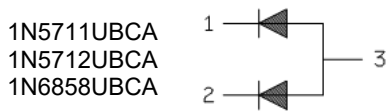
1N5711UR-1, 1N5712UR-1, 1N6857UR-1, and 1N6858UR-1

FIGURE 2. Physical dimensions. (DO-213AA).

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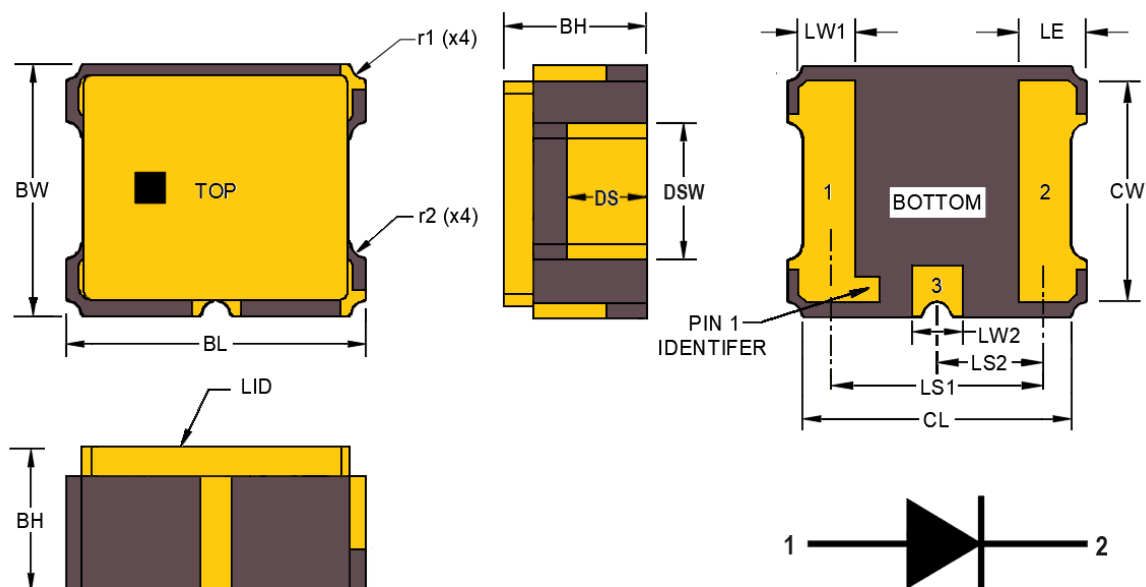
Symbol	Dimensions				Symbol	Dimensions			
	Inches	Inches	mm	mm		Inches	Inches	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	.040	.056	1.02	1.42	LS ₁	.035	.040	0.89	1.02
BL	.115	.128	2.92	3.25	LS ₂	.071	.079	1.81	2.01
BW	.085	.108	2.16	2.74	LW	.016	.024	0.41	0.61
CL		.128		3.25	r		.008		0.20
CW		.108		2.74	r1		.012		0.31
LL1	.022	.038	0.56	0.96	r2		.022		0.56
LL2	.017	.035	0.43	0.89					



- * NOTES:
1. Dimensions are in inches.
 2. Millimeters are given for general information only.
 3. Hatched areas on package denote metallized areas.
 4. Pad 4 = Shielding connected to the lid.

FIGURE 3. Physical dimensions, surface mount (UB version).

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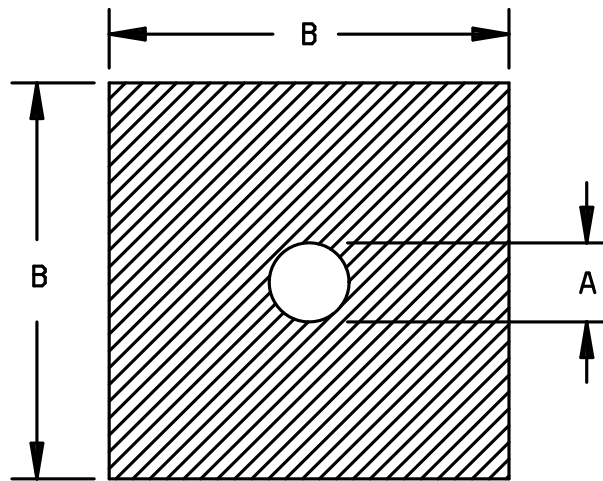


Symbol	Inches	Inches	mm	mm	Symbol	Inches	Inches	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	0.048	0.062	1.186	1.590	LE	0.021	0.033	0.540	0.840
BL	0.112	0.128	2.850	3.250	LS1	0.085	0.093	2.160	2.360
BW	0.092	0.108	2.340	2.740	LS2	0.043	0.047	1.080	1.180
CL	0.103	0.113	2.620	2.880	LW1	0.019	0.027	0.490	0.690
CW	0.083	0.093	2.120	2.360	LW2	0.019	0.021	0.490	0.530
DS	0.028	0.034	0.720	0.880	r1		0.006		0.150
DSW	0.051	0.057	1.330	1.430	r2		0.006		0.150

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Pad 3 is connected to the lid braze ring for shielding.
3. Cathode marked with a square.
4. Pads 1 and 2 layout equivalent to 1N6858UR-1.
5. Diode outline shown in ISO third angle projection.

* FIGURE 4. Physical dimensions of UD surface mount package.



BACKSIDE IS CATHODE

1N5711 Dimensions				
Ltr	Inches	Inches	mm	mm
	Min	Max	Min	Max
A	.004	.005	0.102	0.127
B	.0130	.0170	0.330	0.432

1N5712 Dimensions				
Ltr	Inches	Inches	mm	mm
	Min	Max	Min	Max
A	.0029	.0035	0.074	0.089
B	.0130	.0170	0.330	0.432

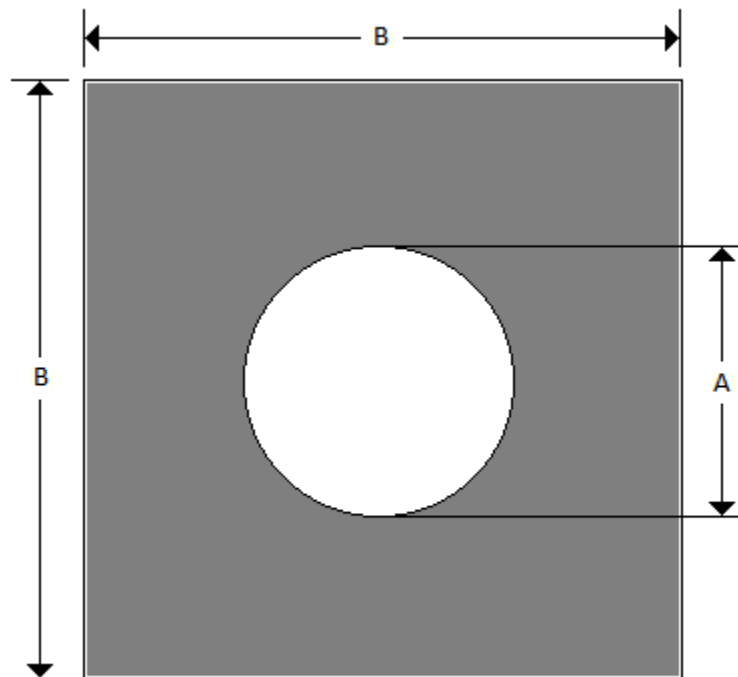
1N6857, 1N6858 Dimensions				
Ltr	Inches	Inches	mm	mm
	Min	Max	Min	Max
A	.0055	.0065	0.140	0.165
B	.0130	.0170	0.330	0.432

*NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Element evaluation accomplished utilizing TO-5 package.
3. The physical characteristics of the die are:
Metallization:
Top (anode): Al.
Back (cathode): Au.
Al thickness: 25,000 Å minimum.
Gold thickness: 4,000 Å minimum.
Chip thickness: .010 inch (0.25 mm) ±.002 inch (±0.05 mm).

FIGURE 5. Physical dimensions, die, A version.

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1N5711 Dimensions				
Ltr	Inches	Inches	mm	mm
	Min	Max	Min	Max
A	.004	.006	0.102	0.152
B	.011	.013	0.279	0.330

* NOTES:

- Dimensions are in inches. Millimeters are given for general information only.
- The physical characteristics of the die are:
Metallization:
Top (anode): Al.
Back (cathode): Au.
Al thickness: 14,000 Å minimum.
Gold thickness: 5,600 Å minimum.
Chip thickness: .008 inch (.203 mm) $\pm$.002 inch ($\pm$.051 mm).

FIGURE 6. Physical dimensions, die, B version.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DRAWING

DEFENSE ELECTRONICS SUPPLY CENTER (DESC)

C68001 - Test Fixture for Effective Minority Carrier Lifetime.

(Copies of DESC Drawing C68001 are available from DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail semiconductor@dlamail.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

EC	End-cap.
τ CL	Effective carrier lifetime.
UR	Surface mount case outline, round end-cap.

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and [figure 1](#), [figure 2](#), [figure 3](#), [figure 4](#), [figure 5](#), and [figure 6](#) herein.

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3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Diode construction. All devices (except UB and UD version) shall be metallurgically bonded, double plug construction in accordance with the requirements of MIL-PRF-19500. All glass diodes shall be designed with sufficient thermal compensation in the axial direction to optimize tensile and compressive stresses. Dimensional analysis is required of all materials used to achieve axial thermal compensation. Dimensional tolerances and corresponding coefficient of thermal expansion (CTE) shall be documented on the DSCC Design and Construction Form 36D and shall be approved by the qualifying activity to maintain qualification. Dimensional tolerances shall be sufficiently tight enough to prevent excessive stresses due to the inherent CTE mismatch. The UB and UD devices shall be eutectically mounted and wire bonded in a ceramic package.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I.

3.6 Electrical test requirements. The electrical test requirements shall be table I as specified herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. Manufacturer's identification and date code shall be marked on the devices. Initial container package marking shall be in accordance with MIL-PRF-19500. The polarity shall be indicated with a contrasting color band to denote the cathode end. The prefixes JAN, JANTX, JANTXV, and JANS can be abbreviated as J, JX, JV, or JS, respectively. The part number may be reduced to J5711, JX5711, JV5711, or JS5711. No color coding shall be permitted for part numbering.

3.7.1 Polarity. The polarity of axial leaded devices shall be indicated with a contrasting color band to denote the cathode end. No color coding will be permitted for the part number.

3.7.1.1 UB devices. 'UB' devices do not require polarity marking.

* 3.7.1.2 UD devices. For the 'UD' version devices, the cathode end will be indicated by a square symbol on the lid surface.

3.7.2 UR devices. For 'UR' version devices only, all marking, except polarity may be omitted from the body, but shall be retained on the initial container. Polarity marking of 'UR' devices shall consist, as a minimum, a band or three contrasting dots spaced equally around the periphery of the cathode.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.1.1 Sampling inspection. Sampling inspection shall be in accordance with MIL-PRF-19500.

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4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC devices. Qualification shall be in accordance with [MIL-PRF-19500](#).

4.3 Screening. Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements for JANS	Measurements for JANTXV and JANTX level
1a	Required	Not required
1b	Required	Required (JANTXV only)
2	Not required	Not required
3a	Required	Required
3b	Not applicable	Not applicable
(1) 3c	Required (see 4.3.3)	Required (see 4.3.3)
4	Required for UB/UD	Not applicable
5	Required for UB/UD	Not applicable
6	Not applicable	Not applicable
8	Required	Not required
9 and 10	Not applicable	Not applicable
11	Required I_{R1} and V_{F1}	Required I_{R1} and V_{F1}
12	Required, see 4.3.1	Required. See 4.3.1 , $t = 48$ hours
(2) 13	Required. Subgroup 2 and 3 of table I herein; $\Delta I_{R1} \leq 100$ percent of initial reading or 25 nA whichever is greater; $\Delta V_{F1} \leq \pm 20$ mV dc.	Subgroup 2 of table I herein; $\Delta I_{R1} \leq 100$ percent of initial reading or 50 nA whichever is greater; $\Delta V_{F1} \leq \pm 40$ mV dc.

(1) Thermal impedance shall be performed any time after sealing provided temperature cycling is performed in accordance with table E-IV of [MIL-PRF-19500](#), JANTX and JANTXV levels do not need to be repeated in screening requirements.

(2) Test within 24 hours after removal from test.

4.3.1 Burn-in conditions. Burn-in conditions are as follows: High temperature reverse bias (HTRB), method 1038 of [MIL-STD-750](#), test condition A, $V_R = 40$ V; $T_A = +150^\circ\text{C}$ (min) for 1N5711 and 1N6858. $V_R = 12.8$ V, $T_A = +150^\circ\text{C}$ (min) for 1N5712 and 1N6857.

4.3.2 Screening (JANHC or JANKC). Screening of JANC die shall be in accordance with [MIL-PRF-19500](#), "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance measurements. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of [MIL-STD-750](#), as applicable, using the guidelines in that method for determining I_H , I_M , and t_{MD} . t_H shall be 10 ms maximum. See group B inspection, subgroup 6, paragraph [4.4.2.1](#), group C inspection, subgroup 5, paragraph [4.4.3](#), and group E, subgroup 4 of [table II](#) herein.

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4.3.4 JAN testing. JAN level product will have temperature cycling and thermal impedance testing performed in accordance with [MIL-PRF-19500](#), JANTX level screening level requirements.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (for JANS) and table E-VIB (for JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#), and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

* 4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

	<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
*	B3	1051	Required for UB and UD.
	B3	See 4.5.4	Preconditioning for temperature cycling.
*	B4	1037	I _{O1} at rated V _{RWM} (For UB and UD devices, 50 percent of I _{O1} at rated V _{RWM}); f = 60 Hz; T _A = room ambient as defined in 4.5 of MIL-STD-750 ; t _{on} = t _{off} = 3 minutes minimum for 2,000 cycles.
	B5	1038	HTRB in accordance with 4.3.1 .
	B6	4081	R _{θJL} = 250°C/W .375 inch (9.52 mm) lead length (non-surface mount).

* 4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX and JANTXV) of [MIL-PRF-19500](#).

	<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
	B2	See 4.5.4	Preconditioning for temperature cycling.
	B2	1056	0°C to +100°C, 10 cycles (glass diodes only), n = 22, c = 0.
	B2	1051	-55°C to +150°C, 25 cycles, n = 22, c = 0.
	B3	1038	HTRB, in accordance with 4.3.1 .
*	B4	2101	See 4.5.3 (Scribe and break not applicable for UB and UD)
	B4	2075	See 4.5.3.1 (Not applicable to glass packages)
	B6	1032	T _A = +150°C.

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* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	See 4.5.4	Preconditioning for temperature cycling.
C2	1056	0°C to +100°C, 15 cycles, n = 22, c = 0.
C2	1051	-55°C to +150°C, 20 cycles, n = 22, c = 0.
C2	2036	(Not applicable to surface mount devices); lead fatigue conditions: Test condition E; .062 inch (1.57 mm) lead restriction from case. Tension conditions: Test condition A; 10 pounds (4.54 kg), 15 seconds.
C5	4081	$R_{\theta JEC} = 100^{\circ}\text{C/W}$ (maximum) $+25^{\circ}\text{C} \leq T_R \leq +35^{\circ}\text{C}$, at $T_H \geq 25$ seconds in still air. (See 4.3.3.)
C5	4081	$R_{\theta JL} = 250^{\circ}\text{C/W}$ (maximum) at .375 inch (9.52 mm) lead length, $+25^{\circ}\text{C} \leq T_R \leq +35^{\circ}\text{C}$, at $T_H \geq 25$ seconds in still air. (See 4.3.3.)
*	C5	$R_{\theta JSP} = 170^{\circ}\text{C/W}$ (maximum) for UB and $R_{\theta JSP} = 80^{\circ}\text{C/W}$ (maximum) for UD.
	C6	1038 HTRB in accordance with 4.3.1.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table II herein. Electrical measurements (end-points) shall be as specified in table II.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Steady-state operation life. This test shall be conducted with a half-sine wave of the specified peak voltage impressed across the diode in the reverse direction followed by a half-sine waveform of the specified average rectified current. The forward conduction angle of the rectified current shall not be greater than 180 degrees nor less than 150 degrees.

* 4.5.2 Effective carrier lifetime (τ_{CL}). This test shall be measured with the device installed in the test fixture, DESC Drawing C68001 or equivalent for leaded and surface mount devices, using the test set up shown on [figure 7](#) herein. Adjust the signal generator to 54 MHz. Adjust the sensitivity of the oscilloscope to 5 mV/div (1N5711), 10 mV/div (1N6858), 20 mV/div (1N5712), and 50 mV/div (1N6857). With the device in the test fixture, adjust the output of the amplifier or VHF oscillator until the peak amplitude of the forward current is 5 cm as seen on the oscilloscope (5 mA (1N5711), 10 mA (1N6858), 20 mA (1N5712), and 50 mA (1N6857)).

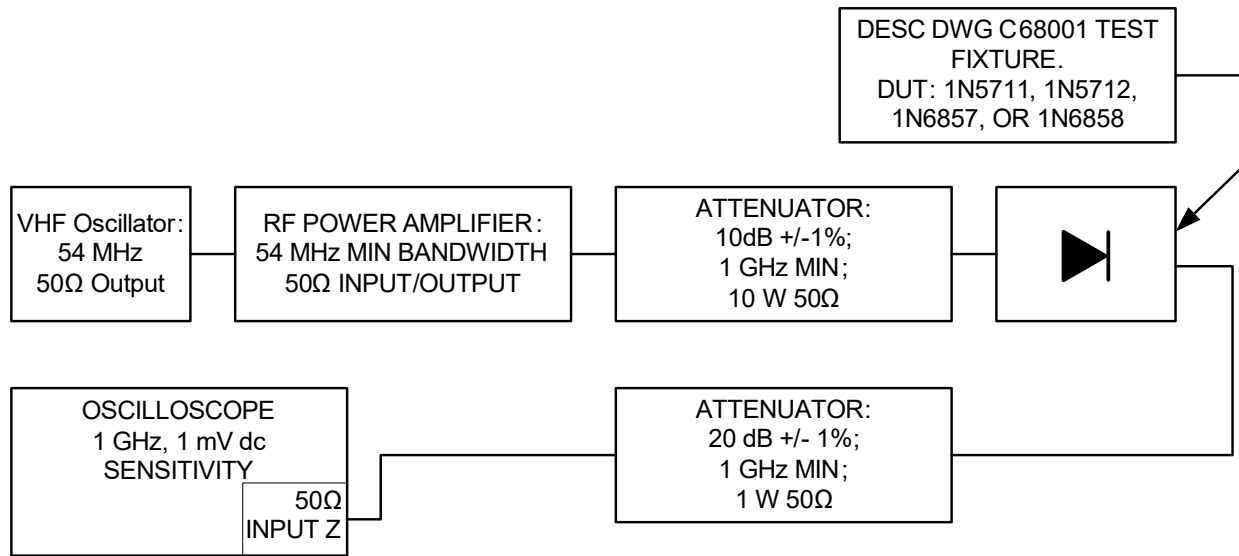


FIGURE 7. Test setup for diode effective lifetime measurement.

Change the sensitivity of scope to 2 mV/div (1N5711, 1N6858), 5 mV/div (1N5712), or 10 mV/div (1N6857). Under these conditions, the effective carrier lifetime is related to the amplitude designated as " τ_{CL} " shown on figure 8. This amplitude has the calibration of 200 ps/div (1N5711), 100 ps/div (1N6858), 125 ps/div (1N5712), and 100 ps/div (1N6857).

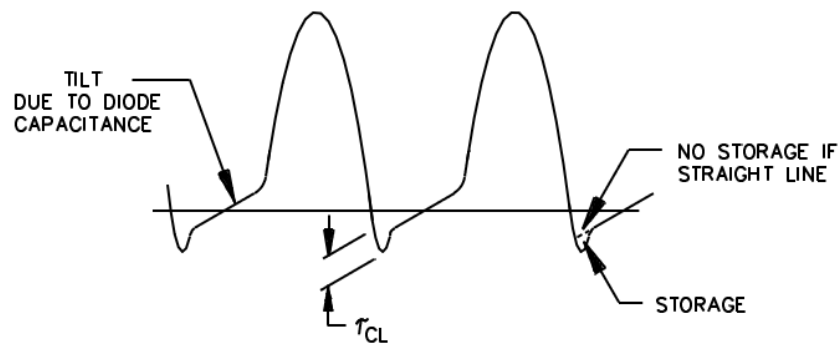


FIGURE 8. Oscilloscope display in diode effective lifetime measurement.

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* 4.5.3 Decap analysis (for glass packages only). Scribe and break (scribe and break not applicable to UB and UD packages). Scratch glass at cavity area with diamond scribe. Carefully snap open. Using 30X magnification, examine the area where die (or bonding material) is in contact with the plugs, verify metallurgical bonding area.

* 4.5.3.1 Decap analysis (for UB and UD packages only). Decap the package. Carefully remove the lid. Using 30X magnification, examine the area where die (or bonding material) is mounted to the header, verify wire bond area.

* 4.5.4 Preconditioning for temperature cycling (not applicable to UB and UD packages).

- a. Read and record I_{R1} , V_{F2} , and $Z_{\theta JX}$. Maintain device serialization throughout testing.
- b. Immerse device terminations into any suitable flux. Flux is used to prevent solder bridging across the terminations of device and to provide for a suitable contact needed for post electrical testing.
- c. Immerse device terminations into solder. The devices terminations shall be immersed instantly and not gradually, and held completely immersed in the solder for 5 ± 2 , -0 seconds. No dwell time over the solder pot shall be permitted. Maintain solder temperature to $+260^{\circ}\text{C} \pm 5^{\circ}\text{C}$.
- d. The device shall be allowed to return to ambient prior to cleaning. Remove residue flux from the terminations by dipping the parts in isopropyl alcohol or other suitable solvent.
- e. Test devices to method 1056 and 1051 of MIL-STD-750 and in accordance with MIL-PRF-19500.
- f. Read and record I_{R1} , V_{F2} , and $Z_{\theta JX}$, test subgroup 2 of table 1 herein.
- g. Failure criteria: Subgroup 2 of table 1 herein.

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* TABLE I. Group A inspection.

Inspection 1/ <u>Subgroup 1</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3101	See 4.3.3	$Z_{\theta JX}$		40	°C/W
Thermal impedance (UB packages) <u>2/</u>	3101	See 4.3.3	$Z_{\theta JX}$		60	°C/W
(UD packages) <u>2/</u>					50	°C/W
1N5711-1, all packages						
Forward voltage	4011	Condition B, $I_F = 1$ mA dc	V_{F1}		.410	V dc
Forward voltage	4011	Condition B, $I_F = 15$ mA dc	V_{F2}		1.0	V dc
Reverse current	4016	Condition A or B, DC method; $V_R = 50$ Vdc	I_{R1}		200	nA dc
Breakdown voltage	4021	$I_R = 10$ μ A dc	$V_{(BR)1}$	70		V dc
1N5712-1, all packages						
Forward voltage	4011	Condition B, $I_F = 1$ mA dc	V_{F1}		.410	V dc
Forward voltage	4011	Condition B, $I_F = 35$ mA dc	V_{F2}		1.0	V dc
Reverse current	4016	Condition A or B, DC method; $V_R = 16$ Vdc	I_{R1}		150	nA dc
Breakdown voltage	4021	$I_R = 10$ μ A dc	$V_{(BR)1}$	20		V dc
1N6857-1, UR-1						
Forward voltage	4011	Condition B, $I_F = 1$ mA dc	V_{F1}		.350	V dc
Forward voltage	4011	Condition B, $I_F = 35$ mA dc	V_{F2}		.75	V dc
Reverse current	4016	Condition A or B, DC method; $V_R = 16$ Vdc	I_{R1}		150	nA dc
Breakdown voltage	4021	$I_R = 10$ μ A dc	$V_{(BR)1}$	20		V dc
1N6858-1, UR-1						
Forward voltage	4011	Condition B, $I_F = 1$ mA dc	V_{F1}		.360	V dc
Forward voltage	4011	Condition B, $I_F = 15$ mA dc	V_{F2}		.65	V dc
Reverse current	4016	Condition A or B, DC method; $V_R = 50$ Vdc	I_{R1}		200	nA dc
Breakdown voltage	4021	$I_R = 10$ μ A dc	$V_{(BR)1}$	70		V dc
<u>Subgroup 3</u>						
1N5711-1, all packages		$T_A = +150^\circ\text{C}$				
High temperature operation						
Reverse current	4016	Condition A or B, DC method; $V_R = 50$ Vdc	I_{R2}		200	μ A dc
Low temperature operation		$T_A = -55^\circ\text{C}$				
Forward voltage	4011	Condition B, $I_F = 1$ mA dc	V_{F3}		.55	V dc
Forward voltage	4011	Condition B, $I_F = 15$ mA dc	V_{F4}		1.0	V dc
Breakdown voltage	4021	$I_R = 10$ μ A dc	$V_{(BR)2}$	70		V dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued.						
1N5712-1, all packages High temperature operation		T _A = +150°C				
Reverse current	4016	Condition A or B, DC method; V _R = 16 V dc	I _{R2}		150	μA dc
Low temperature operation		T _A = -55°C				
Forward voltage	4011	Condition B, I _F = 1 mA dc	V _{F3}		0.55	V dc
Forward voltage	4011	Condition B, I _F = 35 mA dc	V _{F4}		1.0	V dc
Breakdown voltage	4021	I _R = 10 μA dc	V(BR)2	20		V dc
1N6857-1, UR-1 High temperature operation		T _A = +150°C				
Reverse current	4016	Condition A or B, DC method; V _R = 16 V dc	I _{R2}		300	μA dc
Low temperature operation		T _A = -55°C				
Forward voltage	4011	Condition B, I _F = 1 mA dc	V _{F3}		.55	V dc
Forward voltage	4011	Condition B, I _F = 35 mA dc	V _{F4}		1.0	V dc
Breakdown voltage	4021	I _R = 10 μA dc	V(BR)2	20		V dc
1N6858-1, UR-1 High temperature operation		T _A = +150°C				
Reverse current	4016	Condition A or B, DC method; V _R = 50 V dc	I _{R2}		400	μA dc
Low temperature operation		T _A = -55°C				
Forward voltage	4011	Condition B, I _F = 1 mA dc	V _{F3}		.55	V dc
Forward voltage	4011	Condition B, I _F = 15 mA dc	V _{F4}		1.0	V dc
Breakdown voltage	4021	I _R = 10 μA dc	V(BR)2	70		V dc
<u>Subgroup 4</u>						
Capacitance	4001		C			
1N5711-1, 1N5712-1, and UB, UD, and UR		V _r = 0V dc; f = 1 MHz;			2.0	pF
1N6857-1, 1N6858-1, and UR		V _{sig} = 50 mV(pk) maximum			4.5	pF
Effective carrier lifetime (see 4.5.2) <u>3/</u>		(See DESC drawing C68001)	τ _{CL}		100	ps
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.

2/ For end-point measurements, this test is required for the following subgroups:

Group B, subgroups 3, 4 and 5 (JANS).

Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).

Group C, subgroups 2 and 6.

Group E, subgroup 1.

3/ Effective carrier lifetime needs to be performed only one time for each wafer lot.

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TABLE II. Group E inspection (all quality levels) - for qualification and requalification.

Inspection <u>1/</u>	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Thermal shock	1056	100 cycles, -55°C to 100°C (glass diodes only)	
Temperature cycling (air to air)	1051	500 cycles, -55°C to 150°C	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I , subgroup 2 (V_{F1} , I_{R1} and thermal impedance)	
<u>Subgroup 2</u>			45 devices c = 0
Steady-state dc blocking life	1048	See 4.5.1 , 1,000 hrs	
Electrical measurements		See table I , subgroup 2 (V_{F1} and I_{R1})	
<u>Subgroup 4</u>			
Thermal resistance	4081	$R_{\theta JS}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations, see 4.3.3 . (May apply to multiple specification sheets).	n = 15, c = 0
Thermal impedance curves		See MIL-PRF-19500 , table E-IX, group E, subgroup 4.	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			
ESD testing	1020		
<u>Subgroup 9</u>			45 devices
Resistance to glass cracking	1057	Test until failure occurs or to a maximum of 25 cycles, whichever comes first. Not applicable for UB and UD device.	

*

1/ For sampling plan, see [MIL-PRF-19500](#).

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

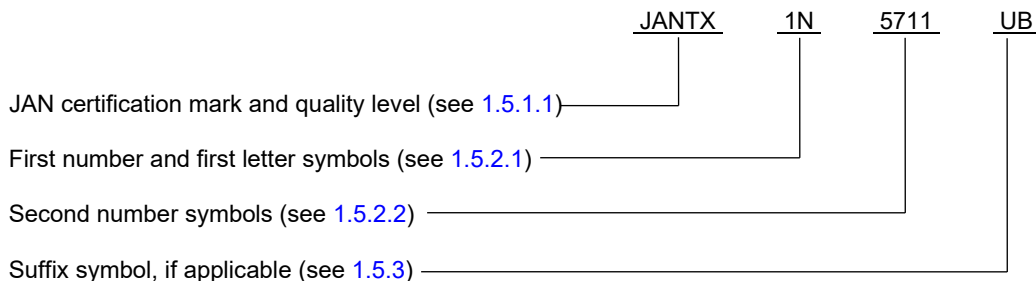
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.4.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

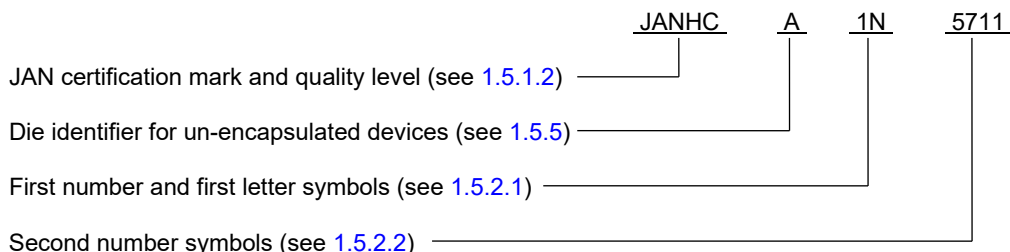
6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



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6.4.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.5 List of PINs.

* 6.5.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N5711-1	JANTX1N5711-1	JANTXV1N5711-1	JANS1N5711-1
JAN1N5711UR-1	JANTX1N5711UR-1	JANTXV1N5711UR-1	JANS1N5711UR-1
JAN1N5711UB	JANTX1N5711UB	JANTXV1N5711UB	JANS1N5711UB
JAN1N5711UBCA	JANTX1N5711UBCA	JANTXV1N5711UBCA	JANS1N5711UBCA
JAN1N5711UBCC	JANTX1N5711UBCC	JANTXV1N5711UBCC	JANS1N5711UBCC
JAN1N5711UBD	JANTX1N5711UBD	JANTXV1N5711UBD	JANS1N5711UBD
JAN1N5712-1	JANTX1N5712-1	JANTXV1N5712-1	JANS1N5712-1
JAN1N5712UR-1	JANTX1N5712UR-1	JANTXV1N5712UR-1	JANS1N5712UR-1
JAN1N5712UB	JANTX1N5712UB	JANTXV1N5712UB	JANS1N5712UB
JAN1N5712UBCA	JANTX1N5712UBCA	JANTXV1N5712UBCA	JANS1N5712UBCA
JAN1N5712UBCC	JANTX1N5712UBCC	JANTXV1N5712UBCC	JANS1N5712UBCC
JAN1N5712UBD	JANTX1N5712UBD	JANTXV1N5712UBD	JANS1N5712UBD
JAN1N6857-1	JANTX1N6857-1	JANTXV1N6857-1	JANS1N6857-1
JAN1N6857UR-1	JANTX1N6857UR-1	JANTXV1N6857UR-1	JANS1N6857UR-1
JAN1N6858-1	JANTX1N6858-1	JANTXV1N6858-1	JANS1N6858-1
JAN1N6858UR-1	JANTX1N6858UR-1	JANTXV1N6858UR-1	JANS1N6858UR-1
JAN1N6858UB	JANTX1N6858UB	JANTXV1N6858UB	JANS1N6858UB
JAN1N6858UBCA	JANTX1N6858UBCA	JANTXV1N6858UBCA	JANS1N6858UBCA
JAN1N6858UBCC	JANTX1N6858UBCC	JANTXV1N6858UBCC	JANS1N6858UBCC
JAN1N6858UBD	JANTX1N6858UBD	JANTXV1N6858UBD	JANS1N6858UBD
JAN1N6858UD	JANTX1N6858UD	JANTXV1N6858UD	JANS1N6858UD

6.5.2 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

PINs for types 1N5711	PINs for types 1N5712	PINs for types 1N6857	PINs for types 1N6858
JANHCA1N5711	JANHCA1N5712	JANHCA1N6857	JANHCA1N6858
JANKCA1N5711	JANKCA1N5712	JANKCA1N6857	JANKCA1N6858
JANHCB1N5711			
JANKCB1N5711			

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6.6 Suppliers of die. The qualified die suppliers with the applicable letter version (e.g., JANHCA1N5711) will be identified on the QML.

PIN	JANC ordering information	JANC ordering information
	Manufacturer	Manufacturer
	43611	52GC4
1N5711-1 1N5712-1 1N6857-1 1N6858-1	JANHCA1N5711, JANKCA1N5711 JANHCA1N5712, JANKCA1N5712 JANHCA1N6857, JANKCA1N6857 JANHCA1N6858, JANKCA1N6858	JANHCB1N5711, JANKCB1N5711

6.7 Substitutability of dash one parts. Non-dash-one devices have been deleted from this specification. Dash-one devices are a direct substitute for non dash-one devices and are preferred. The following table shows the direct substitutability.

Superseded part number	Superseding part number
1N5711	1N5711-1
1N5711UR	1N5711UR-1
1N5712	1N5712-1

6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2025-080)

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.