The documentation and process conversion measures necessary to comply with this document shall be completed by 31 July 2026.

INCH-POUND

MIL-PRF-19500/435R
w/AMENDMENT 1
4 March 2026
SUPERSEDING
MIL-PRF-19500/435R
23 November 2020

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, LOW-NOISE VOLTAGE REGULATOR, TYPES 1N4099 THROUGH 1N4135, 1N4614 THROUGH 1N4627, 5, 2, AND 1 PERCENT VOLTAGE TOLERANCE, ENCAPSULATED (AXIAL LEAD THROUGH-HOLE AND SURFACE MOUNT PACKAGES) AND UN-ENCAPSULATED (DIE), QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for 500 milliwatt, silicon, low-noise, voltage regulator diodes with voltage tolerances of 5 percent, 2 percent, and 1 percent. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device (die).

1.2 Package outlines. The device package outlines are as follows: DO-35 in accordance with figure 1, DO-213AA in accordance with figure 2, UB, in accordance with figure 3, UB2 in accordance with figure 4, and UD in accordance with figure 5. The dimensions and topography for JANHC and JANKC unencapsulated die are as follows: A, B, and C version die in accordance with figure 6, the D version die in accordance with figure 7, and E version die in accordance with figure 8.

1.3 Maximum ratings. Unless otherwise specified T_C = 25°C. Maximum ratings are as shown in maximum test ratings herein (see 3.6.1), and as follows:

a. P_{TL} = 500 mW (DO-35) at T_L = +50°C, L = .375 inch (9.53 mm); both ends of case or diode body to heat sink. (Derate to 0 at +175°C).

b. P_{TEC} = 500 mW (DO-213AA) at T_{EC} = +125°C. (Derate to 0 at +175°C).
-65°C ≤ T_J ≤ +175°C; -65°C ≤ T_{STG} ≤ +175°C.

c. P_{TPCB} =400 mW, (DO-7, DO-35) T_A = +55°C. (Derate to 0 at +175°C).

d. $P_{SP(IS)}$ = 500 mW (UB, UB2, and UD) at $T_{SP(IS)}$ = +125°C. (Derate to 0 at +175°C).
-65°C ≤ T_J ≤ +175°C; -65°C ≤ T_{STG} ≤ +175°C.

e. P_{TPCB} = 400 mW (UB, UB2, and UD) at T_A = +75°C. (Derate to 0 at +175°C.)

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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1.3 Maximum ratings. – continued.

(1) See figures 10, 11, and 12 for derating curves.

(2) T_A = +75°C for both axial leaded and US mounted to printed circuit board (PCB). The PCB details for determining ratings when axial leaded or UR devices are mounted horizontally and in still air are as follows: Base material is FR4 .0625 inch (1.59 mm) thick, 1-layer 1-Oz Cu. PCB pad size for US devices is .05 inch (1.27 mm) x .087 inch (2.21 mm). PCB land sizes for axial leaded devices is .092 inch (2.34 mm) diameter with L ≤ .125 inch (3.18 mm) lead length. Strips connected to the lands and pads are .030 inch (0.762 mm) x 1 inch (25.4 mm) long.

1.4 Primary electrical characteristics. Primary electrical characteristics are as shown in primary test ratings herein (see 3.6.1) and as follows:

a. 1.8 V dc ≤ V_Z ≤ 100 V dc.

b. Noise density see 4.5.5 and figure 9.

c. 1N4099 through 1N4135 and 1N4614 through 1N4627 are ±5 percent voltage tolerance.

d. 1N4370C through 1N4372C and 1N746C through 1N759C are ±2 percent voltage tolerance.

e. 1N4370D through 1N4372D and 1N746D through 1N759D are ±1 percent voltage tolerance.

f. For thermal impedance curves, see figures 13, 14, 15, 16, 17, 18 and 19.

g. $R_{\theta JA}$ = 300°C/W for junction to ambient including PCB.

h. $R_{\theta JL}$ = 250°C/W (maximum) at L = .375 inch (9.53 mm) (DO-35).

i. $R_{\theta JEC}$ = 100°C/W (maximum) for junction to end-caps (DO-213AA).

j. $R_{\theta JSP(IS)}$ = 90°C/W (maximum) for junction to solder pad (IS) (UB and UB2).

k. $R_{\theta JA(PCB)}$ = 250°C/W (maximum) for junction to ambient (PCB) (UB and UB2).

l. $R_{\theta JSP(IS)}$ = 80°C/W (maximum) for junction to solder pad (IS) for UD package.

m. $R_{\theta JA(PCB)}$ = 228°C/W (maximum) for junction to ambient (PCB) for UD package.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example, 6.5 for a list of available PINs and 6.6 for supersession information.

1.5.1 JAN brand and quality level designators.

1.5.1.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".

1.5.1.2 JAN certification mark and quality level for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The diodes of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows:

4100	4101	4102	4103	4104	4105	4106	4107	4108	4109
4110	4111	4112	4113	4114	4115	4116	4117	4118	4119
4120	4121	4122	4123	4124	4125	4126	4127	4128	4129
4130	4131	4132	4133	4134	4135				
				4614	4615	4616	4617	4618	4619
4620	4621	4622	4623	4624	4625	4626	4627		4099

1.5.3 Suffix symbols. The following suffix symbol(s) are incorporated into the PINs as applicable.

1.5.3.1 First suffix symbols (voltage tolerance). All devices covered by this specification sheet have a voltage tolerance. Those voltage tolerances are designated by the use a first suffix symbol or no suffix symbol (blank) as indicated as follows.

Blank	Indicates a non-modified version of the diode that have a nominal voltage tolerance of ±5 percent.
C	Indicates a modified version of the diode that have a nominal voltage tolerance of ±2 percent over the basic numbered (non-suffix) device for all types covered by this specification.
D	Indicates a modified version of the diode that have a nominal voltage tolerance of ±1 percent over the basic numbered (non-suffix) device for all types covered by this specification.

1.5.3.2 Second suffix symbols (package designators). The second suffix symbols (or lack thereof) that designate the package outline for the devices covered by this specification sheet are as follows.

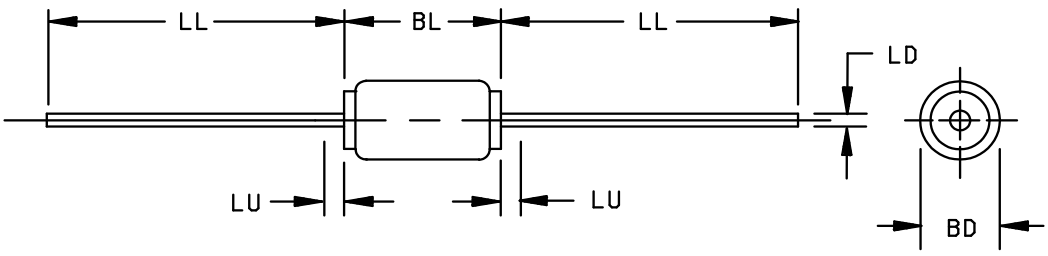
-1	Indicates an axial through-hole mount (DO-35) package with a metallurgical bond. (see figure 1).
UR-1	Indicates a surface mount, round endcap (DO-213AA) package with a metallurgical bond. (see figure 2)
UB	Indicates a 3 terminal, 4 pad surface mount package (see figure 3).
UB2	Indicates a 3 terminal, 4 pad surface mount package (see figure 4).
UD	Indicates a 2 terminal, 3 pad surface mount package (see figure 5).

1.5.3.3 Third suffix symbols (internal circuit schematic suffix designators for UB only). The suffix symbols that designate the internal circuit schematic (see schematic on figure 3) of the UB surface mount packages are as follows:

	Indicates a unidirectional, single diode circuit.
CA	Indicates dual diode with a common anode pin.
CC	Indicates a dual diode with a common cathode pin.
D	Indicates a dual diode doubler.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

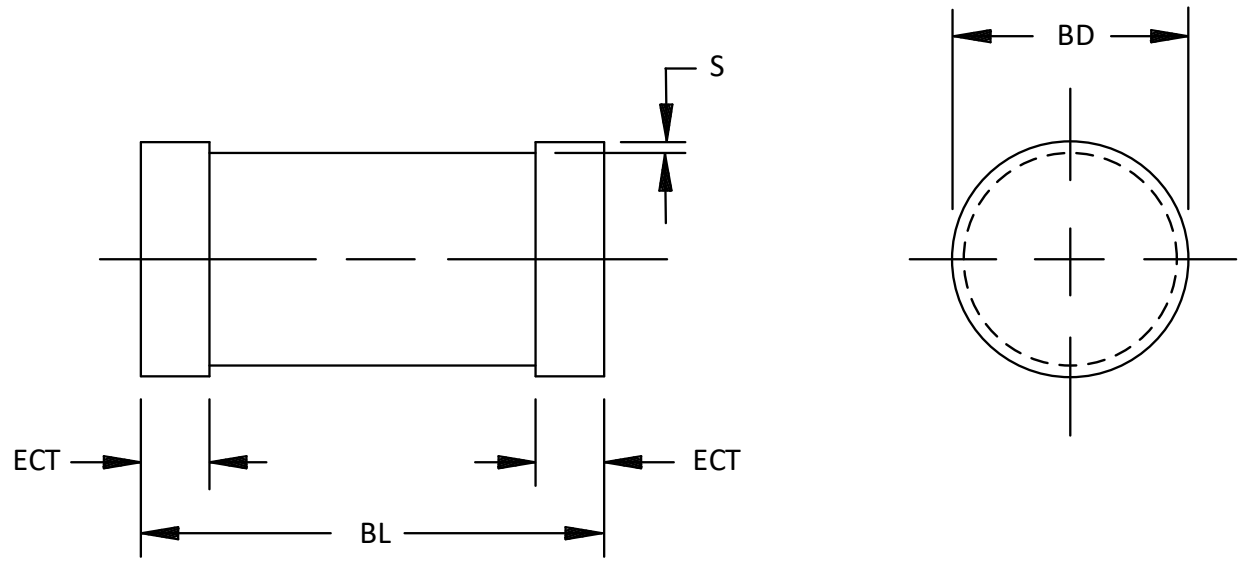
1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A" “B”, "C", "D", and "E" (see figures 6, 7, 8 and 6.5).



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BD	.056	.090	1.42	2.29	3
BL	.140	.200	3.56	5.08	3
LD	.018	.022	0.46	0.56	
LL	1.000	1.500	25.40	38.10	
LU		.050		1.27	4

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. Dimensions are pre-solder dip.
3. Package contour optional within BD and length BL. Heat slugs, if any, shall be included within this cylinder but shall not be subject to minimum limit of BD. The BL dimension shall include the entire body including slugs.
4. Within this zone lead, diameter may vary to allow for lead finishes and irregularities other than heat slugs.

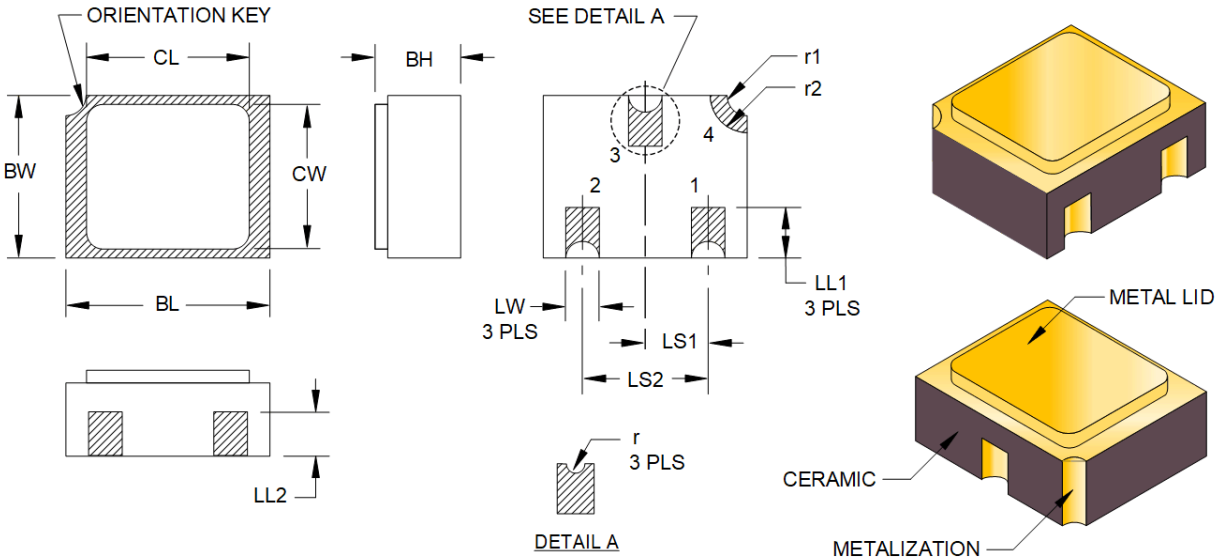
FIGURE 1. Physical dimensions of axial leaded DO-35 package.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BD	.063	.067	1.60	1.70
ECT	.016	.022	0.41	0.56
BL	.130	.146	3.30	3.71
S	.001 min		0.03 min	

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. Dimensions are pre-solder dip.
3. Dimension S is optional however the glass body diameter shall not exceed endcap diameter.

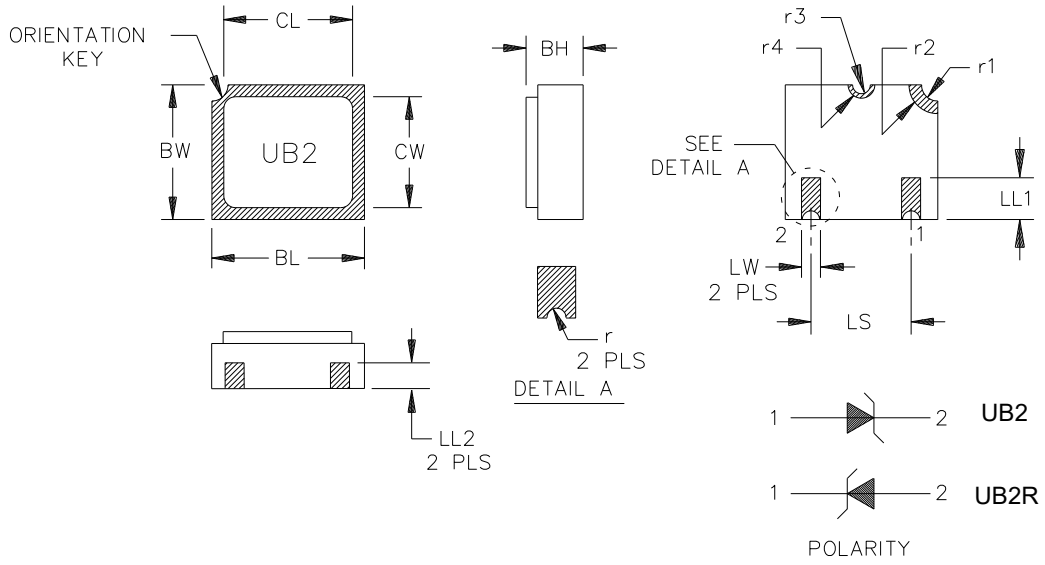
FIGURE 2. Physical dimensions of UR DO-213AA surface mount package.



Symbol	Dimensions				Symbol	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
BH	.040	.056	1.02	1.42	LS1	.035	.039	0.89	0.99
BL	.115	.128	2.92	3.25	LS2	.071	.079	1.80	2.01
BW	.085	.108	2.16	2.74	LW	.016	.024	0.41	0.61
CL		.128		3.25	r		.008		0.20
CW		.108		2.74	r1		.012		0.31
LL1	.022	.038	0.56	0.97	r2		.022		0.56
LL2	.017	.035	0.43	0.89					

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Ceramic package only.
3. Hatched areas on package denote metallized areas. Pad 4 = shielding, connected to the lid.
4. Dimensions are pre-solder dip.

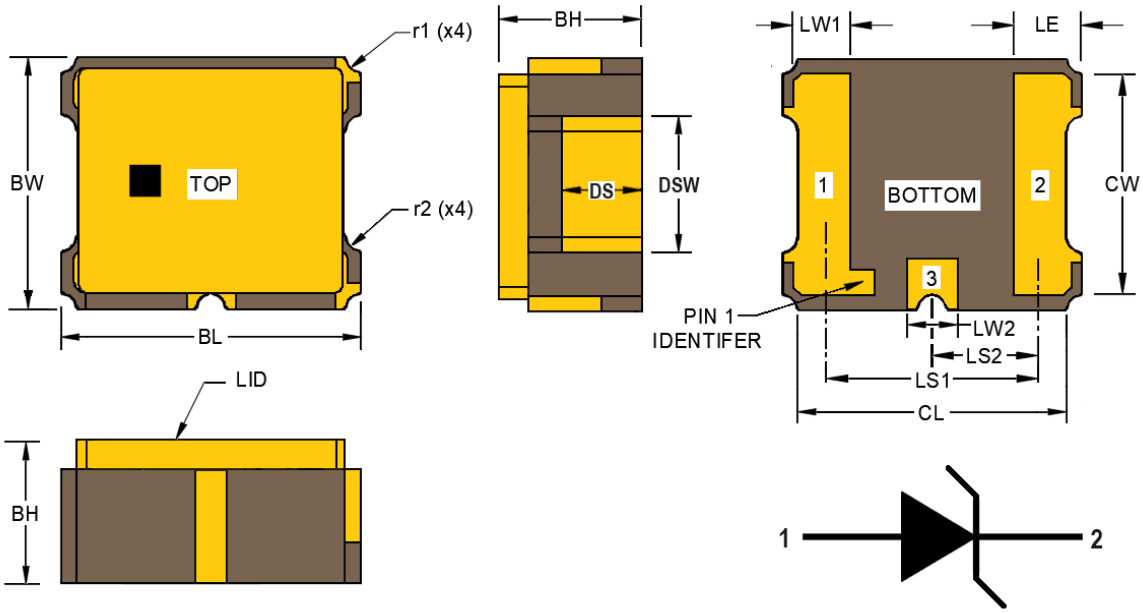
FIGURE 3. Physical dimensions of 3 terminal UB surface mount package.



Symbol	Dimensions				Symbol	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
BH	.040	.056	1.02	1.42	LS	.071	.079	1.80	2.01
BL	.115	.128	2.92	3.25	LW	.016	.024	0.41	0.61
BW	.085	.108	2.16	2.74	r	.008 TYP		0.20 TYP	
CL		.128		3.25	r1	.012 TYP		0.30 TYP	
CW		.108		2.74	r2	.022 TYP		0.56 TYP	
LL1	.022	.038	0.56	0.96	r3	.008 TYP		0.20 TYP	
LL2	.017	.035	0.43	0.89	r4	.012 TYP		0.30 TYP	

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Ceramic package only.
3. Hatched areas on package denote metallized areas. Pad 4 = shielding, connected to the lid.
4. Dimensions are pre-solder dip.

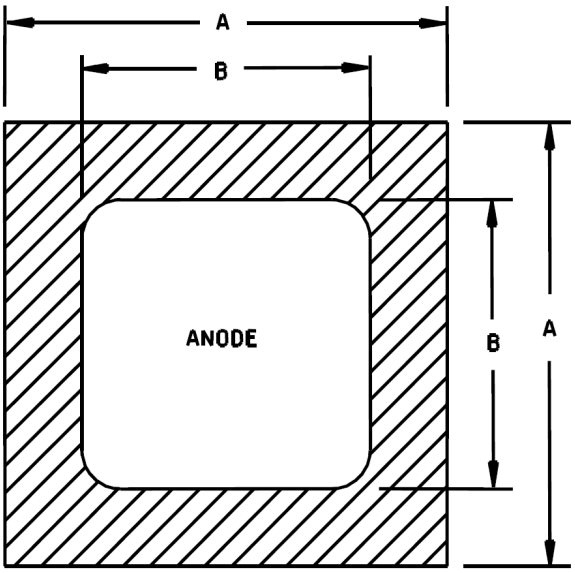
FIGURE 4. Physical dimensions of 2 terminal UB2 surface mount package.



Symbol	Inches	Inches	mm	mm	Symbol	Inches	Inches	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	0.078	0.092	1.979	2.329	LE	0.021	0.033	0.540	0.840
BL	0.112	0.128	2.850	3.250	LS1	0.085	0.093	2.160	2.360
BW	0.092	0.108	2.340	2.740	LS2	0.043	0.047	1.080	1.180
CL	0.103	0.113	2.620	2.880	LW1	0.019	0.027	0.490	0.690
CW	0.083	0.093	2.120	2.360	LW2	0.019	0.021	0.490	0.530
DS	0.028	0.034	0.720	0.880	r1		0.006		0.150
DSW	0.051	0.057	1.330	1.430	r2		0.006		0.150

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Pad 3 is connected to the lid braze ring for shielding.
3. Cathode marked with a square.
4. Pads 1 and 2 layout is equivalent to those for 1N4614-1 through 1N4627-1, and 1N4614UR-1 through 1N4627UR-1.
5. Diode outline shown in ISO third angle projection.

FIGURE 5. Physical dimensions of 2 terminal UD surface mount package.



BACKSIDE IS CATHODE

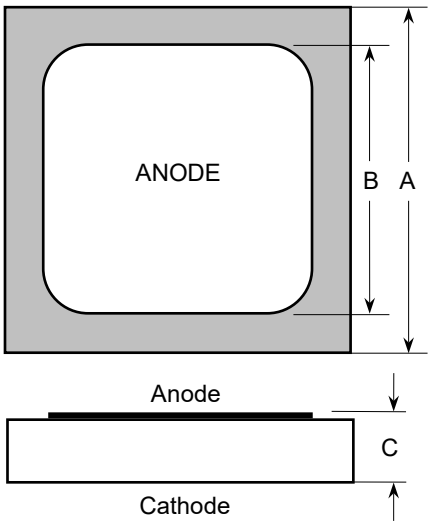
JANHCA and JANKCA				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
A	.021	.025	0.53	0.63
B	.013	.017	0.33	0.43

JANHCB and JANKCB				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
A	.024	.028	0.61	0.71
B	.017	.021	0.43	0.53

JANHCC and JANKCC				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
A	.019	.023	0.48	0.58
B	.013	.017	0.33	0.43

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The JANHCA and JANKCA die thickness is .010 (0.25 mm) ±.002 inches (±0.05 mm).
   Anode metallization: Al, thickness = 25,000 Å minimum;
   Cathode metallization: Au, thickness = 4,000 Å minimum.
3. The JANHCB and JANKCB die thickness is .010 (0.25 mm) ±.002 inches (±0.05 mm).
   Anode metallization: Al, thickness = 40,000 Å minimum;
   Cathode metallization: Au, thickness = 5,000 Å minimum.
4. The JANHCC and JANKCC die thickness is .010 (0.25 mm) ±.002 inches (±0.05 mm).
   Anode metallization: Al, thickness = 25,000 Å minimum;
   Cathode metallization: Au, thickness = 4,000 Å minimum.
5. Circuit layout data: For zener operation, cathode must be operated positive with respect to anode.

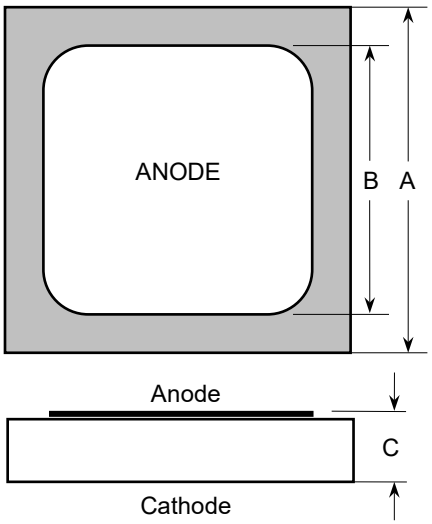
FIGURE 6. Physical dimensions for JANHC and JANKC (A, B, and C versions) die.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.023	.027	0.584	0.686
B	.015	.019	0.381	0.483
C	.008	.012	0.203	0.305

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The die thickness is .010 (0.25 mm) ±.002 inches (±0.05 mm).
   Anode metallization: Al, thickness = 34,000 Å minimum.
   Cathode metallization: Au, thickness = Ti/Au (200Å/4,350Å) nominal.

FIGURE 7. Physical dimensions for JANHC and JANKC (D version) die.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.011	.015	0.28	0.38
B	.005	.009	0.13	0.23
C	.006	.010	0.15	0.25

NOTES:
1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. The die thickness is .008 (0.203 mm) ±.002 inches (±0.051 mm).
   Anode metallization: Al, thickness = 20,000 Å minimum;
   Cathode metallization: Au, thickness = 8,000 Å) nominal.

FIGURE 8. Physical dimensions for JANHC and JANKC (E version) die.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

$R_{\theta JA}$	Thermal resistance, junction to ambient.
$R_{\theta JA(PCB)}$	Thermal resistance, junction to ambient, when mounted to PCB.
$R_{\theta JEC}$	Thermal resistance, junction to end-cap.
$R_{\theta JL}$	Thermal resistance, junction to lead.
$R_{\theta JSP(IS)}$	Thermal resistance, junction to solder pad, infinite sink.
T_{EC}	Temperature of end-cap.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, 4, 5, 6, 7 and 8 herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Diode construction. All devices shall be in accordance with the requirements of MIL-PRF-19500.

3.4.2.1 Dash one construction. Dash one (-1) diodes shall be of metallurgically bonded double plug construction or straight through construction in accordance with the requirements of category I, II, or III (see MIL-PRF-19500).

3.4.2.2 JANS construction. Construction shall be dash one or straight through construction, category I or II metallurgical bond in accordance with MIL-PRF-19500.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500 and as specified herein. Manufacturer's identification and date code shall be marked on the devices. Initial container package marking shall be in accordance with MIL-PRF-19500. The prefixes JAN, JANTX, JANTXV, and JANS may be abbreviated as J, JX, JV, and JS respectively. (Example: The PIN for an axial leaded device 1N4614 may be reduced to J4614, JX4614, JV4614, or JS4614.) No color coding shall be permitted for part identification.

3.5.1 Axial leaded devices. For axial leaded versions only, the polarity shall be indicated with a contrasting color band to denote the cathode end.

3.5.2 UR devices. For 'UR' version devices only, all marking, except polarity (and serial number for JANS) may be omitted from the body. Polarity shall be identified with a cathode band as a minimum. Alternatively, a minimum of three evenly spaced contrasting color dots around the periphery of the cathode end may be used.

3.5.3 UB and UB2 devices. The 'UB' and UB2 version devices do not require polarity marking.

3.5.4 UD devices. The 'UD' devices shall mark the cathode with a square symbol on the lid.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6.1 Maximum and primary electrical characteristics test requirements. Maximum test ratings for voltage regulator diodes are specified in table III herein.

3.6.2 Selection of tight tolerance devices. The C and D suffix devices shall be selected from JAN, JANTX, JANTXV, or JANS devices which have successfully completed all applicable screening, table I, and groups B and C testing as 5 percent tolerance devices. All sublots of C and D suffix devices shall pass table I, subgroup 2 at the tightened tolerances. The P_{TL} or P_{TEC} for C and D suffix devices shall be maintained at 30°C ±2°C for V_Z correlation on tight tolerances.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in 4.4.2, 4.4.3, table I, table II, and table III.

3.8 Workmanship. Semiconductor devices, diode, silicon, low-noise voltage regulator, shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, table I and table II).

d. Element evaluation of un-encapsulated die (see 4.6).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC devices. JANHC and JANKC devices shall be qualified in accordance with MIL-PRF-19500.

4.2.3 Construction verification. Cross sectional photos from three devices shall be submitted in the qualification report.

4.3 Screening (JAN, JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with appendix E, table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS level	Measurements for JANTXV and JANTX level
(1) 3c	Required (see 4.3.2)	Required (see 4.3.2)
4	Not applicable	Not applicable
9	Required on Nom V_Z > 10 V, I_{R1} and V_Z	Not applicable
10	Required on Nom V_Z > 10 V	Not applicable
11	ΔI_{R1} ≤ 100 percent of initial reading or 10 nA whichever is greater. ΔV_Z ≤ 2 percent of initial reading.	I_{R1} and V_Z
12	See 4.3.3, t = 240 hours.	See 4.3.3, t = 48 hours
(2) 13	Subgroups 2 and 3 of table I herein; ΔI_{R1} ≤ 100 percent of initial reading or 10 nA whichever is greater; ΔV_Z ≤ 2 percent of initial reading.	Subgroup 2 of table I herein; ΔI_{R1} ≤ 100 percent of initial reading or 10 nA whichever is greater; ΔV_Z ≤ 2 percent of initial reading.

(1) Shall be performed anytime after temperature cycling, screen 3a; TX and TXV levels do not need to be repeated in screening requirements.
(2) PDA = 5 percent for screen 13, applies to ΔI_{R1}, ΔV_Z, I_{R1} and V_Z (JANS only).

4.3.1 JAN product. JAN product will have temperature cycling and thermal impedance testing performed in accordance with MIL-PRF-19500, JANTX level screening requirements.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 as applicable of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). See table II, subgroup 4 herein.

4.3.3 Free air power burn-in conditions. Power burn-in conditions are as follows (see 4.5.4 herein): $I_{Z(min)} = I_{Z(PCB)}$. T_A = 75°C maximum. Test conditions shall be in accordance with method 1038 of MIL-STD-750, condition B. Adjust I_Z or T_A to achieve the required T_J. T_J = 125°C minimum. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table E-V of MIL-PRF-19500. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein.

4.4.2.1 Quality level JANS.

Subgroup	Method	Condition
B3	2101	Decap analysis scribe and break only. Not applicable for UB, UB2, and UD devices.
B3	2075	For UB, UB2, and UD only.
B4	1037	2,000 cycles
B5	1027	I_{ZM} = column 10 of table III minimum for 1,000 hours; adjust I_Z or T_A to achieve T_J = +175°C minimum. Marking legibility requirements shall not apply.
B6	3101 or 4081	$R_{\theta JEC}$ = 100°C/W (max) at zero lead length (DO-213AA), +25°C ≤ T_R ≤ +35°C (see 4.5.4). $R_{\theta JL}$ = 250°C/W (max) at L = .375 inch (9.53 mm), (DO-35). $R_{\theta JL}$ and $R_{\theta JEC}$ only.

4.4.2.2 Quality levels JAN, JANTX, JANTXV.

Subgroup	Method	Condition
B3	1027	I_{ZM} = column 10 of table III herein minimum. Adjust I_Z or T_A to ensure a T_J = +150°C (min).
B4	2101	Decap analysis scribe and break only. Not applicable for UB, UB2, and UD devices.
B4	2075	For UB, UB2, and UD only.
B5		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	1056	0°C to +100°C, 10 cycles.
C2	2036	Tension: condition A; 10 pounds (4.54 Kg); t = 15 seconds (not applicable to UR, UB, UB2, and UD suffix devices). Lead fatigue: Condition E, (not applicable to UR, UB, UB2, and UD suffix devices
C2	1071	Test condition E for axial leaded and UR devices (not applicable for UB, UB2 and UD devices). Fine and gross leak are required for UB, UB2, and UD devices.
C3		Not applicable.
C5	4081	See 4.3.2, $R_{\theta JL}$ and $R_{\theta JEC}$ only.
C6	1027	I_{ZM} = column 10 of table III minimum. Adjust I_Z or T_A to ensure a T_J = +150°C (min).
C8	4071	I_Z = 250 µA dc, T_A = +25°C ±5°C, T_2 = +125°C, αV_Z = column 8 of table III, sampling plan = 22 devices, c = 0.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and in table II herein. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Surge current (I_{ZSM}). The peak currents shown in column 5 of table III shall be applied in the reverse direction and these shall be superimposed on the current (I_Z = 250 µA dc) a total of five surges at 1 minute intervals. Each individual surge shall be one-half square-wave-pulse of 1/120 second duration or an equivalent one-half sinewave with the same effective rms current.

4.5.2 Regulator voltage measurements. The test current shall be applied until thermal equilibrium is attained (20 ±2 seconds maximum) prior to reading the breakdown voltage. For this test, the diode shall be suspended by its leads with mounting clips whose inside edge is located at .375 inch (9.53 mm) from the body and the mounting clips shall be maintained at a temperature of +25°C +8°C, -2°C. This measurement may be performed after a shorter time following application of the test current than that which provides thermal equilibrium if correlation to stabilized readings can be established to the satisfaction of the qualifying activity. The breakdown voltage on JANHC and JANKC shall be read with a pulse measurement of 10 ms (max).

4.5.3 Temperature coefficient of regulator voltage (αV_Z). The device shall be temperature stabilized with current applied prior to reading regulator voltage at the specified ambient temperature as specified in table I herein, subgroup 7.

4.5.4 Free air burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each DUT still sees the full P_T (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. Use method 3100 of MIL-STD-750 to measure T_J.

4.5.5 Noise density. Noise density shall be measured using a noise density test circuit as shown on figure 8. Place a low-noise resistor, equivalent in value to the dynamic impedance of the diode under test, in the test clips and adjust test current (I_{ZT}) and measure output-noise voltage. Remove resistor, insert diode under test in test clips, readjust test current to 400 µA dc and measure output-noise voltage again. To obtain noise density (N_D), subtract rms resistor output-noise voltage from rms diode output-noise voltage and divide by product of overall system gain and square root of bandwidth. All measurements shall be made at +25°C.

4.5.6 Decap internal visual scribe and break. Scratch glass at cavity area with diamond scribe. Carefully snap open. Using 30X magnification examine the area where die (or bonding material) are in contact with the plugs, verify metallurgical bonding area. If the verification of the metallurgical bonding area is in question with test method 3101 of MIL-STD-750, and test condition and limits herein, ($Z_{\theta JX}$) shall be used to determine suitability for use.

4.6 Element evaluation of un-encapsulated die. The element evaluation of unencapsulated die shall be in accordance with appendix G of MIL-PRF-19500. As a minimum, die shall be 100-percent probed to ensure compliance with table I, subgroup 2. Burn-in duration for the JANKC level shall follow the JANS requirements; the JANHC level shall follow the JANTX requirements of MIL-PRF-19500.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit 2/	Limit 2/	Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Forward voltage	4011	Condition B, I_F = 200 mA dc	V_F		1.1	V dc
Reverse current leakage	4016	Condition A or B; V_R = column 6 of table III	I_{R1}		Column 7	µA dc
Regulator voltage	4022	I_Z = 250 µA dc (see 4.5.2)	V_Z	Column 2 -V_Z tol	Column 2 +V_Z tol	V dc
Thermal impedance	3101	See 4.3.2	$Z_{\theta JX}$			°C/W
Subgroup 3						
High-temperature operation		T_A = +150°C				
Reverse current	4016	Condition A or B; V_R = column 6 of table III	I_{R2}		Column 3	µA dc
Subgroup 4						
Small-signal reverse breakdown impedance	4051	I_Z = 250 µA dc; I_{SIG} = 25 µA ac rms	Z_{ZT}		Column 4	Ohms
Noise density		I_Z = 400 µA dc (see 4.5.5)	N_D		Column 9	µV/$\sqrt{\text{Hz}}$
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	See 4.5.1				
Electrical measurements		Table I, subgroup 2				

See notes at end of table.

TABLE I. Group A inspection – continued.

Inspection 1/	MIL-STD-750		Symbol	Limit 2/	Limit 2/	Unit
	Method	Conditions		Min	Max	
Subgroup 7 (JANS only) Temperature coefficient of regulator voltage	4071	I_Z = 250 µA dc; T_1 = +25°C, ±5°C; T_2 = T_1 +100°C (see 4.5.3)	α_{VZ}		Column 8	%/°C

1/ For sampling plan, see MIL-PRF-19500.
2/ Column references are to table III herein.

TABLE II. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection 1/	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 1			45 devices, c = 0
Temperature cycling	1051	500 cycles.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			
Intermittent life	1037	6,000 cycles. I_Z = column 10 of table III.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			
Thermal resistance	3101 or 4081	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets) $R_{\theta JSP(AM)}$ need be calculated only	15 devices, c = 0
Thermal impedance curves		See MIL-PRF-19500	N/A
Subgroups 5 and 6			
Not applicable			
Subgroup 9			n = 45
Resistance to glass cracking	1057	Condition B. Cool down after solder immersion is permitted. Test until failure occurs on all devices or to a maximum of 25 cycles, whichever comes first. Not applicable for UB, UB2, and UD devices.	

1/ A separate sample may be pulled for each test.

TABLE III. Test ratings, primary electrical characteristics. 1/

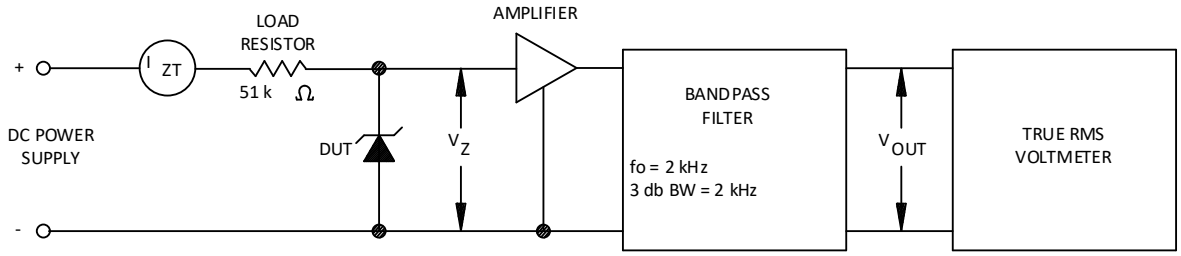
Col 1	Col 2	Col 3	Col 4	Col 5		Col 6	Col 7	Col 8	Col 9	Col 10
2/	V_Z nom	I_R at +150°C	Z_{ZT} max	I_{ZSM} (surge) Axial, UR 3/	I_{ZSM} (surge) UB, UD 4/	V_R	I_R	α_{VZ} T_1 = +25°C T_2 = +125°C	ND At 400 µA 1-3 kHz	I_{ZPCB}
	Volts	µA dc	ohms	mA	mA	Volts	µA dc	%/°C	µV/ $\sqrt{Hz}$	mA
1N4614-1	1.8	10.0	1,200	1,600	500	1.0	3.5	-0.075	1	120
1N4615-1	2.0	8.0	1,250	1,500	469	1.0	2.5	-0.075	1	110
1N4616-1	2.2	6.0	1,300	1,350	422	1.0	2.0	-0.075	1	100
1N4617-1	2.4	4.0	1,400	1,250	390	1.0	1.0	-0.075	1	95
1N4618-1	2.7	2.0	1,500	1,100	343	1.0	0.5	-0.075	1	90
1N4619-1	3.0	1.0	1,600	1,025	320	1.0	0.4	-0.075	1	87
1N4620-1	3.3	7.0	1,650	950	297	1.5	3.5	-0.075	1	85
1N4621-1	3.6	10.0	1,700	875	273	2.0	3.5	-0.065	1	83
1N4622-1	3.9	5.0	1,650	825	258	2.0	2.5	-0.060	1	80
1N4623-1	4.3	4.0	1,600	800	250	2.0	2.0	-0.050	1	77
1N4624-1	4.7	10.0	1,550	750	234	3.0	5.0	+.020,-.050	1	75
1N4625-1	5.1	10.0	1,500	725	227	3.0	5.0	+.030,-.045	2	70
1N4626-1	5.6	10.0	1,400	700	219	4.0	5.0	+.040,-.020	4	65
1N4627-1	6.2	10.0	1,200	650	203	5.0	5.0	+.050,-.010	5	61
1N4099-1	6.8	5.0	200	650	203	5.2	1.0	+.060	40	56
1N4100-1	7.5	5.0	200	650	203	5.7	1.0	+.065	40	51
1N4101-1	8.2	5.0	200	650	203	6.3	0.5	+.070	40	46
1N4102-1	8.7	5.0	200	650	203	6.7	0.5	+.075	40	44
1N4103-1	9.1	5.0	200	650	203	7.0	0.5	+.080	40	42
1N4104-1	10.0	5.0	200	650	203	7.6	0.5	+.080	40	38
1N4105-1	11.0	5.0	200	590	184	8.5	0.05	+.080	40	35
1N4106-1	12.0	5.0	200	540	169	9.2	0.05	+.080	40	32
1N4107-1	13.0	5.0	200	500	156	9.9	0.05	+.080	40	29
1N4108-1	14.0	5.0	200	464	145	10.7	0.05	+.085	40	27
1N4109-1	15.0	5.0	100	433	135	11.4	0.05	+.085	40	25

See footnotes at end of table.

TABLE III. Test ratings, primary electrical characteristics - Continued. 1/

Col 1	Col 2	Col 3	Col 4	Col 5		Col 6	Col 7	Col 8	Col 9	Col 10
2/	V_Z nom	I_R at +150°C	Z_{ZT} max	I_{ZSM} (surge) Axial, UR 3/	I_{ZSM} (surge) UB, UD 4/	V_R	I_R	αV_Z T_1 = +25°C T_2 = +125°C	ND At 400 µA 1-3 kHz	I_{ZPCB}
	Volts	µA dc	ohms	mA	mA	Volts	µA dc	%/°C	µV/ $\sqrt{Hz}$	mA
1N4110-1	16.0	5.0	100	406	127	12.2	0.05	+.085	40	24
1N4111-1	17.0	5.0	100	382	119	13.0	0.05	+.090	40	22
1N4112-1	18.0	5.0	100	361	113	13.7	0.05	+.090	40	21
1N4113-1	19.0	2.5	150	342	107	14.5	0.05	+.090	40	20
1N4114-1	20.0	2.5	150	325	102	15.2	0.01	+.090	40	19
1N4115-1	22.0	2.5	150	295	92	16.8	0.01	+.090	40	17
1N4116-1	24.0	2.5	150	271	85	18.3	0.01	+.090	40	16
1N4117-1	25.0	2.5	150	260	81	19.0	0.01	+.090	40	15
1N4118-1	27.0	2.5	150	240	75	20.5	0.01	+.090	40	14
1N4119-1	28.0	2.5	200	232	73	21.3	0.01	+.095	40	14
1N4120-1	30.0	2.5	200	216	68	22.8	0.01	+.095	40	13
1N4121-1	33.0	2.5	200	197	66	25.1	0.01	+.095	40	12
1N4122-1	36.0	2.5	200	180	56	27.4	0.01	+.095	40	11
1N4123-1	39.0	2.5	200	166	52	29.7	0.01	+.095	40	9.8
1N4124-1	43.0	2.5	250	151	47	32.7	0.01	+.095	40	8.9
1N4125-1	47.0	4.0	250	138	43	35.8	0.01	+.095	40	8.1
1N4126-1	51.0	5.0	300	127	40	38.8	0.01	+.100	40	7.5
1N4127-1	56.0	5.0	300	116	36	42.6	0.01	+.100	40	6.7
1N4128-1	60.0	5.0	400	108	34	45.6	0.01	+.100	40	6.4
1N4129-1	62.0	5.0	500	105	33	47.1	0.01	+.100	40	6.1
1N4130-1	68.0	7.0	700	95	30	51.7	0.01	+.100	40	5.6
1N4131-1	75.0	7.0	700	86	27	57.0	0.01	+.100	40	5.1
1N4132-1	82.0	8.0	800	79	25	62.4	0.01	+.100	40	4.6
1N4133-1	87.0	8.0	1,000	75	23	66.2	0.01	+.100	40	4.4
1N4134-1	91.0	10.0	1,200	71	22	69.2	0.01	+.100	40	4.2
1N4135-1	100.0	10.0	1,600	65	20	76.0	0.01	+.100	40	3.8

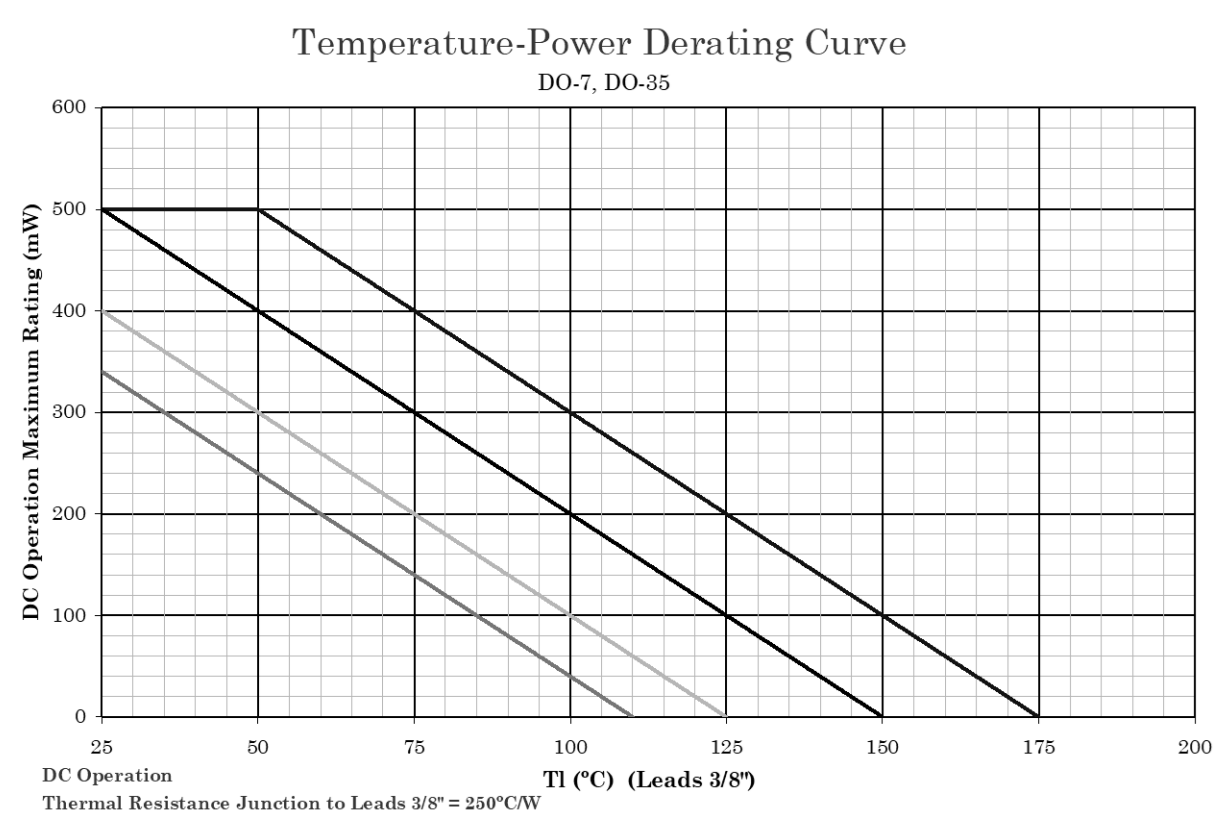
1/ Unless otherwise specified T_C = 25°C.
2/ Applies to all voltage tolerance devices. (Examples: 1N4099-1 is ±5 percent; 1N4099C-1 is ±2 percent; and 1N4099D-1 is ±1 percent tolerance).
3/ Applicable for axial leaded and UR devices.
4/ Applicable for UB, UB2, and UD devices.



NOTES:

1. Input voltage and lead resistance should be high so that zener can be driven from a constant current source.
2. Input impedance of band pass filter should be high compared with the dynamic impedance of the diode under test.
3. Filter bandwidth characteristics shall be as follows:
   a. fo = 2,000 Hz.
   b. Shape factor, -40 db to -3 dB, approximately 2.
   c. Passband at the -3 dB is 1,000 Hz ≤50 Hz to 3,000 Hz ≤150 Hz.
   d. Passband at the -40 dB is 500 Hz ≤50 Hz to 6,000 Hz ≤600 Hz.

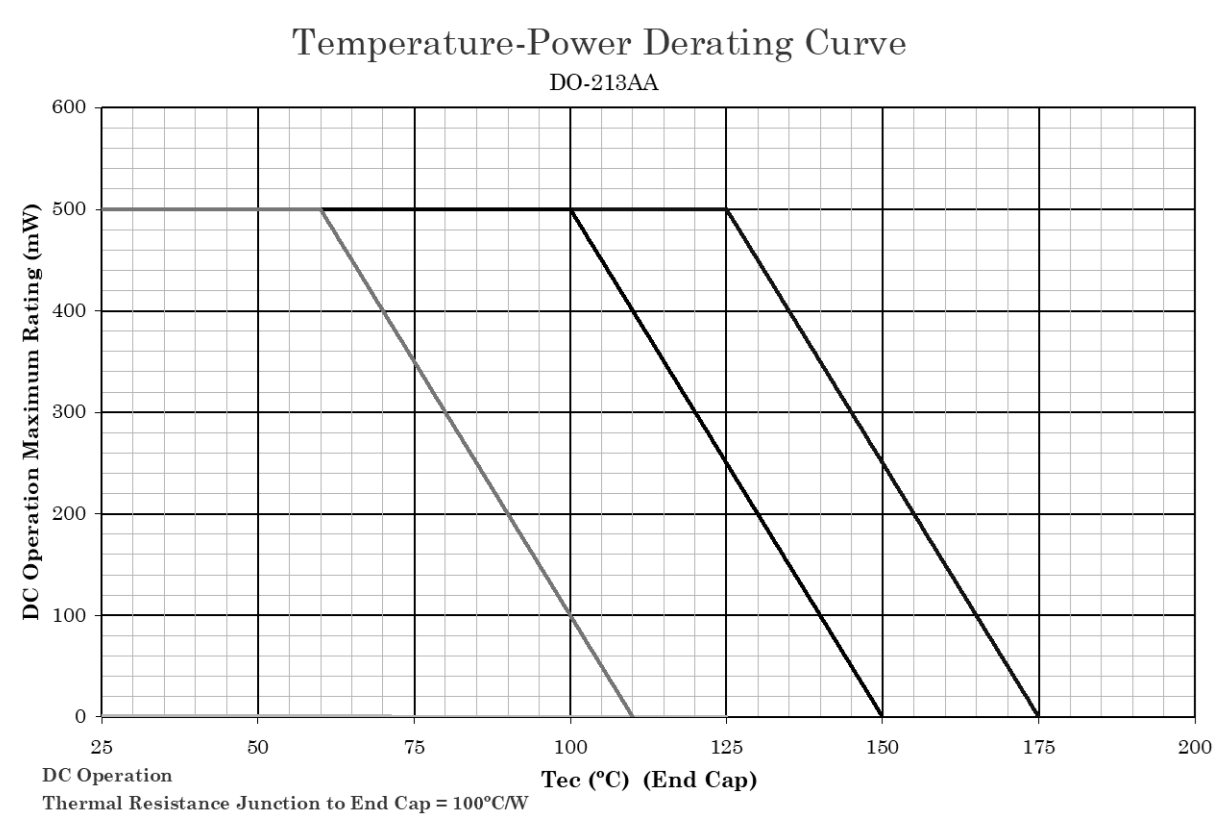
FIGURE 9. Circuit for determination of noise density.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

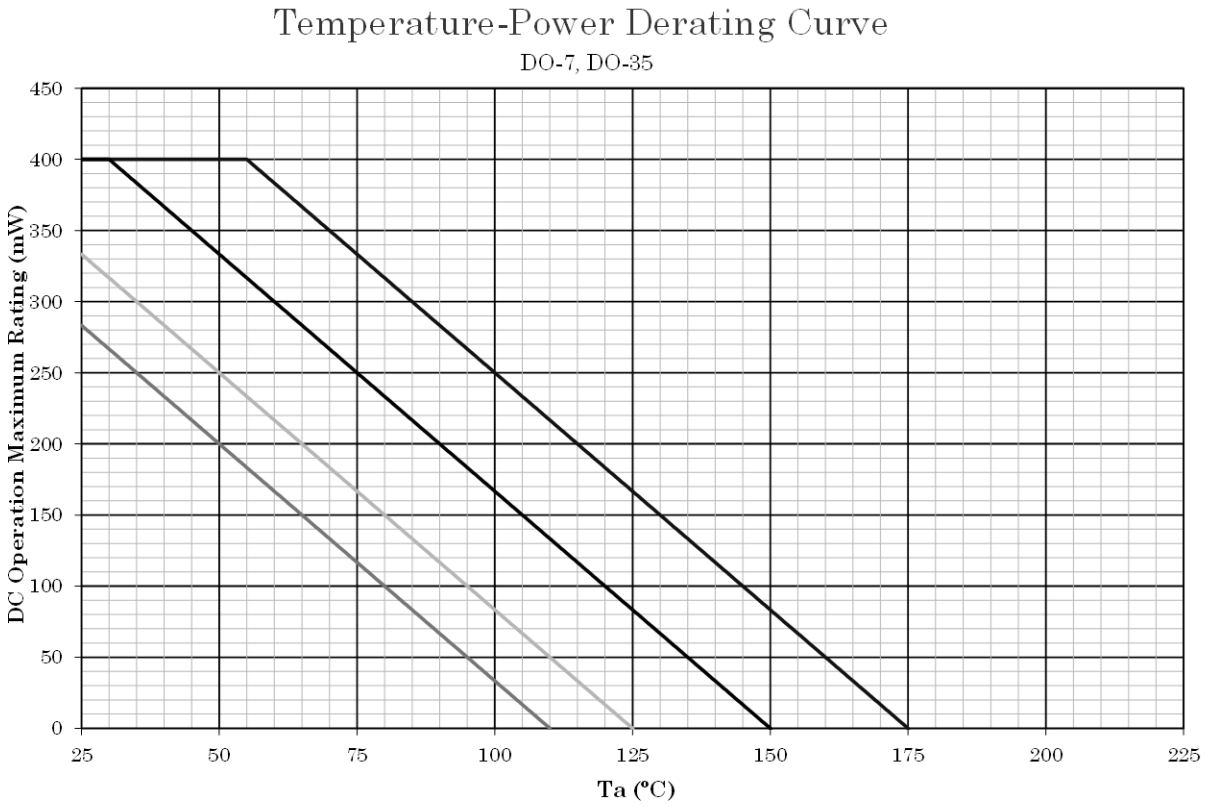
FIGURE 10. Temperature-power derating curve (DO-35).



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Temperature-power derating curve (DO-213AA).

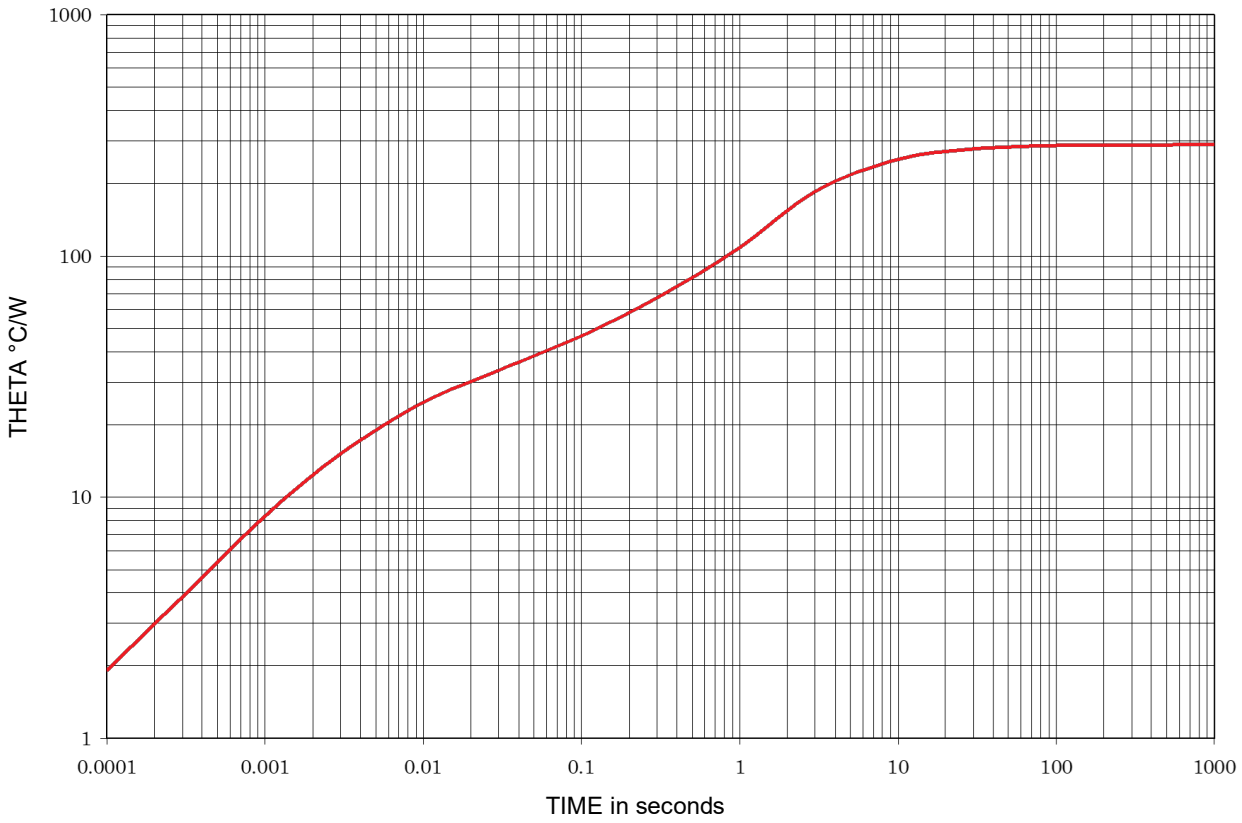


Thermal resistance junction to PCB = 300°C/W

NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

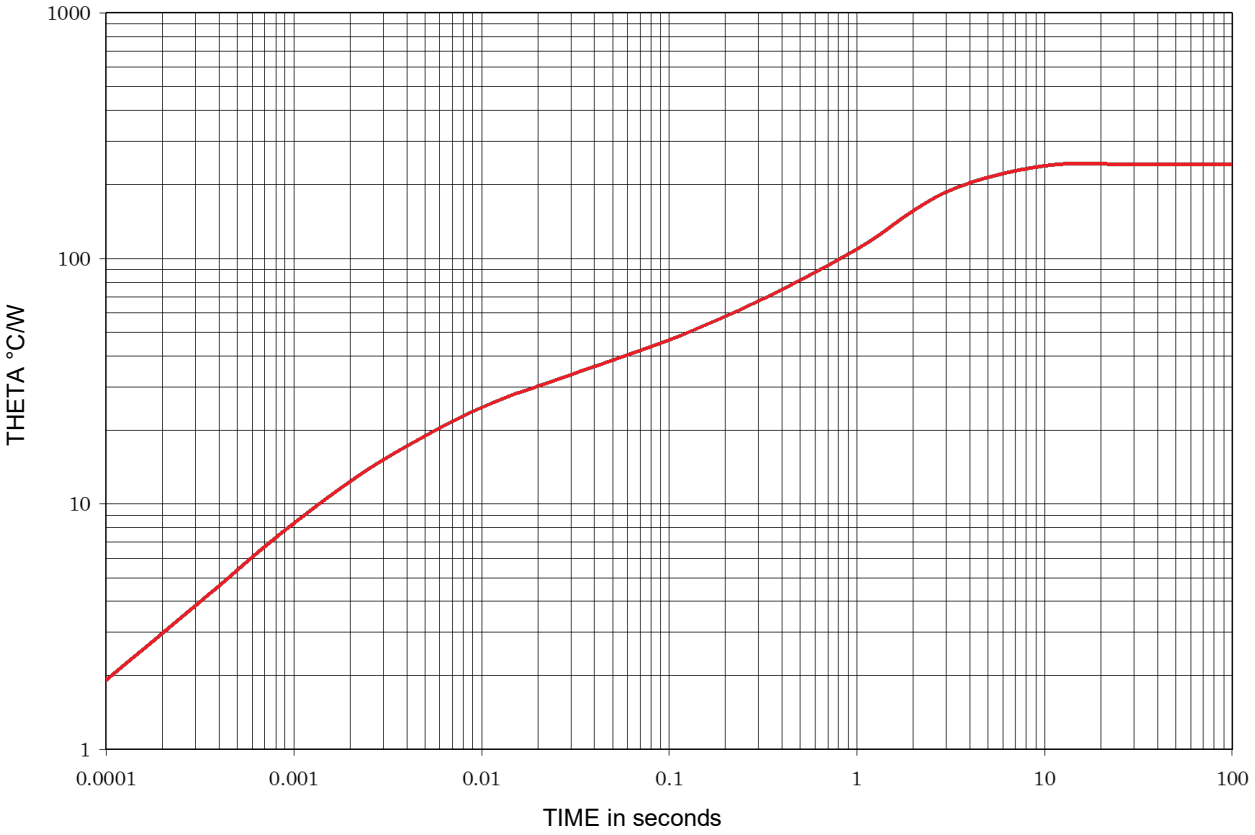
FIGURE 12. Temperature-power derating curve (DO-35 on PCB).



NOTES:

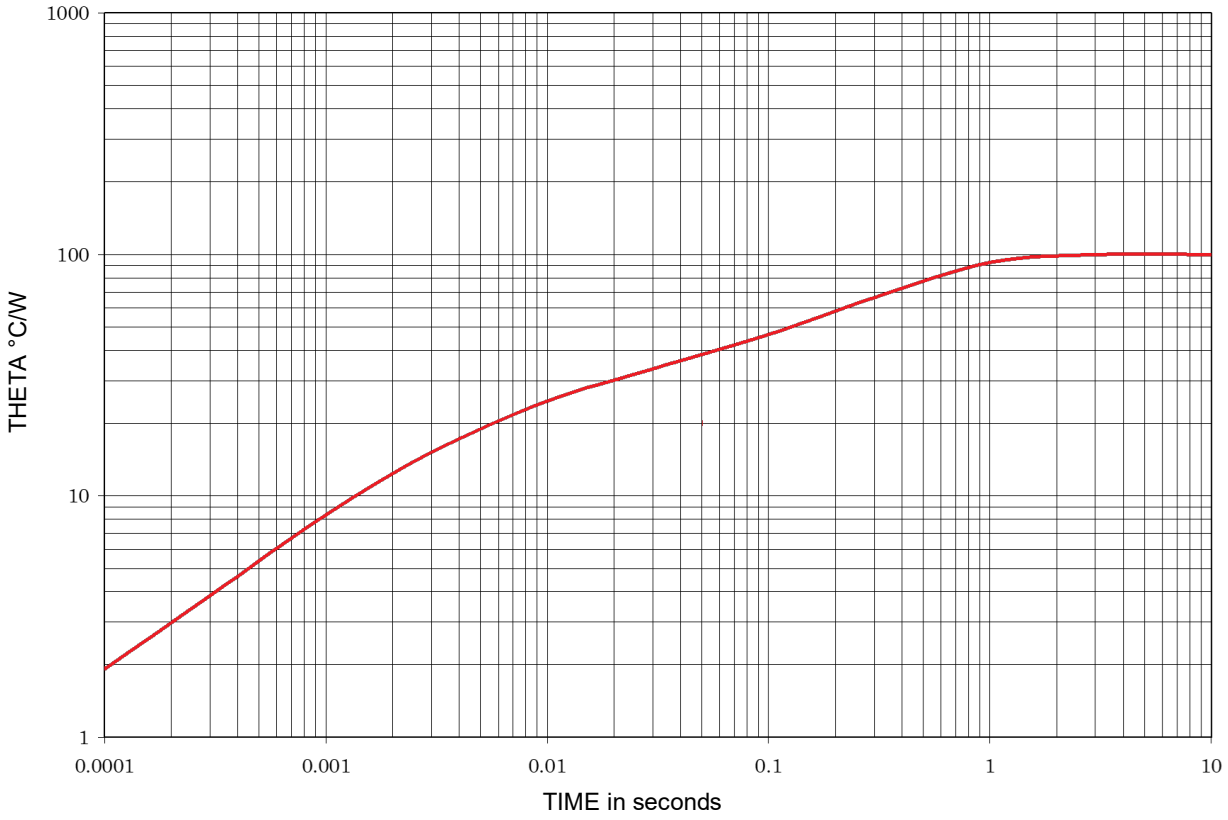
1. Thermal impedance testing for DO-35 axial leaded or UR when mounted to PCB. T_A = +25°C for both axial leaded and UR packages.
2. PCB details are as follows. Material is FR4 (.0625 inch (1.59 mm) thick, 1-layer of 1 oz Cu. PCB land sizes for axial leaded devices is 3.6 inches (92 mm) diameter with .125 inch (3.18 mm) lead length. PCB pad sizes for UR devices = 2.0 x 3.4 inches (50 x 87 mm) pads.
3. Thermal resistance = 300°C/W.

FIGURE 13. Thermal impedance DO-35 and UR, junction to ambient including PCB mount.



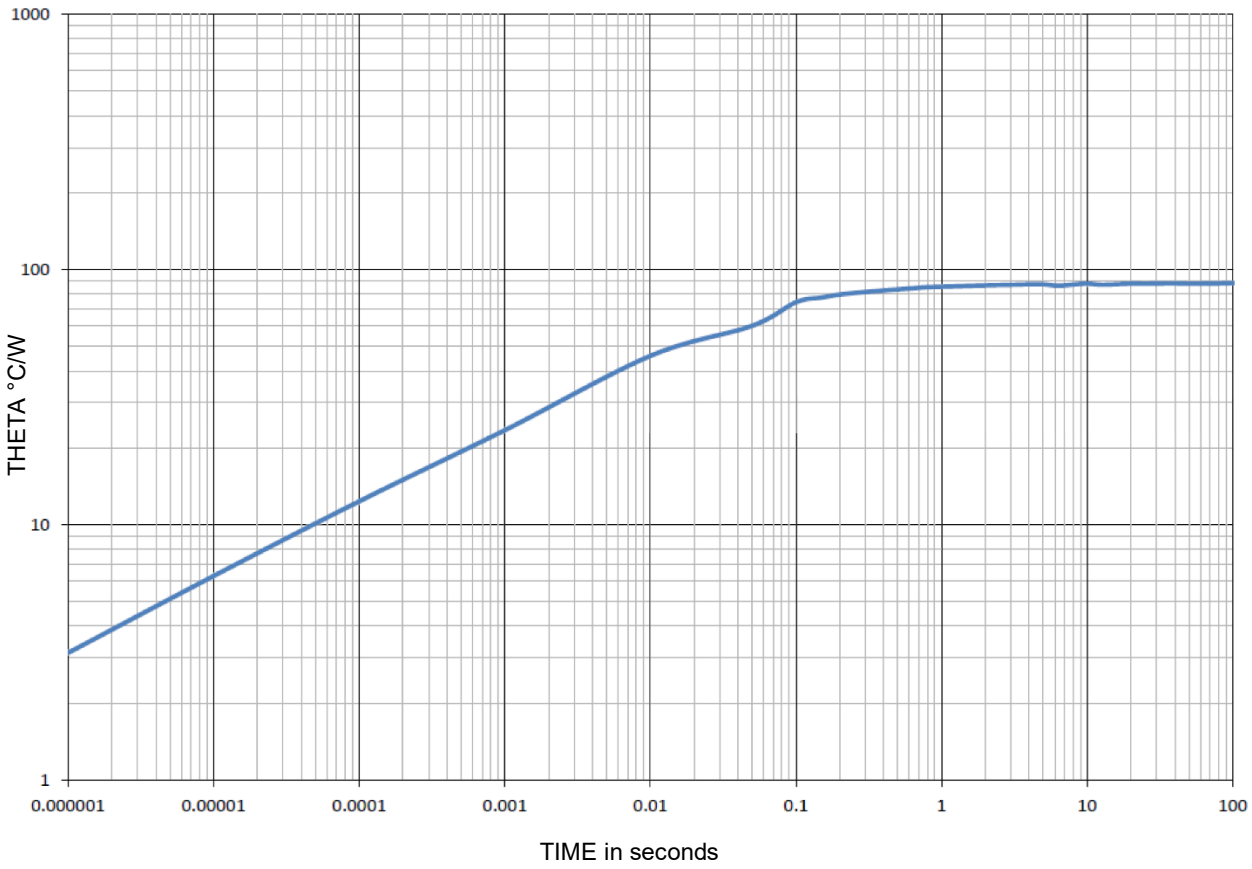
NOTES:
1. Thermal impedance DO-35 axial leaded, T_L = 25°C at L = .375 inch (9.525 mm) from body.
2. $R_{\theta JL}$ = 250°C/W.

FIGURE 14. Thermal impedance DO-35 axial leaded only, junction to lead.



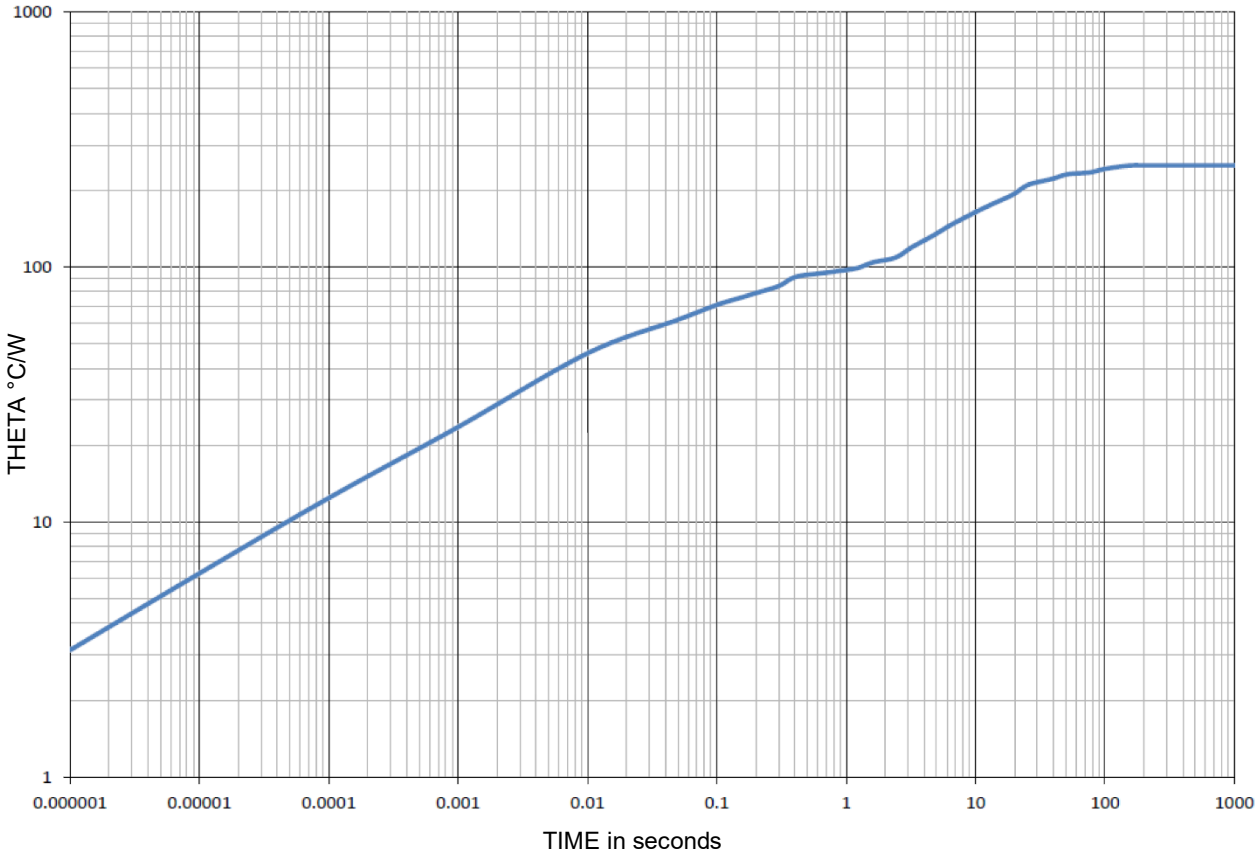
NOTES:
1. Thermal impedance UR DO-213A MELF, T_{EC} = 25°C.
2. Thermal resistance $R_{\theta JEC}$ = 100°C/W.

FIGURE 15. Thermal impedance UR (DO-213A MELF) junction to end-caps.



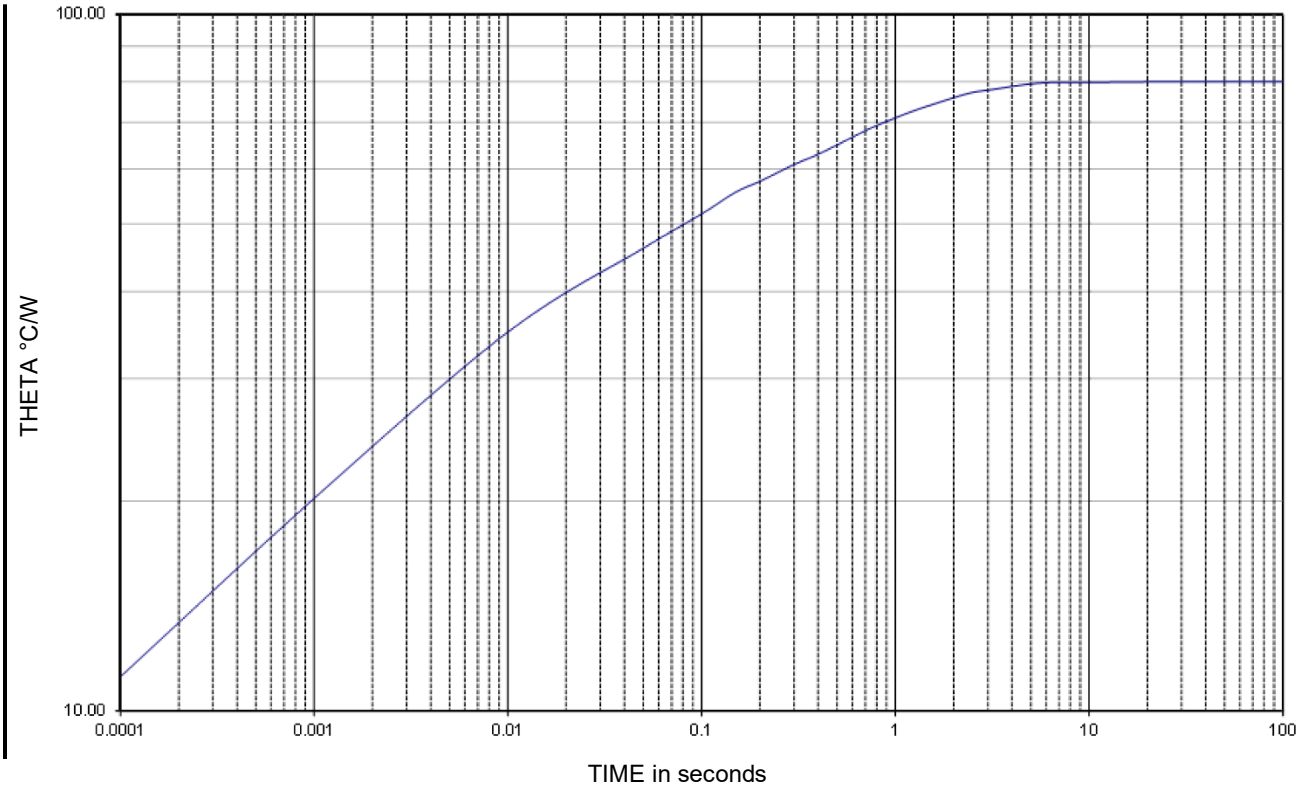
NOTES:
1. $R_{\theta JPCB(IS)}$ = 90°C/W.
2. $Z_{\theta JX}$ = 45°C/W maximum at 10 ms.

FIGURE 16 Thermal impedance $R_{\theta JSP(IS)}$ UB and UB2 devices.



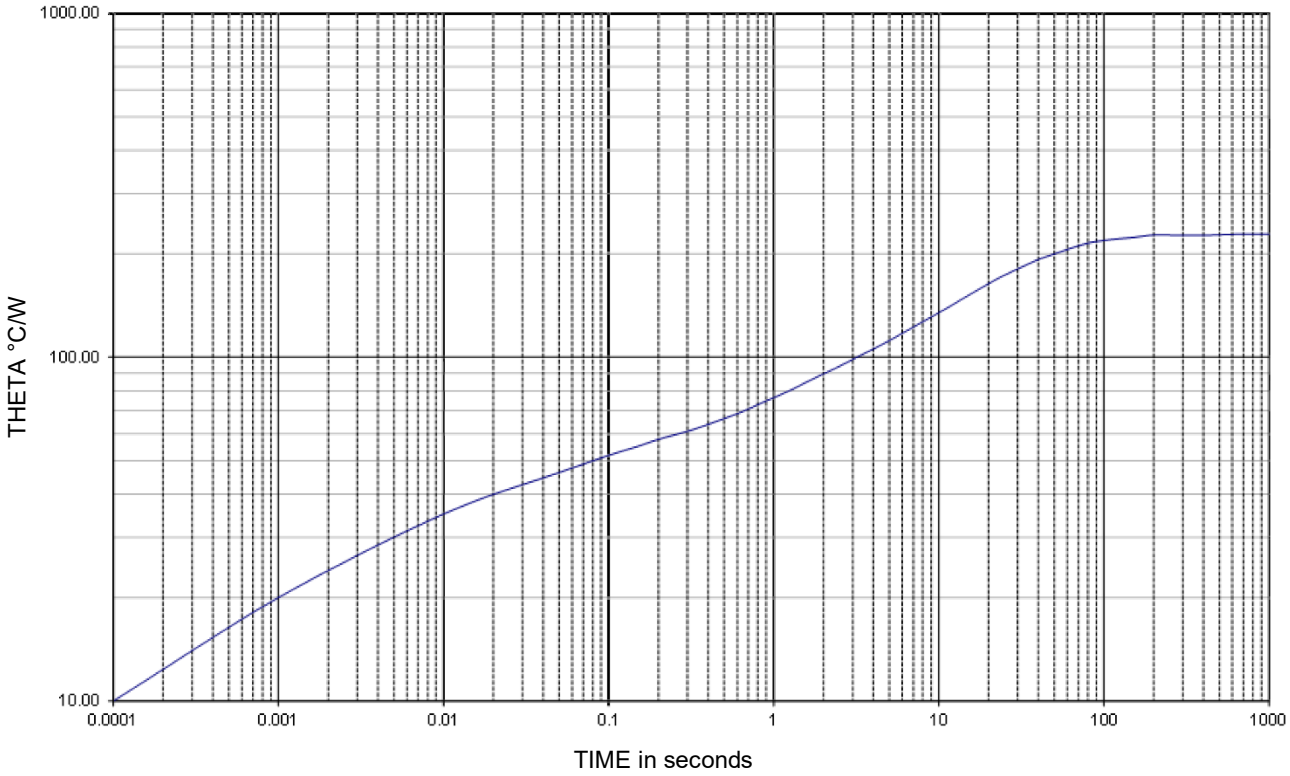
NOTES:
1. $R_{\theta JA(PCB)}$ = 250°C/W.
2. $Z_{\theta JX}$ = 45°C/W maximum at 10 ms.

FIGURE 17 Thermal impedance $R_{\theta JA(PCB)}$ for UB and UB2 devices.



NOTES:
1. $R_{\theta JA(PCB)}$ = 80°C/W.
2. $Z_{\theta JX}$ = 35°C/W maximum at 10 ms.

FIGURE 18. Thermal impedance $R_{\theta JSP(IS)}$ for UD devices.



NOTES:
1. $R_{\theta JA(PCB)}$ = 228°C/W.
2. $Z_{\theta JX}$ = 35°C/W maximum at 10 ms.

FIGURE 19. Thermal impedance $R_{\theta JA(PCB)}$ for UD devices.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

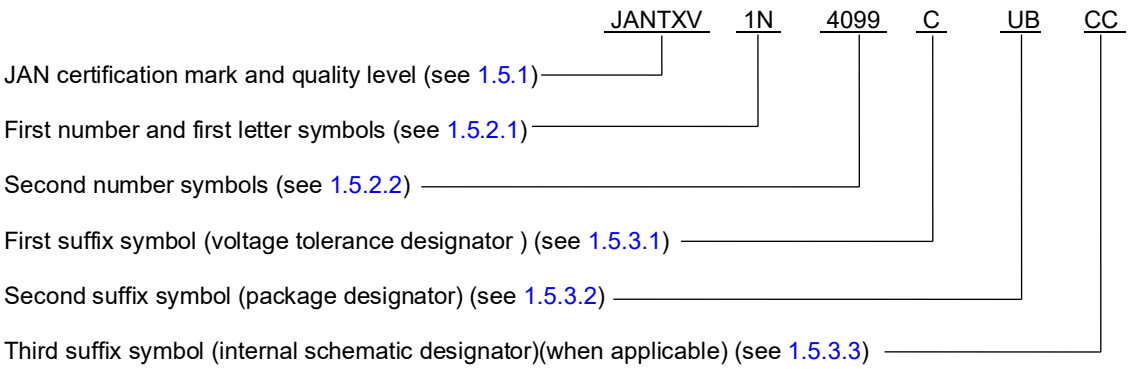
c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.4.

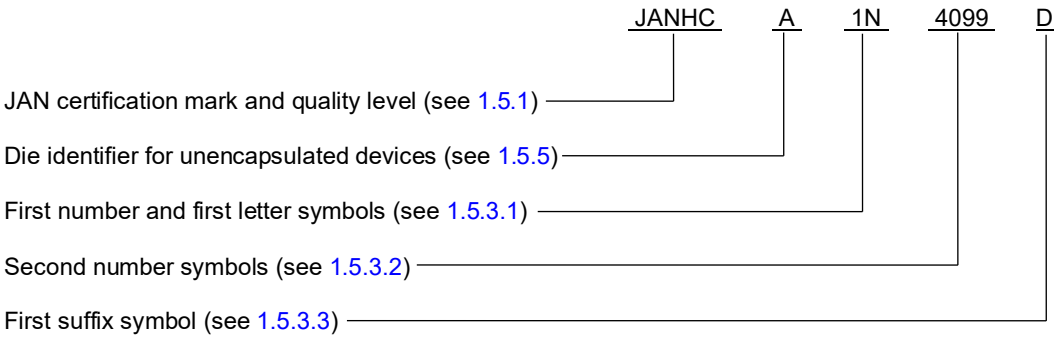
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Weapons Support, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at http://qpldocs.dla.mil.

6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.4.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.5 List of PINs.

6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N4099#$	JANTX1N4099#$	JANTXV1N4099#$	JANS1N4099#$
JAN1N4100#$	JANTX1N4100#$	JANTXV1N4100#$	JANS1N4100#$
JAN1N4101#$	JANTX1N4101#$	JANTXV1N4101#$	JANS1N4101#$
JAN1N4102#$	JANTX1N4102#$	JANTXV1N4102#$	JANS1N4102#$
JAN1N4103#$	JANTX1N4103#$	JANTXV1N4103#$	JANS1N4103#$
JAN1N4104#$	JANTX1N4104#$	JANTXV1N4104#$	JANS1N4104#$
JAN1N4105#$	JANTX1N4105#$	JANTXV1N4105#$	JANS1N4105#$
JAN1N4106#$	JANTX1N4106#$	JANTXV1N4106#$	JANS1N4106#$
JAN1N4107#$	JANTX1N4107#$	JANTXV1N4107#$	JANS1N4107#$
JAN1N4108#$	JANTX1N4108#$	JANTXV1N4108#$	JANS1N4108#$
JAN1N4109#$	JANTX1N4109#$	JANTXV1N4109#$	JANS1N4109#$
JAN1N4110#$	JANTX1N4110#$	JANTXV1N4110#$	JANS1N4110#$
JAN1N4111#$	JANTX1N4111#$	JANTXV1N4111#$	JANS1N4111#$
JAN1N4112#$	JANTX1N4112#$	JANTXV1N4112#$	JANS1N4112#$
JAN1N4113#$	JANTX1N4113#$	JANTXV1N4113#$	JANS1N4113#$
JAN1N4114#$	JANTX1N4114#$	JANTXV1N4114#$	JANS1N4114#$
JAN1N4115#$	JANTX1N4115#$	JANTXV1N4115#$	JANS1N4115#$
JAN1N4116#$	JANTX1N4116#$	JANTXV1N4116#$	JANS1N4116#$
JAN1N4117#$	JANTX1N4117#$	JANTXV1N4117#$	JANS1N4117#$
JAN1N4118#$	JANTX1N4118#$	JANTXV1N4118#$	JANS1N4118#$

See footnotes at end of table.

6.5.1 List of PINs for encapsulated devices. Continued.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N4119#$	JANTX1N4119#$	JANTXV1N4119#$	JANS1N4119#$
JAN1N4120#$	JANTX1N4120#$	JANTXV1N4120#$	JANS1N4120#$
JAN1N4121#$	JANTX1N4121#$	JANTXV1N4121#$	JANS1N4121#$
JAN1N4122#$	JANTX1N4122#$	JANTXV1N4122#$	JANS1N4122#$
JAN1N4123#$	JANTX1N4123#$	JANTXV1N4123#$	JANS1N4123#$
JAN1N4124#$	JANTX1N4124#$	JANTXV1N4124#$	JANS1N4124#$
JAN1N4125#$	JANTX1N4125#$	JANTXV1N4125#$	JANS1N4125#$
JAN1N4126#$	JANTX1N4126#$	JANTXV1N4126#$	JANS1N4126#$
JAN1N4127#$	JANTX1N4127#$	JANTXV1N4127#$	JANS1N4127#$
JAN1N4128#$	JANTX1N4128#$	JANTXV1N4128#$	JANS1N4128#$
JAN1N4129#$	JANTX1N4129#$	JANTXV1N4129#$	JANS1N4129#$
JAN1N4130#$	JANTX1N4130#$	JANTXV1N4130#$	JANS1N4130#$
JAN1N4131#$	JANTX1N4131#$	JANTXV1N4131#$	JANS1N4131#$
JAN1N4132#$	JANTX1N4132#$	JANTXV1N4132#$	JANS1N4132#$
JAN1N4133#$	JANTX1N4133#$	JANTXV1N4133#$	JANS1N4133#$
JAN1N4134#$	JANTX1N4134#$	JANTXV1N4134#$	JANS1N4134#$
JAN1N4135#$	JANTX1N4135#$	JANTXV1N4135#$	JANS1N4135#$
JAN1N4614#$	JANTX1N4614#$	JANTXV1N4614#$	JANS1N4614#$
JAN1N4615#$	JANTX1N4615#$	JANTXV1N4615#$	JANS1N4615#$
JAN1N4616#$	JANTX1N4616#$	JANTXV1N4616#$	JANS1N4616#$
JAN1N4617#$	JANTX1N4617#$	JANTXV1N4617#$	JANS1N4617#$
JAN1N4618#$	JANTX1N4618#$	JANTXV1N4618#$	JANS1N4618#$
JAN1N4619#$	JANTX1N4619#$	JANTXV1N4619#$	JANS1N4619#$
JAN1N4620#$	JANTX1N4620#$	JANTXV1N4620#$	JANS1N4620#$
JAN1N4621#$	JANTX1N4621#$	JANTXV1N4621#$	JANS1N4621#$
JAN1N4622#$	JANTX1N4622#$	JANTXV1N4622#$	JANS1N4622#$
JAN1N4623#$	JANTX1N4623#$	JANTXV1N4623#$	JANS1N4623#$
JAN1N4624#$	JANTX1N4624#$	JANTXV1N4624#$	JANS1N4624#$
JAN1N4625#$	JANTX1N4625#$	JANTXV1N4625#$	JANS1N4625#$
JAN1N4626#$	JANTX1N4626#$	JANTXV1N4626#$	JANS1N4626#$
JAN1N4627#$	JANTX1N4627#$	JANTXV1N4627#$	JANS1N4627#$

(1) The pound sign (#) represents the first suffix symbol (voltage tolerance designator) see 1.5.3.3. The dollar sign ($) represents the second suffix symbol (package designator), see 1.5.3.2.

6.5.2 List of PINs for unencapsulated devices. The following is a list of possible PINs available on this specification sheet. The qualified die suppliers with the applicable letter version (e.g., JANHCA1N4614) will be identified on the QML.

JANC ordering information					
PIN (1)	Manufacturer CAGE				
	43611 (2)	12954 (2)	52GC4 (2)	13409 (2)	52GC4 (2)
1N4614-1	JANHCA1N4614	JANHCB1N4614	JANHCC1N4614	JANHCD1N4614	JANHCE1N4614
1N4615-1	JANHCA1N4615	JANHCB1N4615	JANHCC1N4615	JANHCD1N4615	JANHCE1N4615
1N4616-1	JANHCA1N4616	JANHCB1N4616	JANHCC1N4616	JANHCD1N4616	JANHCE1N4616
1N4617-1	JANHCA1N4617	JANHCB1N4617	JANHCC1N4617	JANHCD1N4617	JANHCE1N4617
1N4618-1	JANHCA1N4618	JANHCB1N4618	JANHCC1N4618	JANHCD1N4618	JANHCE1N4618
1N4619-1	JANHCA1N4619	JANHCB1N4619	JANHCC1N4619	JANHCD1N4619	JANHCE1N4619
1N4620-1	JANHCA1N4620	JANHCB1N4620	JANHCC1N4620	JANHCD1N4620	JANHCE1N4620
1N4621-1	JANHCA1N4621	JANHCB1N4621	JANHCC1N4621	JANHCD1N4621	JANHCE1N4621
1N4622-1	JANHCA1N4622	JANHCB1N4622	JANHCC1N4622	JANHCD1N4622	JANHCE1N4622
1N4623-1	JANHCA1N4623	JANHCB1N4623	JANHCC1N4623	JANHCD1N4623	JANHCE1N4623
1N4624-1	JANHCA1N4624	JANHCB1N4624	JANHCC1N4624	JANHCD1N4624	JANHCE1N4624
1N4625-1	JANHCA1N4625	JANHCB1N4625	JANHCC1N4625	JANHCD1N4625	JANHCE1N4625
1N4626-1	JANHCA1N4626	JANHCB1N4626	JANHCC1N4626	JANHCD1N4626	JANHCE1N4626
1N4627-1	JANHCA1N4627	JANHCB1N4627	JANHCC1N4627	JANHCD1N4627	JANHCE1N4627
1N4099-1	JANHCA1N4099	JANHCB1N4099	JANHCC1N4099	JANHCD1N4099	JANHCE1N4099
1N4100-1	JANHCA1N4100	JANHCB1N4100	JANHCC1N4100	JANHCD1N4100	JANHCE1N4100
1N4101-1	JANHCA1N4101	JANHCB1N4101	JANHCC1N4101	JANHCD1N4101	JANHCE1N4101
1N4102-1	JANHCA1N4102	JANHCB1N4102	JANHCC1N4102	JANHCD1N4102	JANHCE1N4102
1N4103-1	JANHCA1N4103	JANHCB1N4103	JANHCC1N4103	JANHCD1N4103	JANHCE1N4103
1N4104-1	JANHCA1N4104	JANHCB1N4104	JANHCC1N4104	JANHCD1N4104	JANHCE1N4104
1N4105-1	JANHCA1N4105	JANHCB1N4105	JANHCC1N4105	JANHCD1N4105	JANHCE1N4105
1N4106-1	JANHCA1N4106	JANHCB1N4106	JANHCC1N4106	JANHCD1N4106	JANHCE1N4106
1N4107-1	JANHCA1N4107	JANHCB1N4107	JANHCC1N4107	JANHCD1N4107	JANHCE1N4107
1N4108-1	JANHCA1N4108	JANHCB1N4108	JANHCC1N4108	JANHCD1N4108	JANHCE1N4108
1N4109-1	JANHCA1N4109	JANHCB1N4109	JANHCC1N4109	JANHCD1N4109	JANHCE1N4109
1N4110-1	JANHCA1N4110	JANHCB1N4110	JANHCC1N4110	JANHCD1N4110	JANHCE1N4110
1N4111-1	JANHCA1N4111	JANHCB1N4111	JANHCC1N4111	JANHCD1N4111	JANHCE1N4111
1N4112-1	JANHCA1N4112	JANHCB1N4112	JANHCC1N4112	JANHCD1N4112	JANHCE1N4112
1N4113-1	JANHCA1N4113	JANHCB1N4113	JANHCC1N4113	JANHCD1N4113	JANHCE1N4113
1N4114-1	JANHCA1N4114	JANHCB1N4114	JANHCC1N4114	JANHCD1N4114	JANHCE1N4114
1N4115-1	JANHCA1N4115	JANHCB1N4115	JANHCC1N4115	JANHCD1N4115	JANHCE1N4115
1N4116-1	JANHCA1N4116	JANHCB1N4116	JANHCC1N4116	JANHCD1N4116	JANHCE1N4116
1N4117-1	JANHCA1N4117	JANHCB1N4117	JANHCC1N4117	JANHCD1N4117	JANHCE1N4117
1N4118-1	JANHCA1N4118	JANHCB1N4118	JANHCC1N4118	JANHCD1N4118	JANHCE1N4118
1N4119-1	JANHCA1N4119	JANHCB1N4119	JANHCC1N4119	JANHCD1N4119	JANHCE1N4119
1N4120-1	JANHCA1N4120	JANHCB1N4120	JANHCC1N4120	JANHCD1N4120	JANHCE1N4120
1N4121-1	JANHCA1N4121	JANHCB1N4121	JANHCC1N4121	JANHCD1N4121	JANHCE1N4121
1N4122-1	JANHCA1N4122	JANHCB1N4122	JANHCC1N4122	JANHCD1N4122	JANHCE1N4122
1N4123-1	JANHCA1N4123	JANHCB1N4123	JANHCC1N4123	JANHCD1N4123	JANHCE1N4123
1N4124-1	JANHCA1N4124	JANHCB1N4124	JANHCC1N4124	JANHCD1N4124	JANHCE1N4124
1N4125-1	JANHCA1N4125	JANHCB1N4125	JANHCC1N4125	JANHCD1N4125	JANHCE1N4125
1N4126-1	JANHCA1N4126	JANHCB1N4126	JANHCC1N4126	JANHCD1N4126	JANHCE1N4126
1N4127-1	JANHCA1N4127	JANHCB1N4127	JANHCC1N4127	JANHCD1N4127	JANHCE1N4127
1N4128-1	JANHCA1N4128	JANHCB1N4128	JANHCC1N4128	JANHCD1N4128	JANHCE1N4128
1N4129-1	JANHCA1N4129	JANHCB1N4129	JANHCC1N4129	JANHCD1N4129	JANHCE1N4129
1N4130-1	JANHCA1N4130	JANHCB1N4130	JANHCC1N4130	JANHCD1N4130	JANHCE1N4130
1N4131-1	JANHCA1N4131	JANHCB1N4131	JANHCC1N4131	JANHCD1N4131	JANHCE1N4131
1N4132-1	JANHCA1N4132	JANHCB1N4132	JANHCC1N4132	JANHCD1N4132	JANHCE1N4132
1N4133-1	JANHCA1N4133	JANHCB1N4133	JANHCC1N4133	JANHCD1N4133	JANHCE1N4133
1N4134-1	JANHCA1N4134	JANHCB1N4134	JANHCC1N4134	JANHCD1N4134	JANHCE1N4134
1N4135-1	JANHCA1N4135	JANHCB1N4135	JANHCC1N4135	JANHCD1N4135	JANHCE1N4135

(1) C and D tolerance suffix are applicable to JANC chips.
(2) For JANKC level, replace "JANHC" with "JANKC".

6.6 Substitution information.

6.6.1 Substitutability of 2 percent and 1 percent tolerance devices. Devices of tighter tolerance are a direct one way substitute for the looser tolerance devices (example: JANTX1N4614D-1 substitutes for JANTX1N4614-1).

6.6.2 Substitutability of dash-one parts. Non-dash-one devices have been deleted from this specification. Dash-one devices are a direct substitute for non dash-one devices and are preferred. The following table shows the direct substitutability.

Superseded part number	Superseding part number		Superseded part number	Superseding part number		Superseded part number	Superseding part number
1N4614	1N4614-1		1N4102	1N4102-1		1N4119	1N4119-1
1N4615	1N4615-1		1N4103	1N4103-1		1N4120	1N4120-1
1N4616	1N4616-1		1N4104	1N4104-1		1N4121	1N4121-1
1N4617	1N4617-1		1N4105	1N4105-1		1N4122	1N4122-1
1N4618	1N4618-1		1N4106	1N4106-1		1N4123	1N4123-1
1N4619	1N4619-1		1N4107	1N4107-1		1N4124	1N4124-1
1N4620	1N4620-1		1N4108	1N4108-1		1N4125	1N4125-1
1N4621	1N4621-1		1N4109	1N4109-1		1N4126	1N4126-1
1N4622	1N4622-1		1N4110	1N4110-1		1N4127	1N4127-1
1N4623	1N4623-1		1N4111	1N4111-1		1N4128	1N4128-1
1N4624	1N4624-1		1N4112	1N4112-1		1N4129	1N4129-1
1N4625	1N4625-1		1N4113	1N4113-1		1N4130	1N4130-1
1N4626	1N4626-1		1N4114	1N4114-1		1N4131	1N4131-1
1N4627	1N4627-1		1N4115	1N4115-1		1N4132	1N4132-1
1N4099	1N4099-1		1N4116	1N4116-1		1N4133	1N4133-1
1N4100	1N4100-1		1N4117	1N4117-1		1N4134	1N4134-1
1N4101	1N4101-1		1N4118	1N4118-1		1N4135	1N4135-1

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Weapons Support, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218−3990 or by electronic mail at Semiconductor@.dla.mil .

6.8 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
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Navy − SH
Air Force − 85
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DLA − CC

Review activities:
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Preparing activity:
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