

The documentation and process conversion measures necessary to comply with this revision shall be completed by 28 November 2025.

INCH-POUND

MIL-PRF-19500/337M
AMENDMENT 1
27 August 2025
SUPERSEDING
MIL-PRF-19500/337M
24 June 2020

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SWITCHING, DEVICE TYPES 1N4153 AND 1N4534, ENCAPSULATED AND UN-ENCAPSULATED, QUALITY LEVELS JAN, JANTX, JANTXV, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for controlled forward voltage switching diodes. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#). Two levels of product assurance (JANHC and JANKC) are provided for each un-encapsulated device type.

1.2 Package outlines. The device package outlines for the encapsulated device types are as follows: Round body, axial leaded in accordance with [figure 1](#), round terminal surface mount device (SMD) package in accordance with [figure 2](#), UB SMD package in accordance with [figure 3](#) and UD SMD package in accordance with [figure 4](#). The dimensions and topography for JANHC and JANKC un-encapsulated die is in accordance with [figure 5](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Types	V _{BR}	V _{RWM}	I _O (PCB) (1) (2)	I _{FSM} t _p = 8.3ms	R _θ JL (3) (4)	R _θ JEC (UR) (2)	R _θ JA(PCB) (2) (4) (5)	R _θ JSP (UB) (4) (5)	T _{STG} & T _J	
	<u>V_{dc}</u>	<u>V_(pk)</u>	<u>mA</u>	<u>A_(pk)</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C</u>	
1N4153-1	}	}	}	}	250	100	325		-65 to +175	
1N4153UR-1										
1N4153UB, UBN, UBCA, UBCC, UBD, UBND	100	75	200	2			}	120	-55 to +200	
1N4153UD	}	}								325
1N4534							250			
1N4534UR	}	}			}	}		100	}	120
1N4534UB, 1N4534UBN			100	75						
1N4534UD	75	50								

See footnotes on next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

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1.3 Maximum ratings – continued.

- (1) For temperature-current derating curves, see [figures 7 and 8](#).
- (2) $T_A = +75\text{ }^{\circ}\text{C}$ for both axial wire terminals and UR on printed circuit board (PCB), PCB = FR4 - .0625 inch (1.59 mm) 1-layer 1-Oz Cu, horizontal, in still air; pads for (UR) = .061 inch (1.55 mm) x .105 inch (2.67 mm); pads for axial = .092 inch (2.34 mm) diameter, strip = .030 inch (0.76 mm) x 1 inch (25.4 mm) long, lead length $L \leq .187$ inch (≤ 4.75 mm); $R_{\theta JA}$ with a defined PCB thermal resistance condition included, is measured at $I_O = 200$ mA dc.
- (3) $L = .375$ inch (9.53 mm).
- (4) See [figures 9, 10, 11, and 12](#) for thermal impedance curves.
- (5) $R_{\theta JSP}$ refers to thermal resistance from junction to the solder pads of the UB, UBN and UD package.

1.4 Primary electrical characteristics. Unless otherwise specified, at $T_A = +25\text{ }^{\circ}\text{C}$.

Limits	V_{F1} $I_F = 100\text{ }\mu\text{A dc}$	V_{F2} $I_F = 250\text{ }\mu\text{A dc}$	V_{F3} $I_F = 1\text{ mA dc}$	V_{F4} $I_F = 2\text{ mA dc}$	V_{F5} $I_F = 10\text{ mA dc}$	V_{F6} $I_F = 20\text{ mA dc}$
Min	0.490 V dc	0.530 V dc	0.590 V dc	0.620 V dc	0.700 V dc	0.740 V dc
Max	0.550 V dc	0.590 V dc	0.670 V dc	0.700 V dc	0.810 V dc	0.880 V dc

Limit	I_{R1} $V_R = 50\text{ V dc}$	I_{R2} $V_R = 50\text{ V dc}$ $T_A = 150\text{ }^{\circ}\text{C}$	C $V_R = 0\text{ V dc}$ $f = 1\text{ MHz}$	t_{rr} $I_F = I_R = 10\text{ mA dc}$ $R_L = 100\text{ ohms}$, $I_{RR} = 1.0\text{ mA dc}$
Max	50 nA dc	50 $\mu\text{A dc}$	2.0 pF	4 ns

- (1) Primary electrical characteristics for surface mount devices are equivalent to the corresponding non-surface mount devices unless otherwise specified.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#) and as specified herein. See [6.4](#) for PIN construction example, [6.5](#) for a list of available PINs, [6.6](#) and for supersession information.

1.5.1 JAN certification mark and quality level designators.

1.5.1.1 Encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

1.5.1.2 Un-encapsulated die. The quality level designators for un-encapsulated die that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

1.5.2 Device type. The designation system for the device types covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the semiconductors covered by this specification sheet are "4153" and "4534".

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1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN for this specification sheet.

1.5.3.1 Package designators. The suffix symbols (or lack thereof) that designate the package outline for the devices covered by this specification sheet are as follows:

Blank	A blank designator identifies the outline as a round glass body, axial wire terminal package similar to a DO-204AG (formerly DO-34) in accordance with figure 1 (1N4534 only).
-1	This designator identifies the outline as a round glass body, axial wire terminal package similar to a DO-204AH (formerly DO-35) in accordance with figure 1 (1N4153 only). This construction uses a dash-one construction in accordance with MIL-PRF-19500 .
UR-1	This designator identifies the outline as a two terminal, round metal electrode leadless face (MELF) DO-213AA SMD package leadless face in accordance with figure 2 . This construction uses a dash-one construction in accordance with MIL-PRF-19500 (1N4153 only).
UB	This designator identifies the outline as a 3 terminal, 4 pad, metal lid (used as a shield and connected to fourth pad) SMD package in accordance with figure 3 (1N4153 and 1N4534).
UBN	This designator identifies a 3-terminal, 3 pad isolated metal lid SMD package in accordance with figure 3 .
UD	This designator identifies a 2 terminal, 3 pad, metal lid SMD package in accordance with figure 4 .

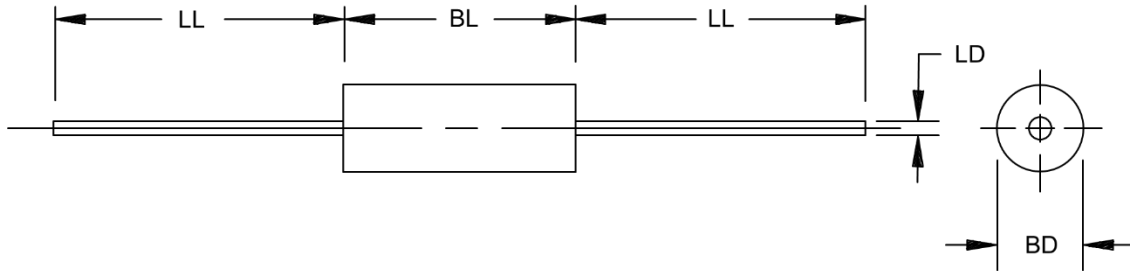
1.5.3.2 Internal circuit schematic designators. The suffix symbols that designate the internal circuit schematic of the dual die (1N4153 only) configurations of the UB and UBN cavity style package covered by [figure 6](#) are as follows:

CA	This designator identifies a common anode internal circuit schematic configuration.
CC	This designator identifies a common cathode internal circuit schematic configuration.
D	This designator identifies a doubler internal circuit schematic configuration.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

1.5.5 Die identifiers for un-encapsulated devices. The manufacturer die identifiers that are applicable for this specification sheet is "A" (see [figure 5](#)).

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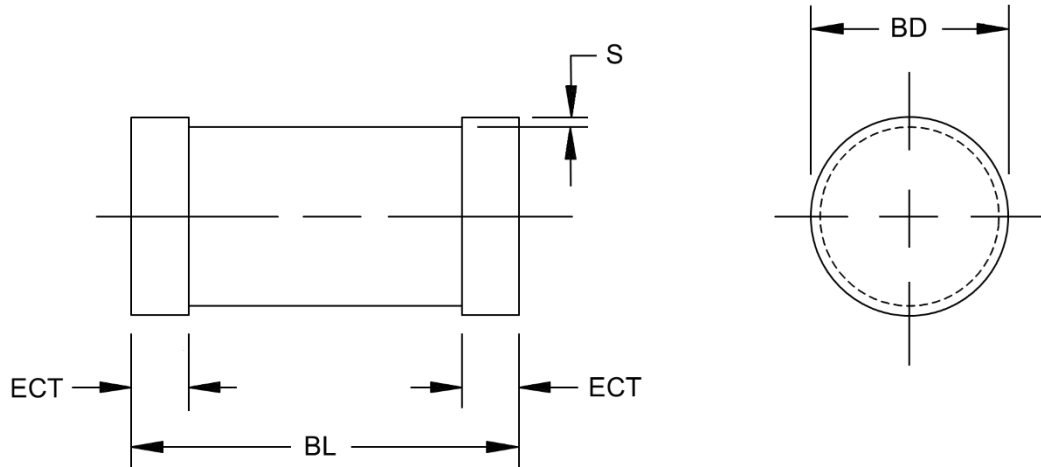
Symbol	Dimensions 1N4153-1 (DO-204AH)				Symbol	Dimensions 1N4534 (DO-204AG)			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
BD	.056	.075	1.42	1.91	BD	.050	.075	1.27	1.91
BL	.140	.180	3.56	4.57	BL	.080	.120	2.03	3.05
LD	.018	.022	0.46	0.56	LD	.018	.022	0.46	0.56
LL	1.000	1.500	25.40	38.10	LL	1.000	1.500	25.40	38.10

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.

FIGURE 1. Physical dimensions of round body, axial leaded DO-204AG and DO-204AH packages.

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Symbol	Dimensions			
	inch	Inch	mm	mm
	Min	Max	Min	Max
BD	.063	.067	1.60	1.70
BL	.130	.146	3.30	3.70
ECT	.016	.022	0.41	0.55
S	.001 reference		0.03 reference	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.
3. Dimension S is optional however dimension BD (glass body) shall not exceed endcap diameter.

FIGURE 2. Physical dimensions for round body, leadless face surface mount (DO-213AA) package.

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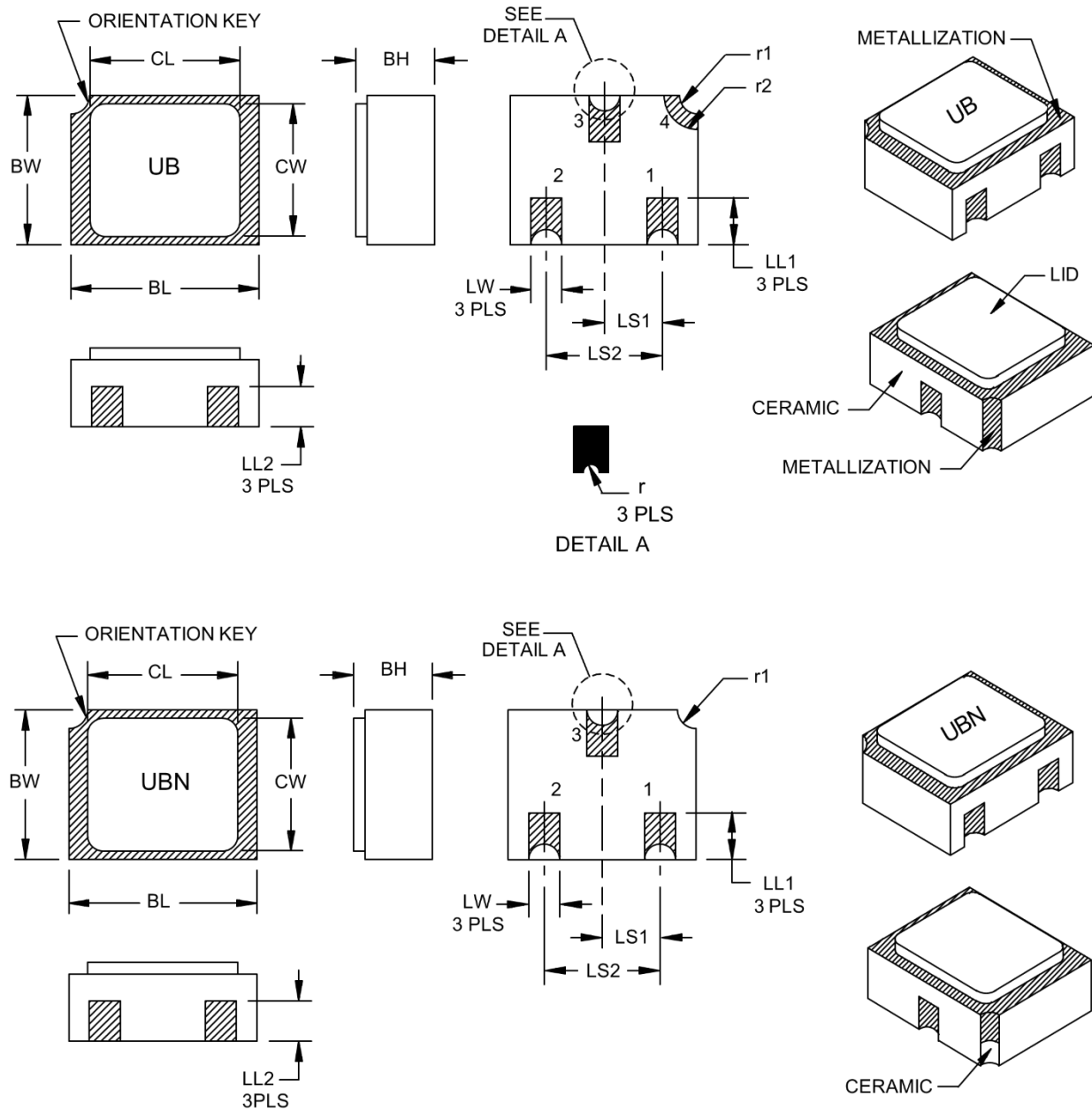


FIGURE 3. Physical dimensions for UB and UBN style surface mount package.

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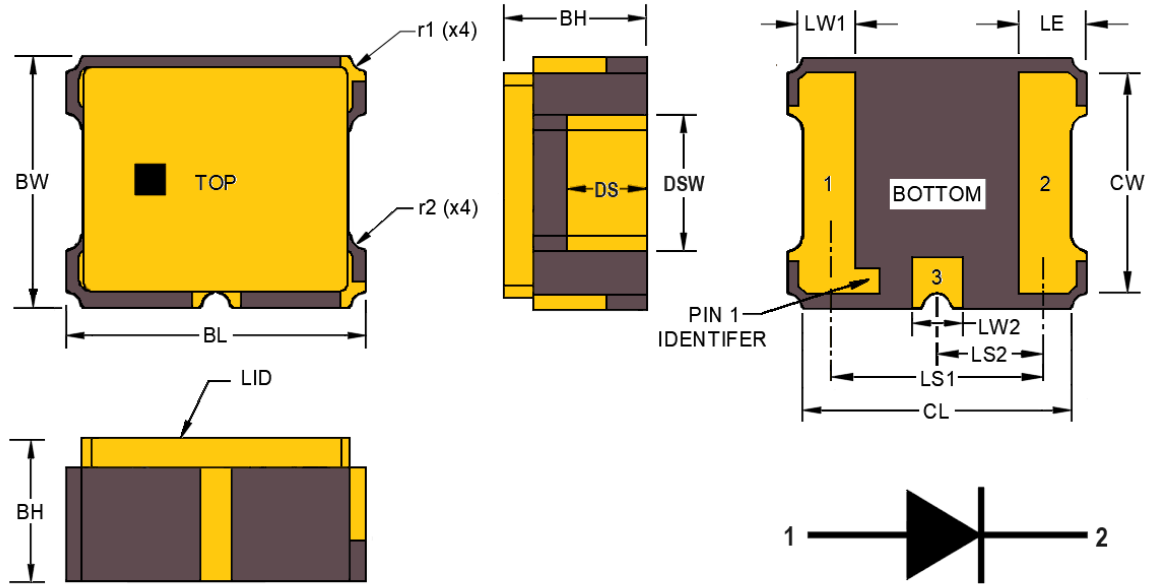
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
BH	.046	.056	1.17	1.42	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.97	
LL2	.014	.036	0.36	0.89	
LS1	.035	.040	0.89	1.02	
LS2	.071	.079	1.80	2.01	
LW	.016	.024	0.41	0.61	
r		.008		0.20	
r1		.012		0.30	
r2		.022		0.56	3

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Hatched areas on package denote metallized areas. Pad 4 (UB only) = shielding connected to the lid.
3. UB only. For design reference only.

FIGURE 3. Physical dimensions for UB and UBN style surface mount package - Continued.

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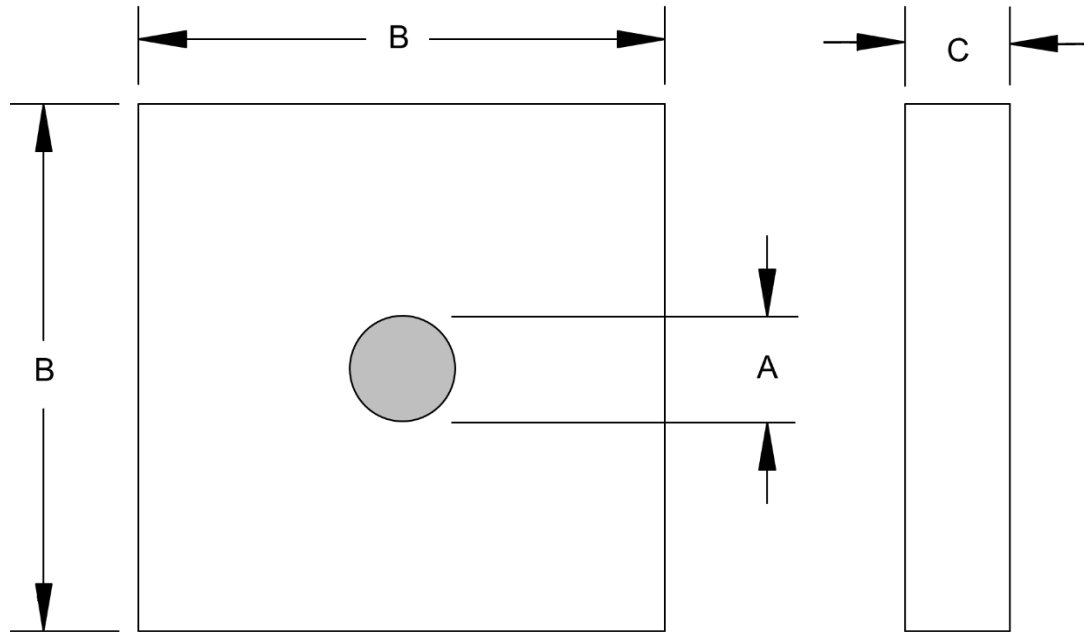


Symbol	Inches	Inches	mm	mm	Symbol	Inches	Inches	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
BH	0.078	0.092	1.979	2.329	LE	0.021	0.033	0.540	0.840
BL	0.112	0.128	2.850	3.250	LS1	0.085	0.093	2.160	2.360
BW	0.092	0.108	2.340	2.740	LS2	0.043	0.047	1.080	1.180
CL	0.103	0.113	2.620	2.880	LW1	0.019	0.027	0.490	0.690
CW	0.083	0.093	2.120	2.360	LW2	0.019	0.021	0.490	0.530
DS	0.028	0.034	0.720	0.880	r1		0.006		0.150
DSW	0.051	0.057	1.330	1.430	r2		0.006		0.150

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Pad 3 is connected to the lid braze ring for shielding.
3. Cathode marked with a square.
4. Pads 1 and 2 layout is equivalent to those for 1N4153UR-1.
5. Diode outline shown in ISO third angle projection.

FIGURE 4. Physical dimensions of UD cavity style surface mount package.



Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0059	.0061	0.150	0.155
B	.0130	.0170	0.330	0.432
C	.0080	.0120	0.203	0.305

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. The metallization characteristics of the die are as follows:
Top (anode): Al. Al thickness: 25,000 Å minimum.
Back (cathode): Au. Gold thickness: 4,000 Å minimum.

FIGURE 5. Physical dimensions, JANHCA and JANKCA die.

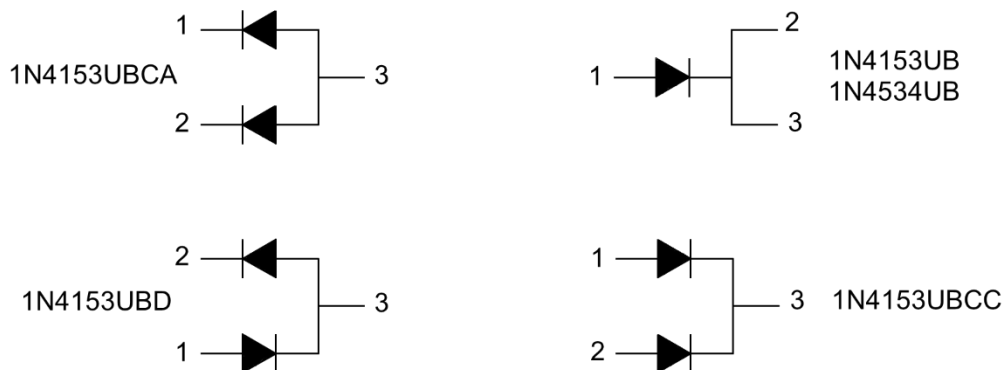


FIGURE 6. Internal schematic circuits for UB package dual and single die configurations.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figures 1](#) (axial leads), [2](#) (DO-213AA), [3](#) (UB and UBN), [4](#) (UD) and [5](#) (die).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Diode construction.

3.4.2.1 Axial packages (axial leaded and UR). All axial devices shall be metallurgically bonded, non-cavity, double plug construction in accordance with the requirements of [MIL-PRF-19500](#). All glass body devices shall be designed with sufficient thermal compensation in the axial direction to optimize tensile and compressive stresses. Dimensional analysis is required of all materials used to achieve axial thermal compensation. Dimensional tolerances and corresponding coefficient of thermal expansion (CTE) shall be documented on the DLA Design and Construction Form 36D and shall be approved by the qualifying activity to maintain qualification. Dimensional tolerances shall be sufficiently tight enough to prevent excessive stresses due to the inherent CTE mismatch. The 'UR' version shall be structurally identical to the axial leaded versions except for end-cap lead attachment.

3.4.2.2 UB and UD packages. The cavity style UB and UD version devices shall be eutectically mounted and wire bonded in a ceramic package. Package styles UB and UBN with circuit designators CA, CC, and D to designate dual die configurations.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#). Manufacturer's identification and date code shall be marked on the devices. Initial container package marking shall be in accordance with [MIL-PRF-19500](#). The prefixes JAN, JANTX, or JANTXV may be abbreviated as J, JX, or JV, respectively. (Example: The PIN for an axial leaded device may be reduced from JANTXV1N4153UR-1 to JV4153). All marking which is omitted from the body of the device, except for polarity, shall appear on the initial container.

3.5.1 Axial lead devices. For axial lead devices only, the polarity shall be indicated with a contrasting color band to denote the cathode end. No color coding shall be permitted for part identification marking.

3.5.2 UR devices. For 'UR' version devices only, all PIN marking, except polarity, may be omitted from the device, but shall be retained on the initial container. Polarity marking of 'UR' devices shall consist as a minimum, a band or three contrasting dots around the periphery of the cathode. At the option of the manufacturer, 'UR' version devices may include laser marking on an end-cap, to include the PIN and lot date code for all quality levels.

3.5.3 UB devices. The 'UB' version devices do not require polarity marking.

3.5.4 UD devices. The 'UD' devices shall mark the cathode with a square symbol on the lid.

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3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#) herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see [4.4](#)).
- d. Element evaluation (see [4.6](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with [MIL-PRF-19500](#).

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANTX and JANTXV only). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. Specified electrical measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screening	JANTXV and JANTX level
3c (1)	Thermal impedance (see 4.3.2)
9	Not required
10	Method 1038 of MIL-STD-750 , condition A
11 (2)	I_{R1} and V_{F1}
12	See 4.3.1
13 (3) (4)	Subgroup 2 of table I herein; ΔI_{R1} = 100 percent of initial value or 15 nA dc, whichever is greater; ΔV_{F1} = 25 mV dc.

- (1) Thermal impedance shall be performed any time after sealing provided temperature cycling is performed in accordance with [MIL-PRF-19500](#), screen 3 prior to this thermal test.
- (2) Test within 24 hours after removal from test.
- (3) When thermal impedance is performed prior to screen 13, it is not required to be repeated in screen 13.
- (4) $PDA \leq 5$ percent.

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4.3.1 Power burn-in conditions. Power burn-in shall be performed in accordance with condition B of method 1038 of MIL-STD-750. The following conditions and those of 4.5.2 shall apply: V_R = rated V_{RWM} ; f = 50 to 60 Hz; $I_{O(min)}$ = 200 mA dc or I_F = 200 mA dc minimum = $I_{O(PCB)}$. T_A = +75 °C maximum. The maximum current density of small die shall be submitted to the qualifying activity for approval. Alternate mounting conditions shall be submitted to the qualifying activity for approval. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Thermal impedance measurements. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750, as applicable, using the guidelines in that method for determining I_H and I_M . Measurement delay time t_{MD} shall be 70 μ s maximum. The duration time t_H shall be 10 ms maximum. The thermal impedance limit shall comply with the thermal impedance graphs on figures 9 through 12 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3101 or 4081 of MIL-STD-750, as applicable. See group E, subgroup 4 of table II herein.

4.3.4 JAN testing. JAN level product shall have temperature cycling and thermal impedance testing performed in accordance with MIL-PRF-19500, JANTX level screening level requirements. Electrical testing shall be in accordance with table I, subgroup 2 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, table I herein, and as specified herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2. Axial leaded samples from the same lot may be used in lieu of UR style samples for life test.

Subgroup	Method	Conditions
B2	1056	0 °C to +100 °C, 10 cycles.
B2	1051	-55 °C to +175 °C, 45 cycles, including screening.
B2	2005	Not applicable to UR, UB, UBN and UD style package).
B3	1027	$V_{(pk)}$ = rated V_{RWM} ; f = 50 to 60 Hz; I_O = 200 mA dc minimum; adjust T_A or I_O to obtain a minimum T_J of +150 °C. (See 4.5.2.)
B4	2075	Design verification for UB and UBN style packages.
B4	2101	Decap analysis; scribe and break (not applicable for UB, UBN and UD style packages).
B6	1032	T_A = +175 °C for non UB style packages and T_A = +200 °C for UB and UD style packages.

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4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	1056	0 °C to +100 °C, 10 cycles.
C2	1051	–55 °C to + 175 °C, 45 cycles including screening.
C2	2036	Tension - test condition A; weight = 10 pounds (4.54 kg), t = 15 seconds; lead fatigue = condition E (not applicable to UR, UB, UBN and UD style packages).
C5	4081	L = .375 inch (9.53 mm), $R_{\theta JL} = 250$ °C/W maximum; $R_{\theta JEC} = 100$ °C/W; (see 4.3.2), 22 devices, c = 0.
C6	1026	1,000 hours minimum, $V(pk) = \text{rated } V_{RWM}$; f = 50 to 60 Hz; $I_O = 200$ mA dc minimum; adjust T_A or I_O to obtain a minimum T_J of +150 °C. (See 4.5.2.)

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Free air power burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each device under test still sees the full I_O (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. Method 3100 of [MIL-STD-750](#) shall be used to measure T_J .

4.5.3 Scope display evaluation. The reverse characteristics shall be inspected and evaluated in accordance with condition A of method 4023 of [MIL-STD-750](#). Each device shall be evaluated only for the following 4 commonly observed faults: drift, unstable (jitter), snap back collapsing $V_{(BR)}$ and floater. Any instance of any of these 4 faults in the trace shall be cause for rejection.

4.6 Element evaluation of un-encapsulated die. The element evaluation of un-encapsulated die shall be in accordance with appendix G of [MIL-PRF-19500](#). The element evaluation may be accomplished utilizing a TO-205 package in lieu of the DO-204, DO-213, or UB packages.

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TABLE I. Group A inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance	3101	See 4.3.2	Z _{θJX}			°C/W
Forward voltage	4011	Condition B, pulsed (see 4.5.1); I _F = 100 μA dc	V _{F1}	0.49	0.55	V dc
Forward voltage	4011	Condition B, pulsed (see 4.5.1); I _F = 250 μA dc	V _{F2}	0.53	0.59	V dc
Forward voltage	4011	Condition B, pulsed (see 4.5.1); I _F = 1 mA dc	V _{F3}	0.59	0.67	V dc
Forward voltage	4011	Condition B, pulsed (see 4.5.1); I _F = 2 mA dc	V _{F4}	0.62	0.70	V dc
Forward voltage	4011	Condition B, pulsed (see 4.5.1); I _F = 10 mA dc	V _{F5}	0.70	0.81	V dc
Reverse current	4016	Condition A or B, V _R = 50 V dc	I _{R1}		50	nA dc
Breakdown voltage All devices except UD UD package devices	4021	I _R = 5 μA dc	V _{BR1} V _{BR1}	100 75		V dc V dc
<u>Subgroup 3</u>						
High temperature operation:		T _A = +150 °C				
Reverse current	4016	Condition A or B, V _R = 50 V dc	I _{R2}		50	μA dc
Low temperature operation:		T _A = −55 °C				
Breakdown voltage All devices except UD UD package devices	4021	I _R = 5 μA dc	V _{BR2} V _{BR2}	75 75		V dc V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	Method	MIL-STD-750 Conditions	Symbol	Limit	Limit	Unit
				Min	Max	
<u>Subgroup 4</u>						
Junction capacitance	4001	$V_R = 0$ V dc, $f = 1$ MHz, $V_{sig} = 50$ mV (pk to pk), max	C		2.0	pF
Reverse recovery time	4031	Condition A, $I_F = I_{RM} = 10$ mA dc	t_{rr}		4	ns
Scope display evaluation	4023	See 4.5.3				
<u>Subgroup 5</u>						
Not applicable						
<u>Subgroup 6</u>						
Surge current	4066	Condition A (sine wave), $I_{f(surge)} = 2$ A(pk), $I_O = 0$, $V_{RM} = 0$, 10 surges, 8.3 ms width each, one surge per minute, $T_A = +25$ °C or Condition B (square wave) $I_{F(surge)} = 4$ A (pk) 10 surges, 1µs width each, duty factor = 0.0055 percent, $T_A = +25$ °C				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 7</u>						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.

2/ Dual die devices (UBCA, UBCC, UBD, and UBND) devices shall have each diode tested individually.

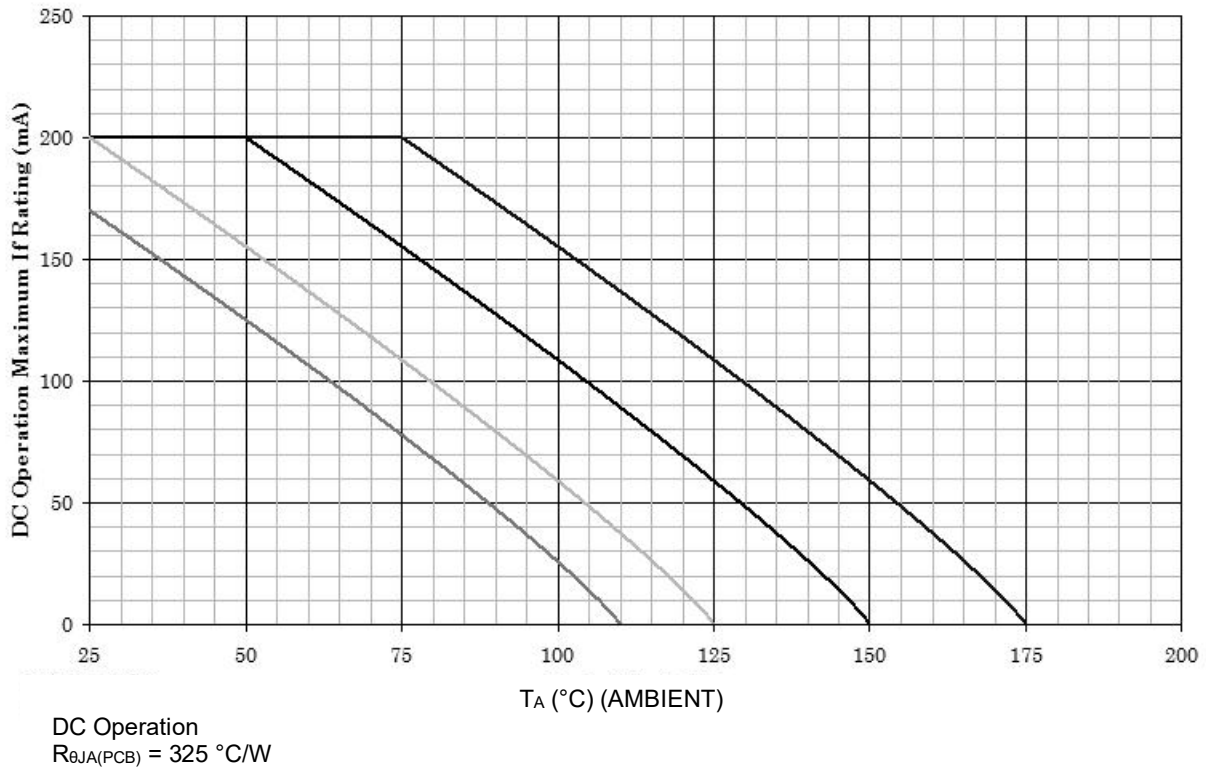
3/ Electrical characteristics for all surface mount versions are identical to the corresponding axial leaded versions unless otherwise specified.

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TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Thermal shock (glass strain)	1056	100 cycles 0 °C to +100 °C	
Temperature cycling	1051	500 cycles, -65 °C to +175 °C	
Hermetic seal	1071	Gross leak only for round body axial and UR versions. Fine and gross leak required for all UB, UBN and UD versions.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2</u>			45 devices, c = 0
Intermittent operating life	1037	10,000 cycles; I _f = 300 mA dc, T _{on} = T _{off} = 1 minute	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			15 devices, c = 0
Thermal resistance	4081	R _{θJSP} can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets)	
Thermal impedance curves		See MIL-PRF-19500 , table E-IX, group E, subgroup 4	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices
Resistance to glass cracking	1057	Test condition B. Test until failure occurs or to a maximum of 25 cycles, whichever comes first. Not required for UB, UBN and UD versions.	
<u>Subgroup 9</u>			22 devices, c = 0
Monitored mission temperature cycling	1055	Not required for UB, UBN and UD versions	
Electrical measurements		See table I , subgroup 2	

Temperature-Current Derating Curve
1N4153-1, 1N4153UR-1, 1N4534

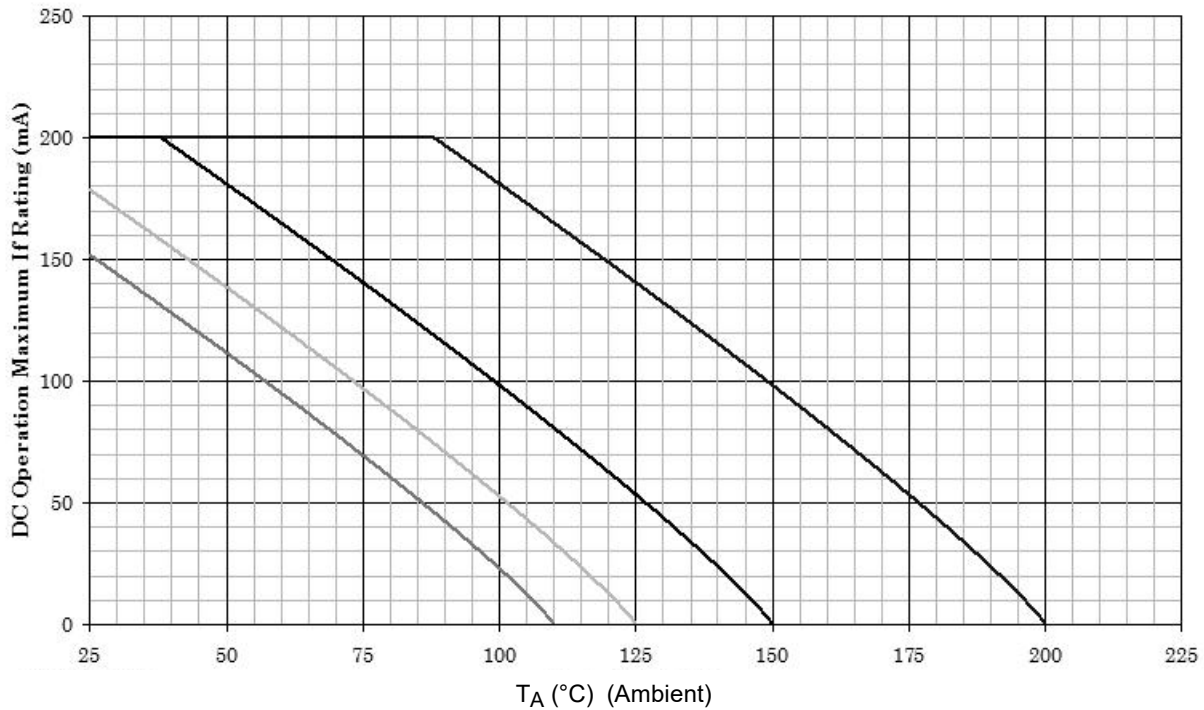


NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 175\text{ }^{\circ}\text{C}$) and current rating specified (see 1.3).
3. Derate design curve chosen at $T_J \leq 150\text{ }^{\circ}\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125\text{ }^{\circ}\text{C}$, and $110\text{ }^{\circ}\text{C}$ to show current rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-current derating graph (all devices).

**Temperature-Current Derating Curve
1N4153UB, 1N4534UB versions**



DC Operation

NOTE: Max Finish-Alloy Temp = 200 °C

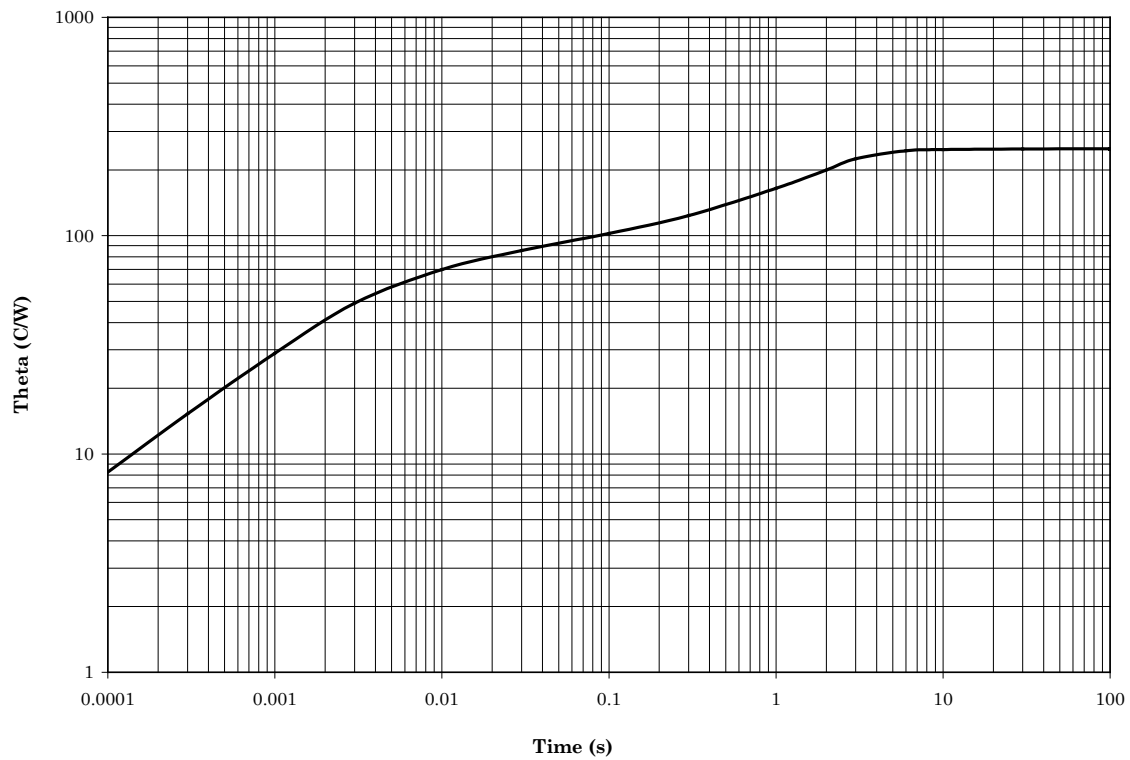
Thermal Resistance Junction to Ambient = 325 °C/W

NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200$ °C) and current rating specified (see 1.3.).
3. Derate design curve chosen at $T_J \leq 150$ °C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125$ °C, and 110 °C to show current rating where most users want to limit T_J in their application.

FIGURE 8. Temperature-current derating graph (UB versions).

Maximum Thermal Impedance Plots
1N4153-1 (DO-204AH), 1N4534 (DO-204AG)
 $T_L = 25^\circ\text{C}$

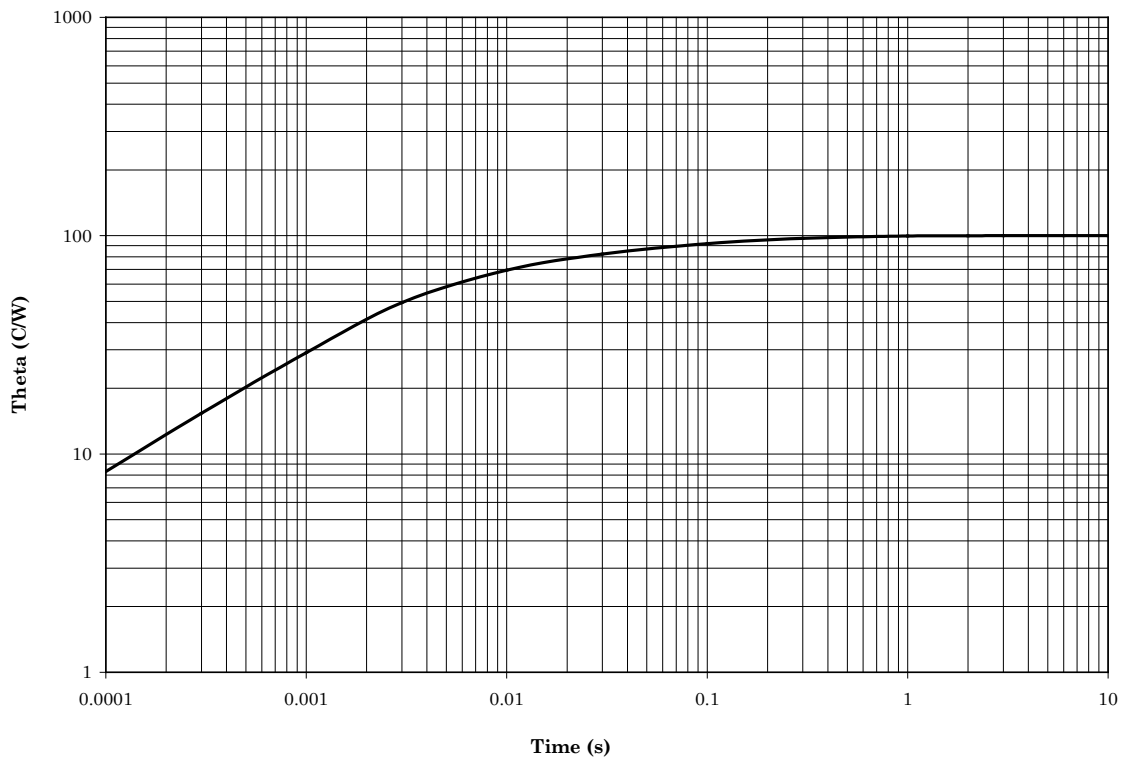


$R_{\theta JL} = 250^\circ\text{C/W}$

NOTE: $Z_{\theta JX} = 70^\circ\text{C/W}$ maximum at $t_H = 10\text{ms}$.

FIGURE 9. Thermal impedance (axial lead versions).

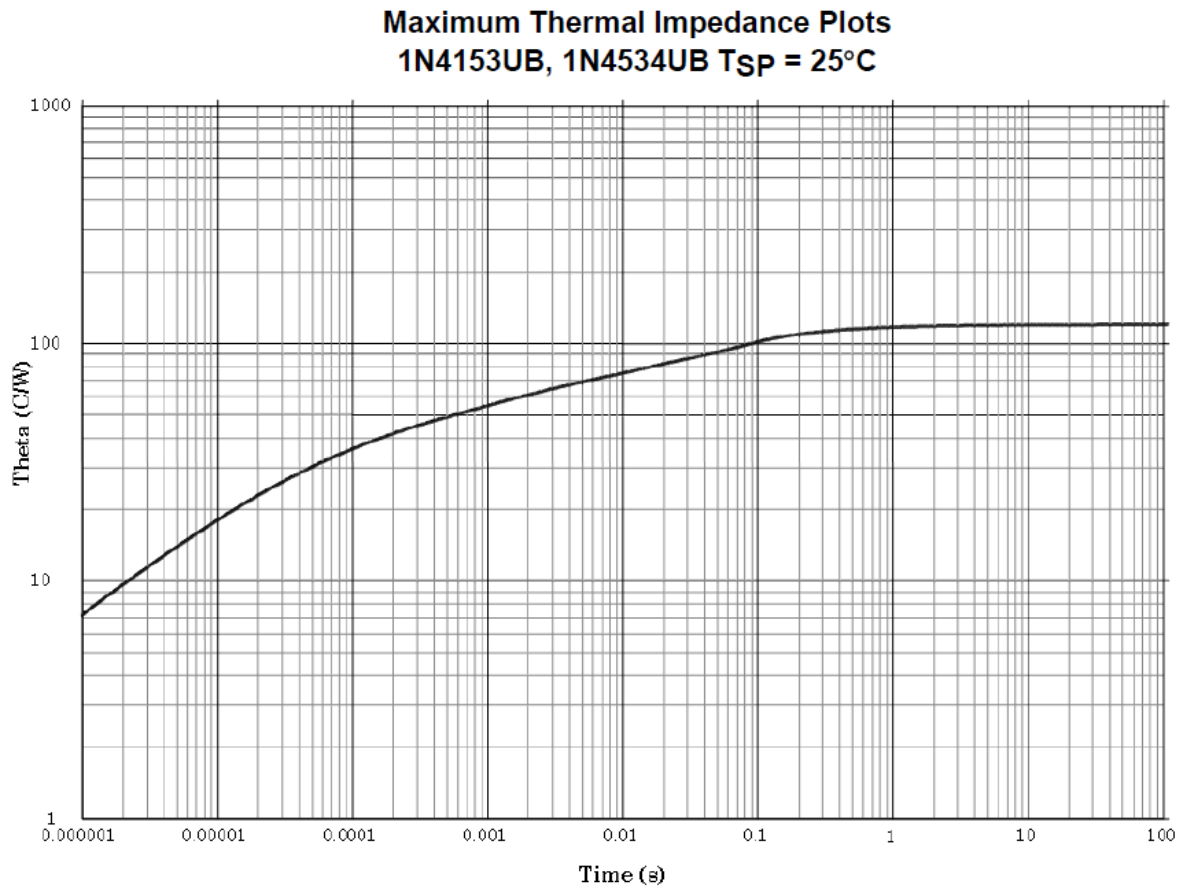
Maximum Thermal Impedance Plots
1N4153UR-1 (DO-213AA)
 $T_{EC} = 25\text{ }^{\circ}\text{C}$



$R_{\theta JEC} = 100\text{ }^{\circ}\text{C/W}$

NOTE: $Z_{\theta JX} = 70\text{ }^{\circ}\text{C/W}$ maximum at $t_H = 10\text{ms}$.

FIGURE 10. Thermal impedance (MELF surface mount versions).

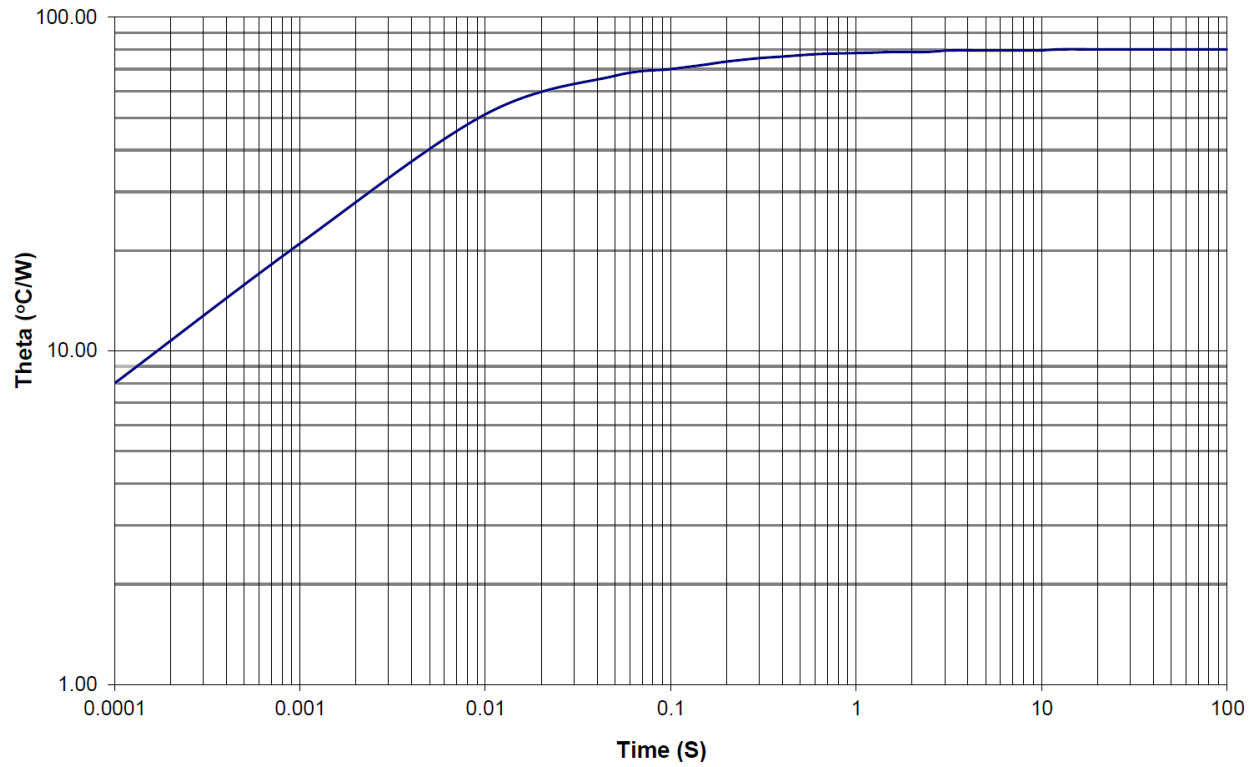


$R_{\theta JSP} = 120^{\circ}\text{C/W}$

NOTE: $Z_{\theta JX} = 75^{\circ}\text{C/W}$ maximum at $t_H = 10\text{ms}$.

FIGURE 11. Thermal impedance (UB versions).

Maximum Thermal Impedance Plots
1N4153UD, 1N4534UD
 $T_{SP} = 25\text{ }^{\circ}\text{C}$



$R_{\theta JSP} = 80\text{ }^{\circ}\text{C/W}$

NOTE: $Z_{\theta JX} = 51\text{ }^{\circ}\text{C/W}$ maximum at $t_H = 10\text{ms}$.

FIGURE 12. Thermal impedance (UD versions).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

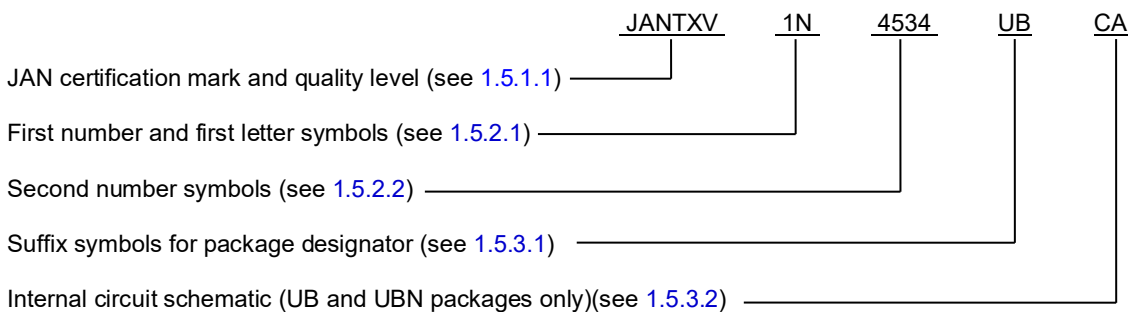
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. Destructive physical analysis when requested.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

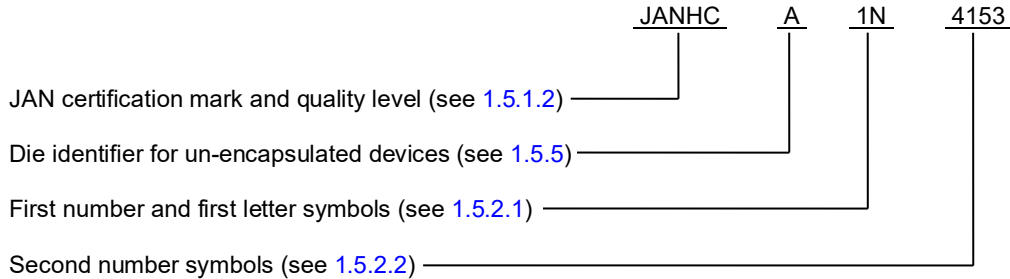
6.4 PIN construction examples. The PINs for encapsulated and un-encapsulated devices and are constructed using the following forms.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



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6.4.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.5 List of PINs.

6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
Axial through-hole mount (similar to DO-204AG and DO-204AH)		
JAN1N4153-1	JANTX1N4153-1	JANTXV1N4153-1
JAN1N4534	JANTX1N4534	JANTXV1N4534
Surface mount version (UR)		
JAN1N4153UR-1	JANTX1N4153UR-1	JANTXV1N4153UR-1
JAN1N4534UR	JANTX1N4534UR	JANTXV1N4534UR
Single die surface mount version (UB, UBN and UD)		
JAN1N4153UB	JANTX1N4153UB	JANTXV1N4153UB
JAN1N4534UB	JANTX1N4534UB	JANTXV1N4534UB
JAN1N4153UBN	JANTX1N4153UBN	JANTXV1N4153UBN
JAN1N4534UBN	JANTX1N4534UBN	JANTXV1N4534UBN
JAN1N4534UD	JANTX1N4534UD	JANTXV1N4534UD
Dual die surface mount version (UB, UBN, and UD)		
JAN1N4153UBCA	JANTX1N4153UBCA	JANTXV1N4153UBCA
JAN1N4153UBCC	JANTX1N4153UBCC	JANTXV1N4153UBCC
JAN1N4153UBD	JANTX1N4153UBD	JANTXV1N4153UBD
JAN1N4153UBND	JANTX1N4153UBND	JANTXV1N4153UBND
JAN1N4153UD	JANTX1N4153UD	JANTXV1N4153UD

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6.5.2 PINs for un-encapsulated devices (die). The following is a list of possible PINs for un-encapsulated devices available on this specification sheet. The qualified JANHC and JANKC suppliers with the applicable letter version will be identified on the QML.

PINs for die of the "HC" quality level	PINs for die of the "KC" quality level
JANHCA1N4153	JANKCA1N4153
JANHCA1N4534	JANKCA1N4534

6.6 Substitution and supersession information.

6.6.1 Substitutability of dash one (-1) devices. The non-dash-one version of device type 1N4153 that were in previous revisions of this document have been deleted from this specification as of MIL-PRF-19500/337H, dated 5 November 2003. The dash-one (-1) devices are a direct substitute for non-dash-one devices and are preferred.

6.6.2 Superseded PINs. The following supersession data applies to PINs associated with this document:

Superseding PIN as specified within MIL-PRF-19500/337H, dated 5 November 2003	Superseded PIN as specified within MIL-S-19500/337(NAVY), dated 20 May 1966
1N4153-1	1N4153

6.6.3 Obsolete device types. Device type 1N3606 as it existed on MIL-S-19500/337(NAVY) dated 20-MAY-1966 was removed with the issuance of MIL-S-19500/337C dated 21-OCT-1972. No supersession or substitution information is available for this obsolete device type.

6.7 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA1N4153) will be identified on the QML.

JANC ordering information	
PIN	Manufacturer
	43611
1N4153	JANHCA1N4153, JANKCA1N4153
1N4534	JANHCA1N4534, JANKCA1N4534

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

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6.9 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:

Army – CR
Navy – SH
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:

DLA – CC

(Project 5961–2025–035)

Review activities:

Army – AR, MI, SM
Navy – AS
Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.